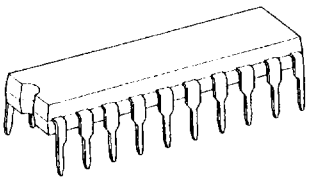
TC9806P, TC9806FW

TENTATIVE DATA

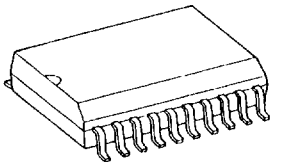
TC9806 is a 20-pin CMOS programmable logic device (PLD) based on EEPROM cells. It has a zero-standby function. Designed using Toshiba's original technology, this device features low power dissipation and a wide operating voltage range (2V to 5.25V), and is applicable to a variety of electronic devices.
The device functions as a dedicated address coder, based on an AND array structure.

TC9806P



DIP20-P-300A

TC9806FW



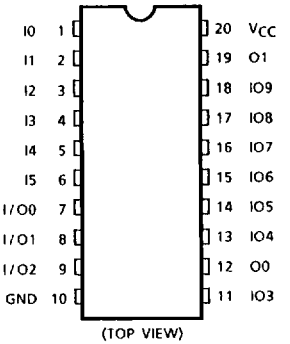
SOL20-P-300

Weight DIP20-P-300A : 1.30g (Typ.)
SOL20-P-300 : 0.46g (Typ.)

FEATURES

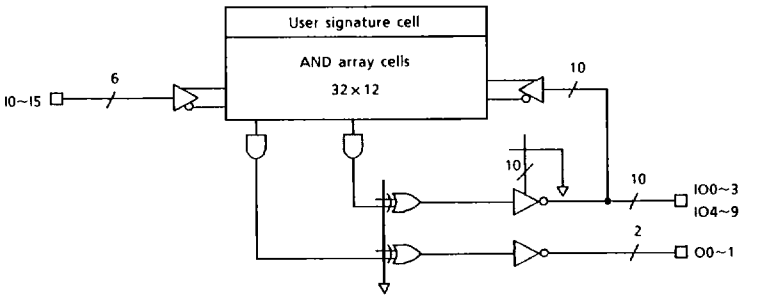
- Architecture ..... 12 AND terms
  12 exclusive OR terms
- Security cell ..... Protection of proprietary information
- Signature word ..... 12 bits for user ID code or inventory control
- High speed operation ..... t_{pd} (input-output) = 11ns (Typ.)
- Low power dissipation ..... I_{CC} (standby) = 4μA (max. @25°C)
- Wide operating voltage range .... V_{CC} = 2~5.25V
- Package ..... 20-pin plastic DIP (TC9806P)
  20-pin plastic SOL (TC9806FW)

PIN NAMES & FUNCTIONS



I0~I5	Input only
O0, O1	Output only
I/O0~I/O9	Input / output

FUNCTION DIAGRAM



ARCHITECTURE

1. MEMORY CELLS

   Programmable memory cells are divided into the following four types : AND array, input/output control array, flag, and user signature.
   Setting program data to 1 disconnects signals to an AND/OR array : setting to 0 connects.

   (1) AND array (32 × 12)

   Programs signals used to control 10 input/outputs. Setting the program data to 1 sets input/output pins to output ; to 0 sets input/output pins to input .

   (2) Input/Output control array (10)

   Setting program data to 1 disconnects signals to an AND array : setting to 0 connects. Output from this array enables CMOS output (I/O0~I/O9).

   (3) Flag cell

   A. Output polarity selection cell .... 12 bits

   B. Security cell ..... 1 bit

   (4) User signature cell

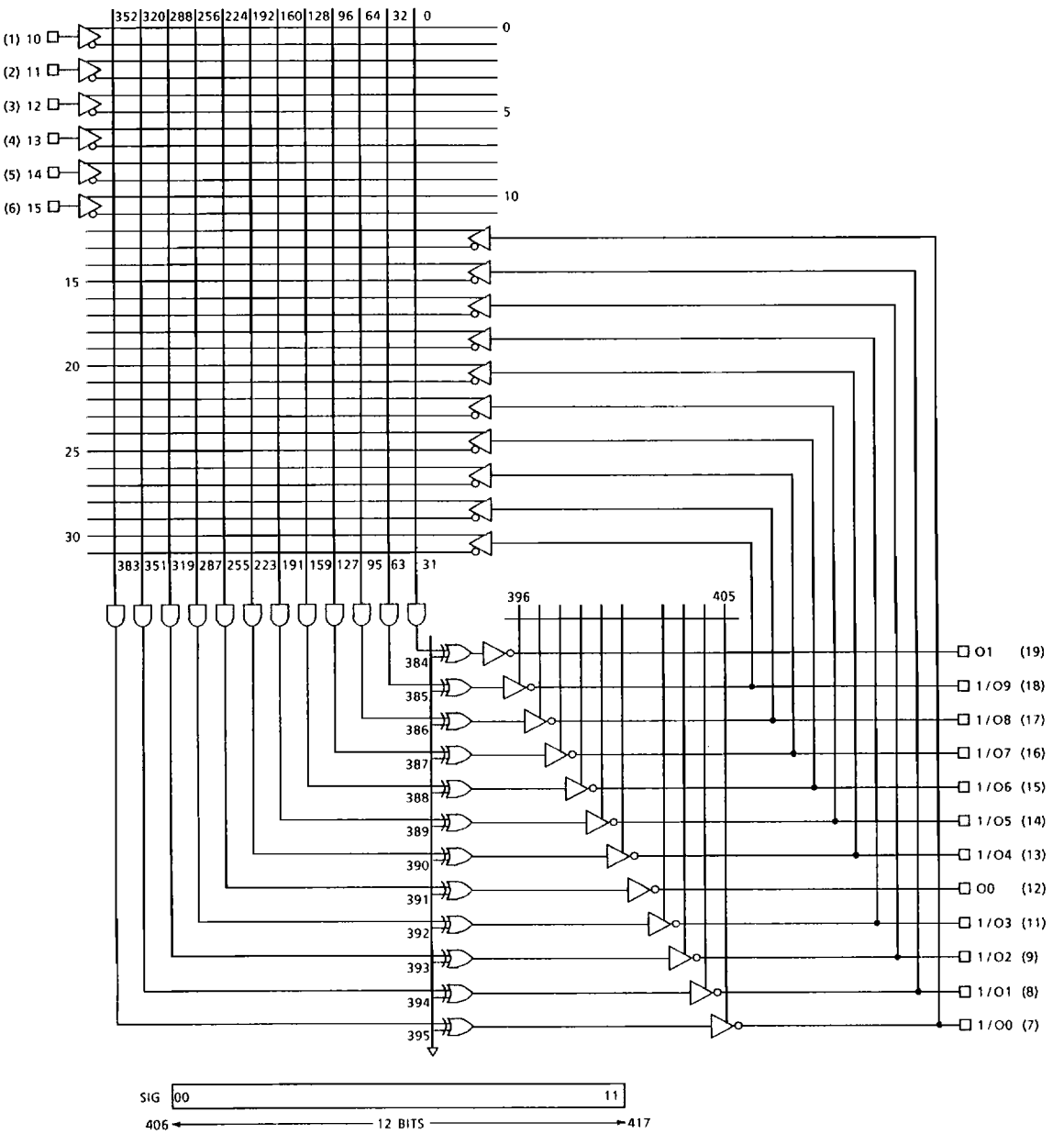
   User can program a 12-bit memory array for a variety of uses including ID codes, inventory control, and revision number. Programming the security bit (security cell) disables access of cells other than the signature cell.

2. Macro cells

   (1) Output polarity of AND array

   Twelve exclusive OR gates control the output polarity of the AND array. These gates are user programmable : setting program data to 1 inputs the output signal from the AND array as inverted ; setting program data to 0, as non-inverted.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500 (DIP) */300 (SOL)	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature (10s)	T_L	300	°C

* 500mW in the range of Ta = −40~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~5.25	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 5.0V ± 0.25V)	ns

DC ELECTRICAL CHARACTERISTICS

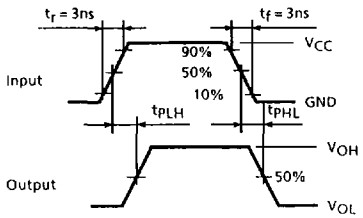
PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITION		V_{CC}	Ta = 25°C MIN.	TYP.	MAX.	Ta = −40 ~ 85°C MIN.	MAX.	UNIT
High-level input voltage	V_{IH}	—			2.0	1.5	—	—	1.5	—	V
					3.0	2.10	—	—	2.10	—	
					5.25	3.67	—	—	3.67	—	
Low-level input voltage	V_{IL}	—			2.0	—	—	0.5	—	0.5	V
					3.0	—	—	0.9	—	0.9	
					5.25	—	—	1.57	—	1.57	
High-level output voltage	V_{OH}	—	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	2.0	1.9	2.0	—	1.9	—	V
					3.0	2.9	3.0	—	2.9	—	
					5.25	5.15	5.25	—	5.15	—	
				I_{OH} = −6mA	4.75	4.43	4.56	—	4.38	—	
Low-level output voltage	V_{OL}	—	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0	—	0.0	0.1	—	0.1	V
					3.0	—	0.0	0.1	—	0.1	
					5.25	—	0.0	0.1	—	0.1	
				I_{OL} = 6mA	4.75	—	0.18	0.26	—	0.33	
Input leakage current	I_{IN}	—	V_{IN} = V_{CC} or GND		5.25	—	—	±0.1	—	±1.0	μA
Quiescent current	I_{CCSB}	—	V_{IN} = V_{CC} or GND Standby		5.25	—	—	4.0	—	40.0	μA
Operating current	I_{CCOP}	—	f_{IN} = 1MHz Operating		5.25	—	—	—	—	12.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 25pF, Input $t_r = t_f$ = 3ns)

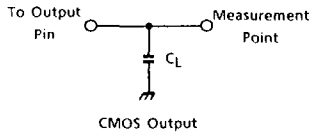
PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITION	V_{CC}	Ta = 25°C MIN.	TYP.	MAX.	Ta = −40 ~ 85°C MIN.	MAX.	UNIT
Propagation Delay Time (Input, I/O-Output)	t_{PLH} t_{PHL}	—		2.0	—			—		ns
				3.0	—			—		
				5 ± 0.25	—	12.0	18.0	—	21.0	

Switching Characteristic Test Waveform

1) t_{PD} (t_{PLH}, t_{PHL})



Output Test Connection Diagram



Note) C_L includes the capacitance of probe.