μPD424258
262,144 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424258 is a static-column dynamic RAM organized as 262,144 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. The data outputs are returned to high impedance by returning $\overline{CS}$ high. Static-column read and write cycles can be executed by switching the column address inputs.

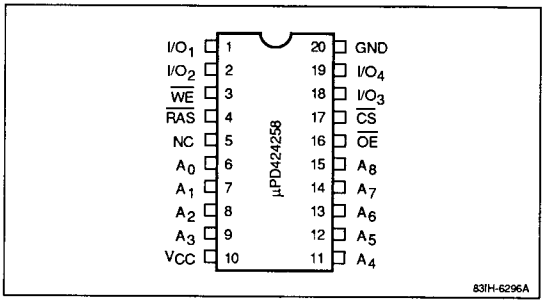
Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read and write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms refresh period.

Features

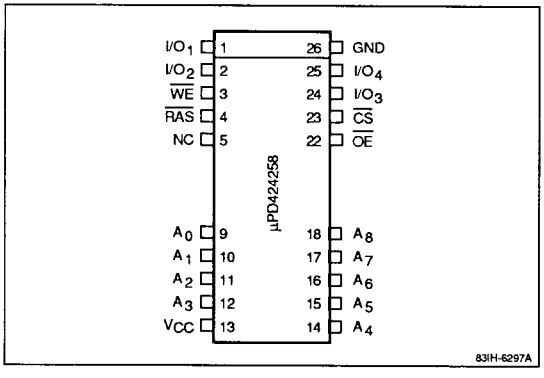
- 262,144-word by 4-bit organization
- Single +5-volt ±10% power supply
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state I/O
- Low input capacitance
- TTL-compatible inputs and outputs
- 512 refresh cycles every 8 ms
- High-density 20-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

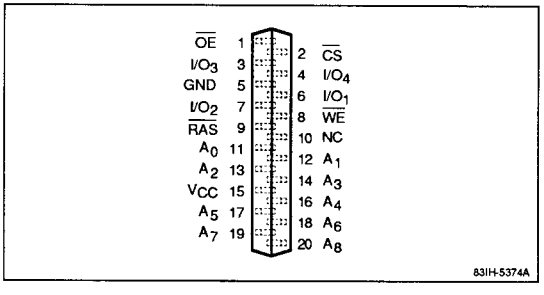
20-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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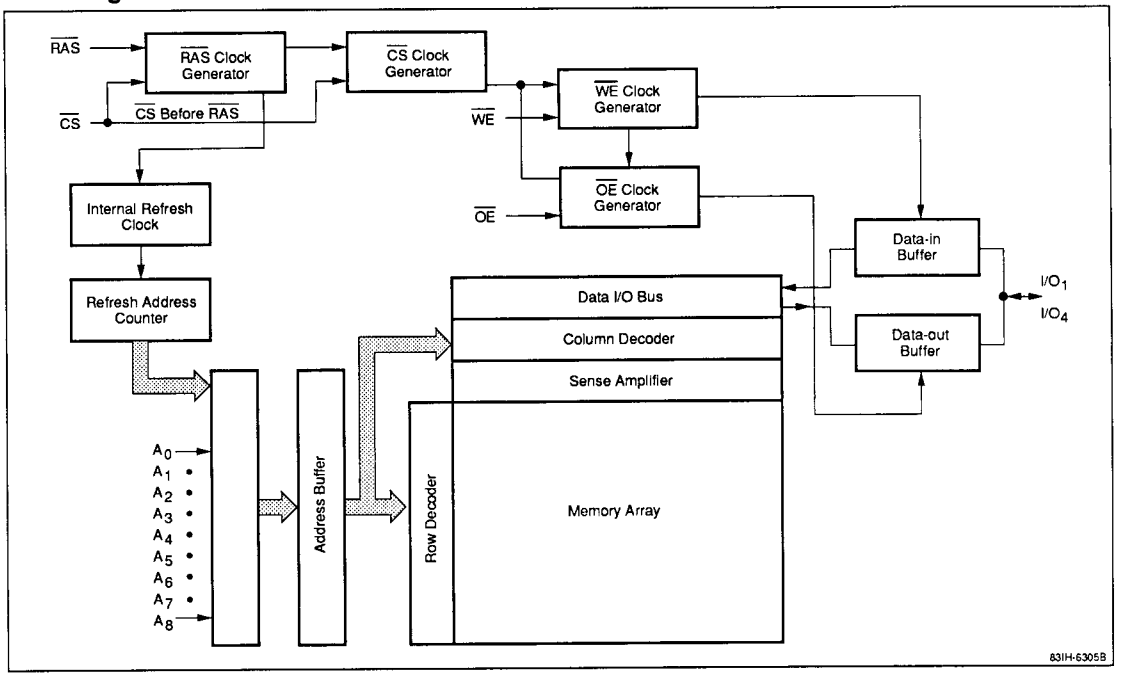
TSOP package will be available in 1991.

Block Diagram



Ordering Information

Part Number	RAS Access Time (max)	R/W Cycle Time (max)	Static-Column Access (max)	Package
μPD424258C-60	60 ns	120 ns	35 ns	20-pin plastic DIP
C-70	70 ns	130 ns	40 ns	
C-80	80 ns	160 ns	50 ns	
C-10	100 ns	190 ns	60 ns	
μPD424258LA-60	60 ns	120 ns	35 ns	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	40 ns	
LA-80	80 ns	160 ns	50 ns	
LA-10	100 ns	190 ns	60 ns	
μPD424258V-60	60 ns	120 ns	35 ns	20-pin plastic ZIP
V-70	70 ns	130 ns	40 ns	
V-80	80 ns	160 ns	50 ns	
V-10	100 ns	190 ns	60 ns	

Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_4	Data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_{IO}	7	pF	I/O_1 - I/O_4

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

DC Characteristics

T_A = 0 to +70 °C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CS}$ = V_{IH}
				1.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$, $\overline{CS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Static-column operating current, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS}$ = $\overline{CS}$ = V_{IL}; addresses cycling; t_{RSC} = t_{RSC} min or t_{WSC} = t_{WSC} min (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10)
Column address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		80		100		ns	(Note 18)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		80		ns	(Note 17)
Column address hold time referenced to $\overline{RAS}$ (write cycle)	t_{AWR}	N/A		N/A		60		60		ns	
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CS}$ precharge time, static-column cycle	t_{CP}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 13)
$\overline{CS}$ pulse width	t_{CS}	20	100,000	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		55		ns	(Note 17)
Write command to $\overline{CS}$ lead time	t_{CWL}	15		15		20		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 16)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	(Note 18)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 16)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	(Note 7)
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}		15		15		20		25	ns	(Note 11)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output hold time from address	t_{OH}	5		5		5		5		ns	
Output enable time from $\overline{WE}$	t_{OW}		25		25		25		30	ns	(Note 7)
Access time from previous $\overline{WE}$ (falling edge)	t_{PWA}		60		70		90		110	ns	(Notes 7, 19)
Column address hold time from previous $\overline{WE}$ (falling edge)	t_{PWH}	60		70		90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, static-column cycle	t_{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	(Note 14)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 14)
Static-column read cycle time	t_{RSC}	35		40		50		60		ns	(Note 6)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay	t_{RSW}	75		85		95		115		ns	
Read-write cycle time	t_{RWC}	165		175		215		255		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		130		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Static-column read-write cycle time	t_{RWSC}	85		95		120		145		ns	(Note 6)
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Previous $\overline{WE}$ (falling edge) to column address delay time	t_{WAD}	20	30	22	35	20	45	25	55	ns	(Note 19)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	(Note 18)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 17)
Write invalid time	t_{WI}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 15)
Static-column write cycle time	t_{WSC}	35		40		50		60		ns	(Note 6)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (-1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}, t_{AA} or t_{OEA}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CS}$ cycles preceded by any cycle.

(14) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(16) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

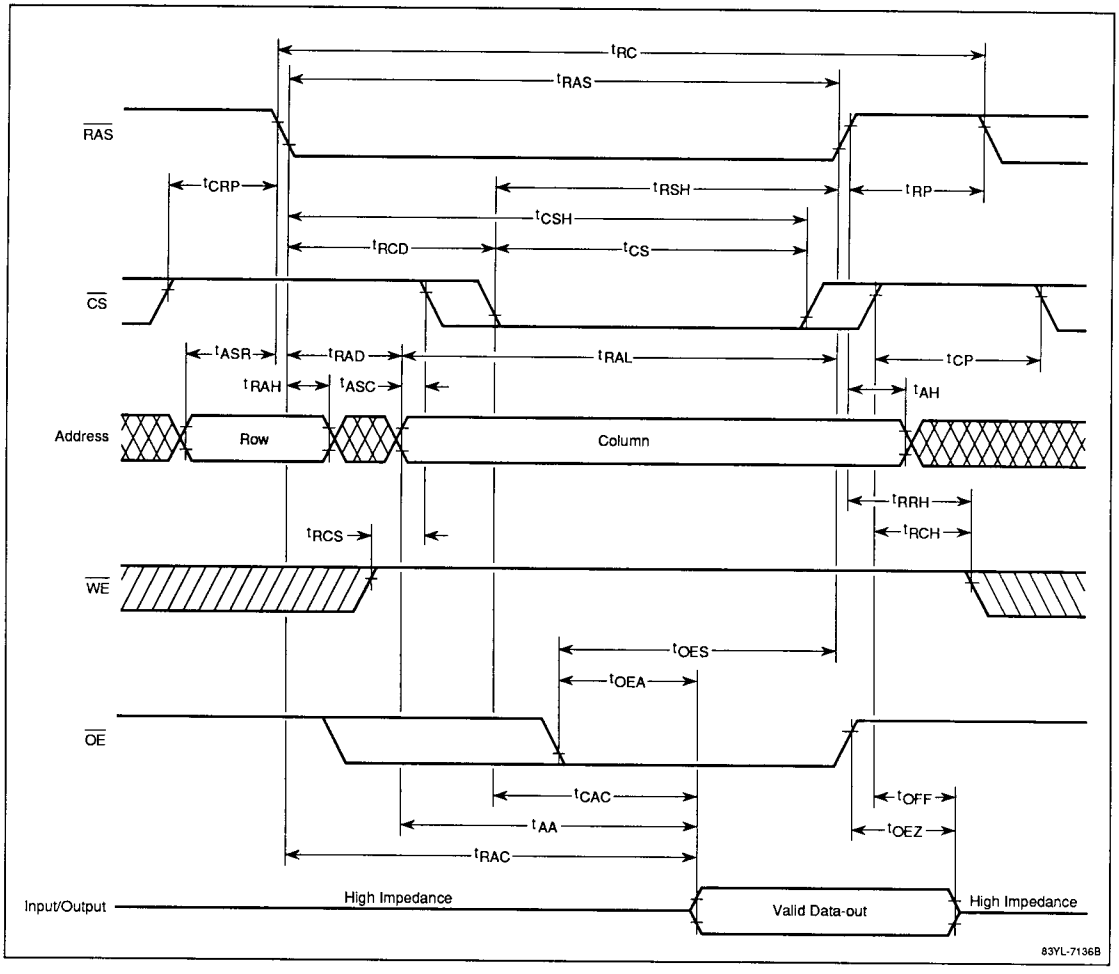
(17) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

(18) This parameter is not needed for the μPD421000-60 and μPD421000-70.

(19) If $t_{WAD} \leq t_{WAD}$ (max), then access time is defined by t_{PWA}.

Timing Waveforms

Read Cycle



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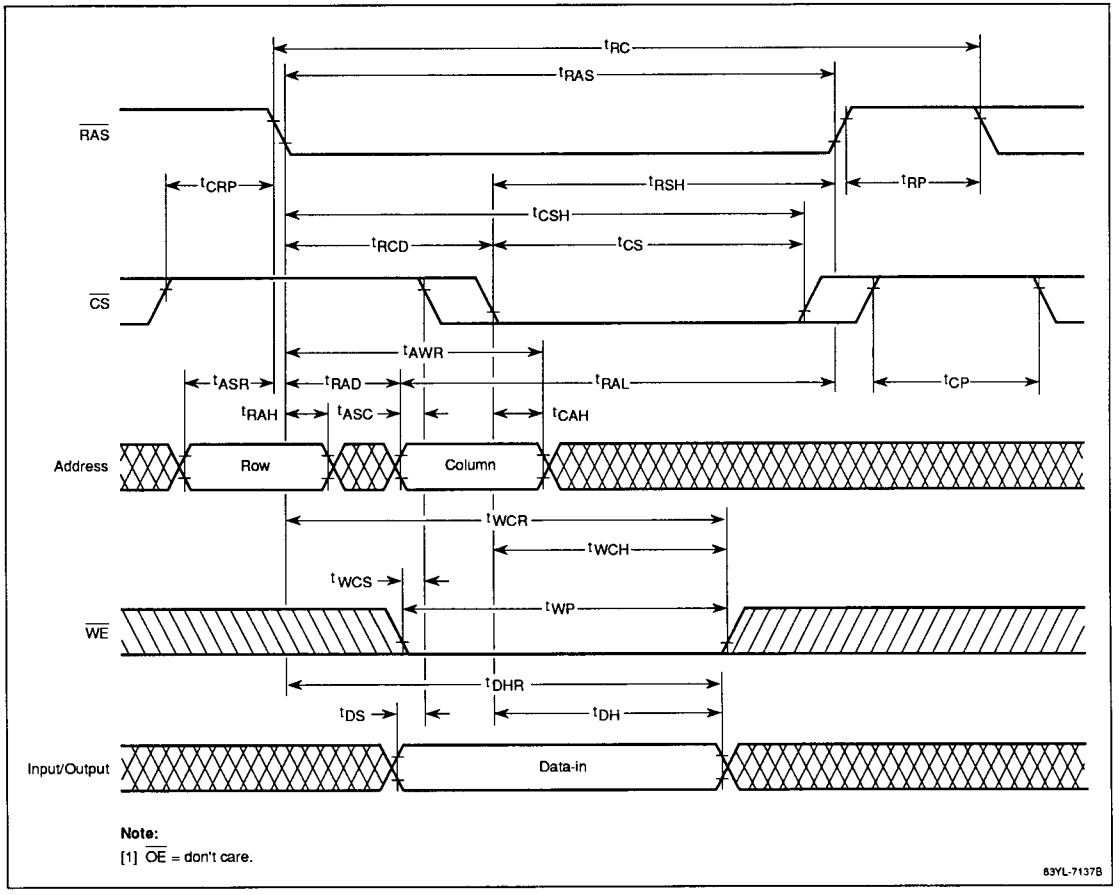
Timing Waveforms (cont)

Early Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

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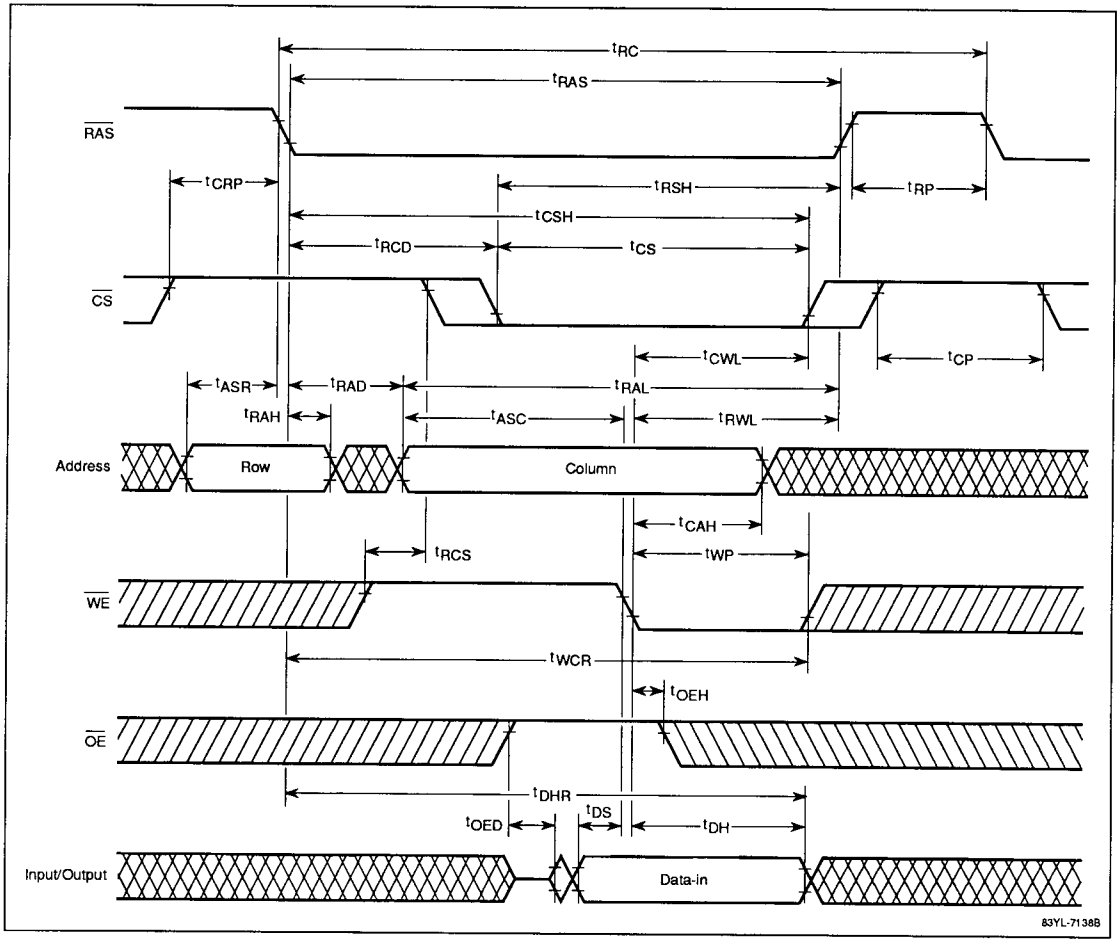
Timing Waveforms (cont)

Late Write Cycle



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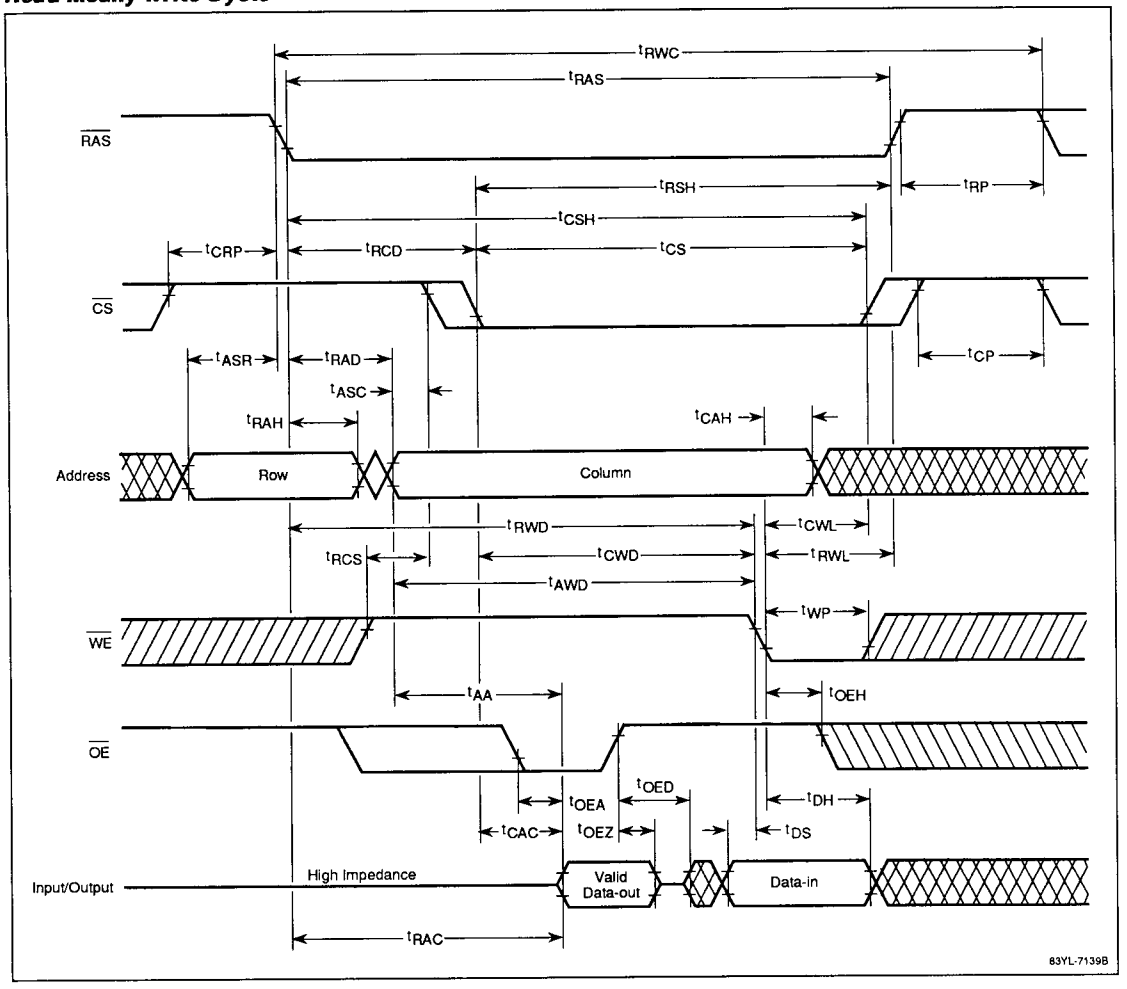
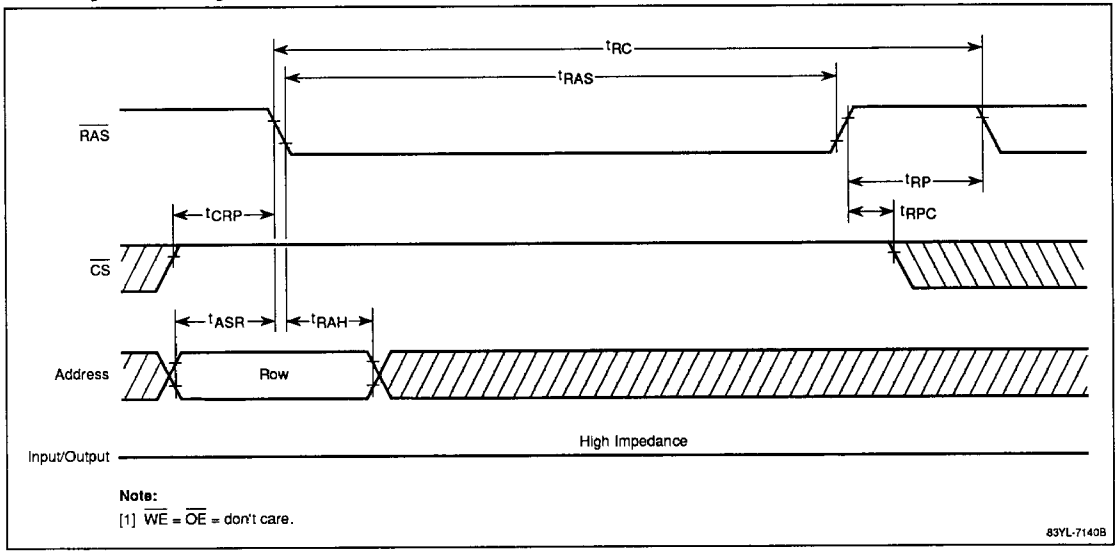
Timing Waveforms (cont)

Read-Modify-Write Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

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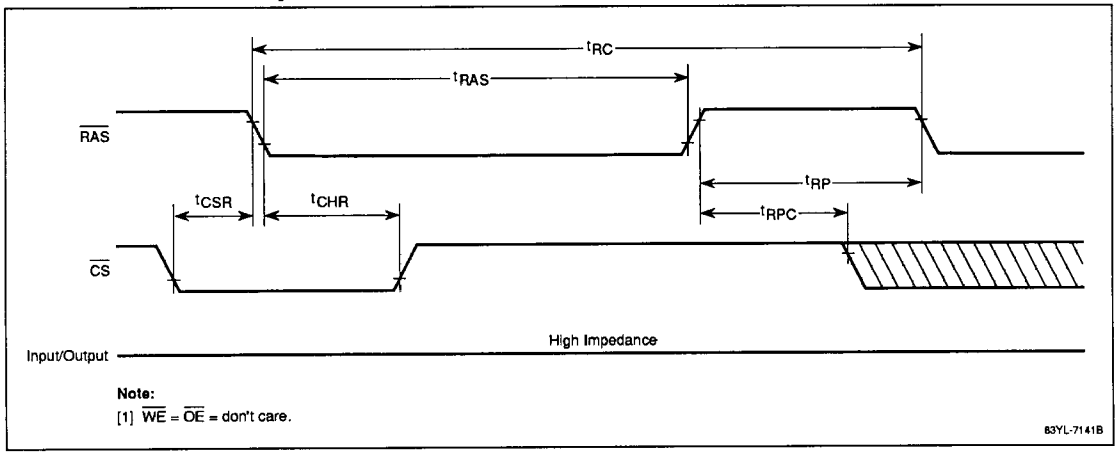
$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

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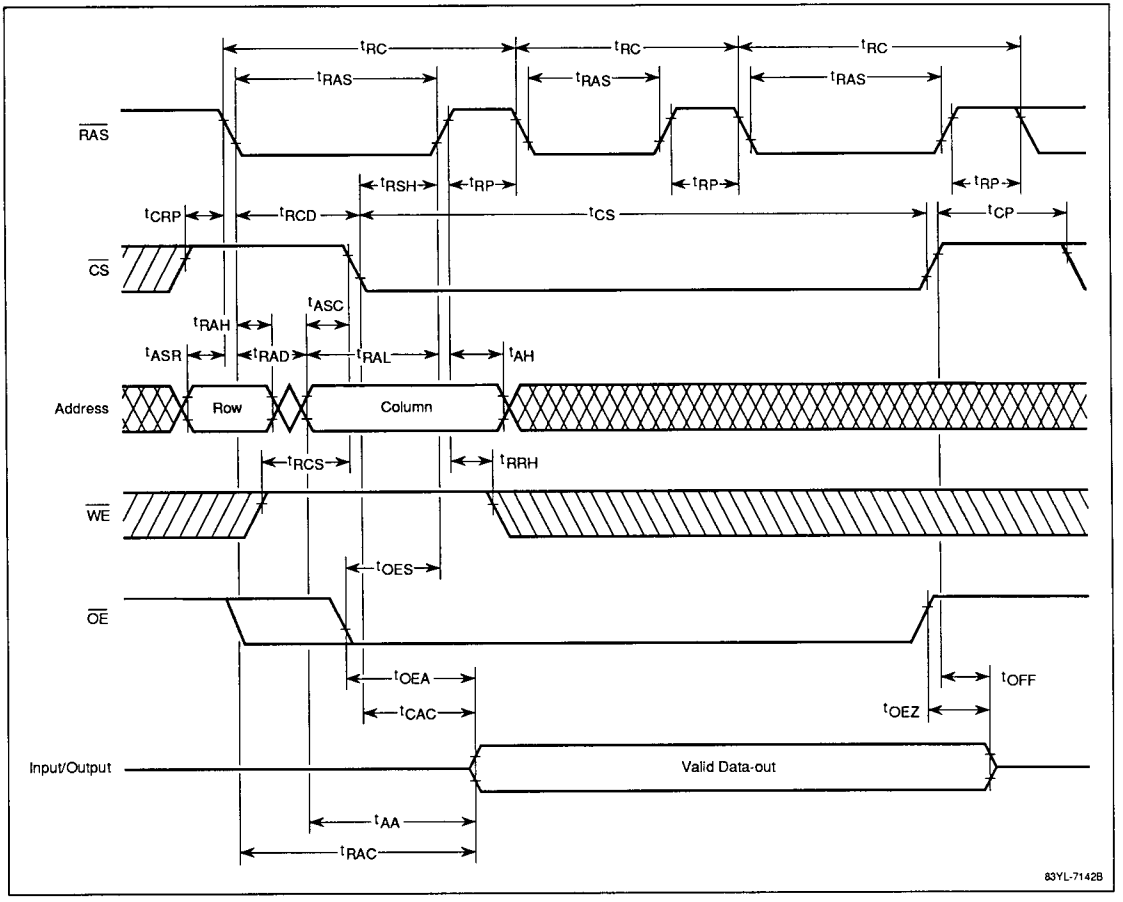
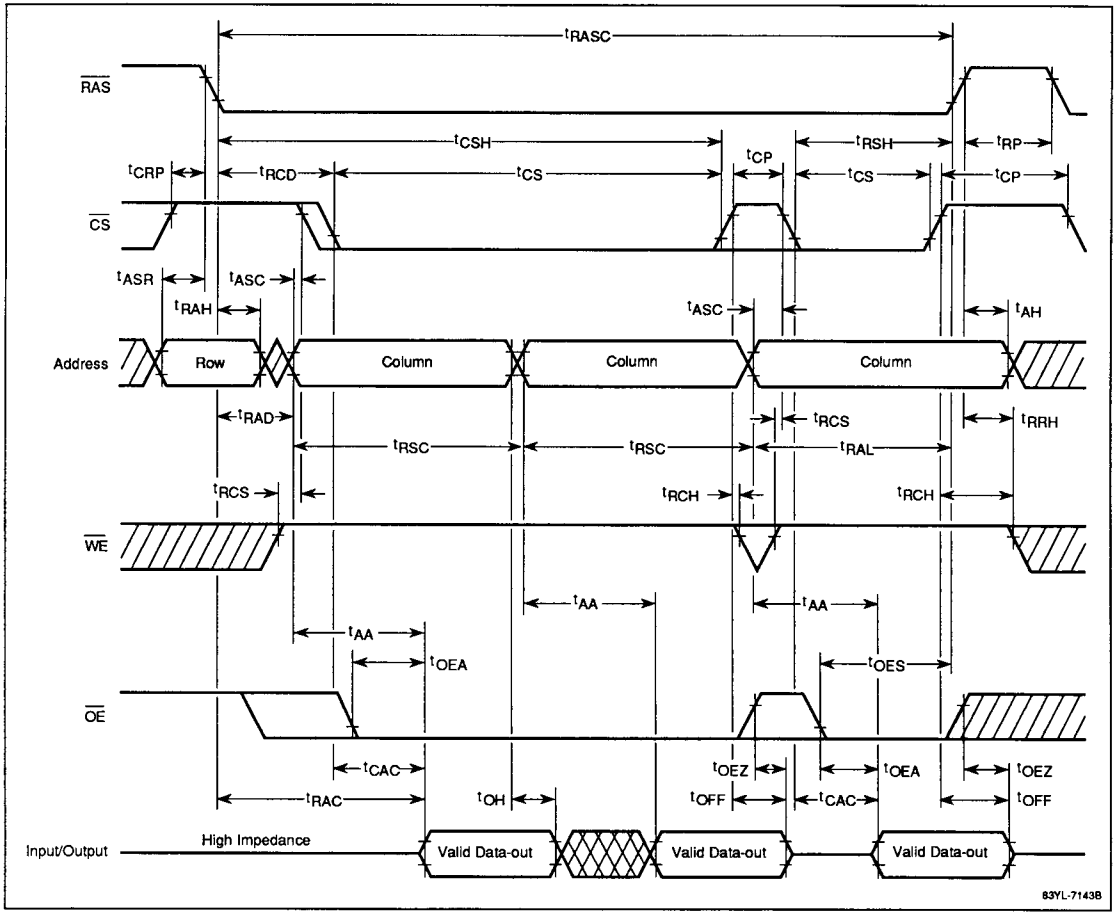
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

Static-Column Read Cycle



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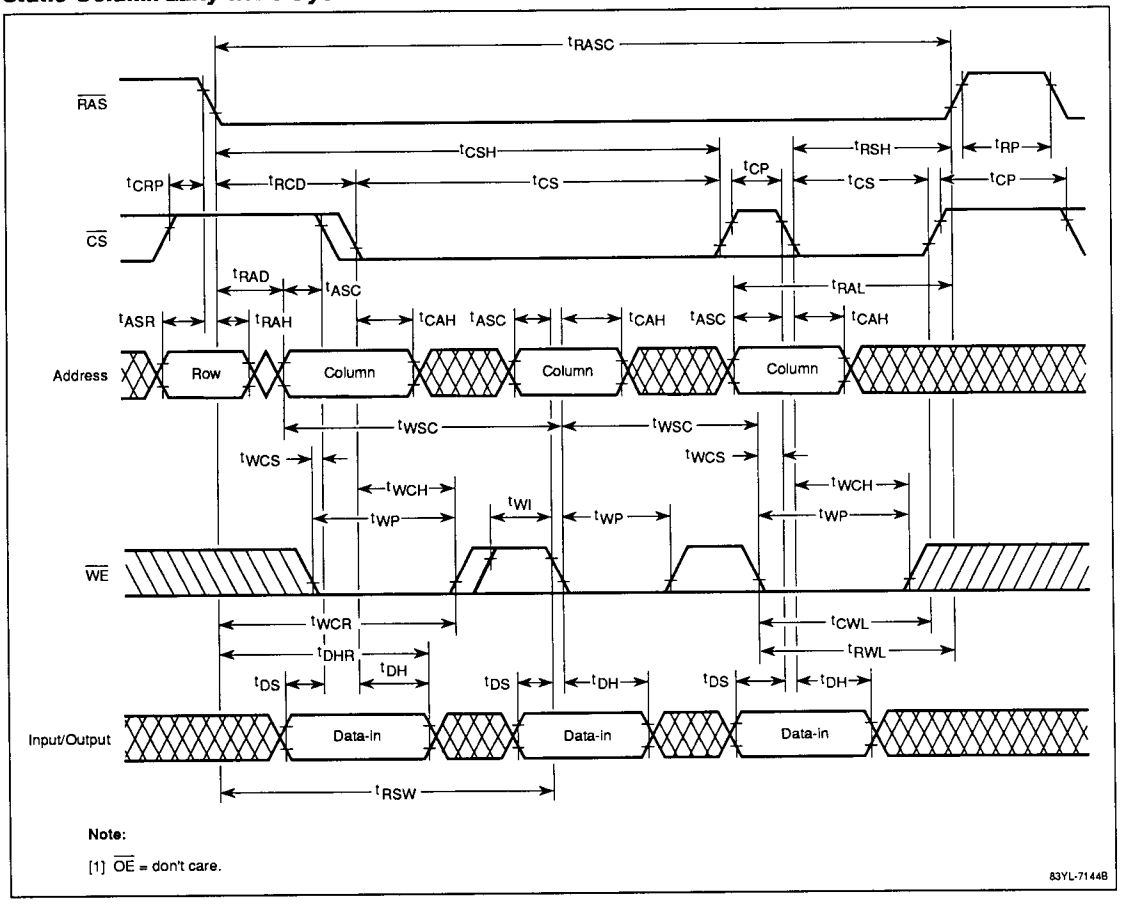
Timing Waveforms (cont)

Static-Column Early Write Cycle



Note:

[1] $\overline{OE}$ = don't care.

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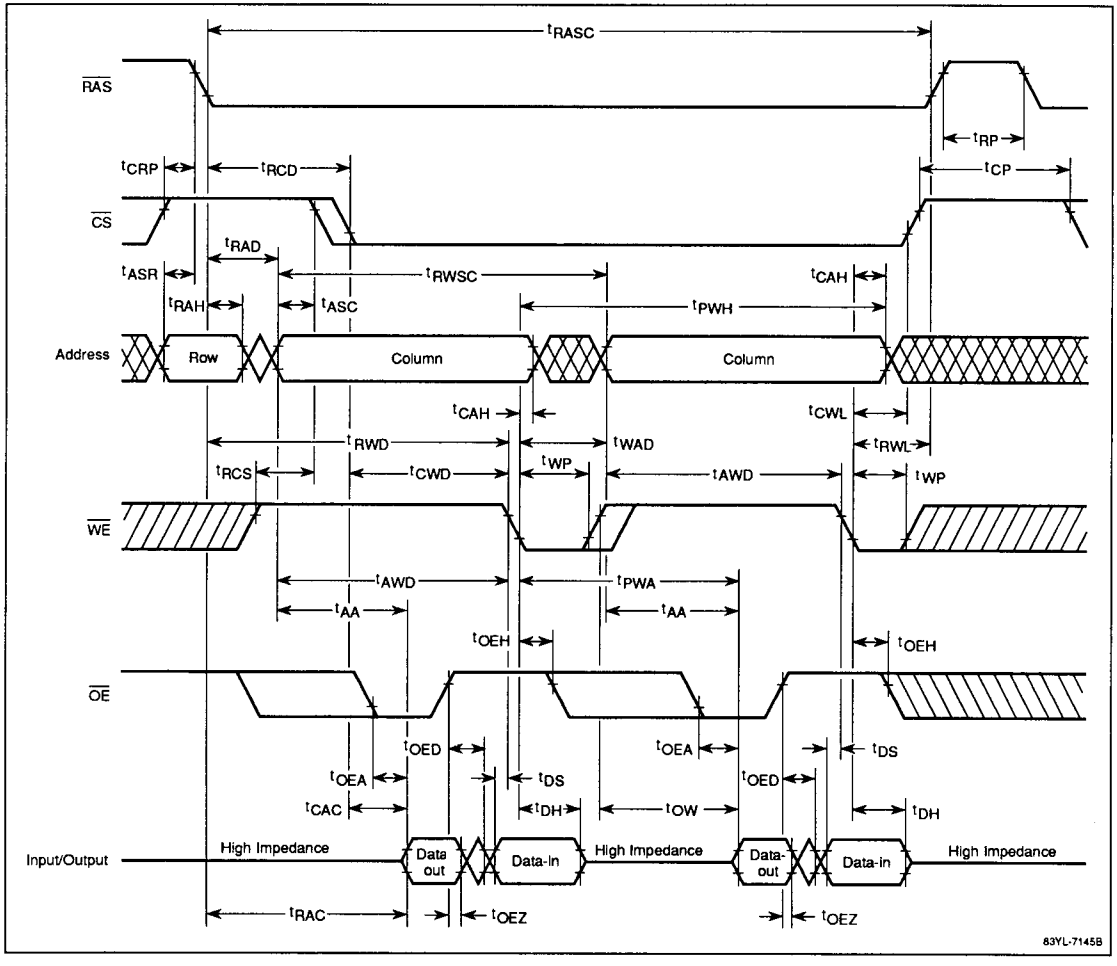
Timing Waveforms (cont)

Static-Column Read-Modify-Write Cycle



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