BAE SYSTEMS

238A790

32K x 8
Radiation Hardened Programmable Read Only Memory (PROM) – 3.3V

Product Description

Features

Radiation

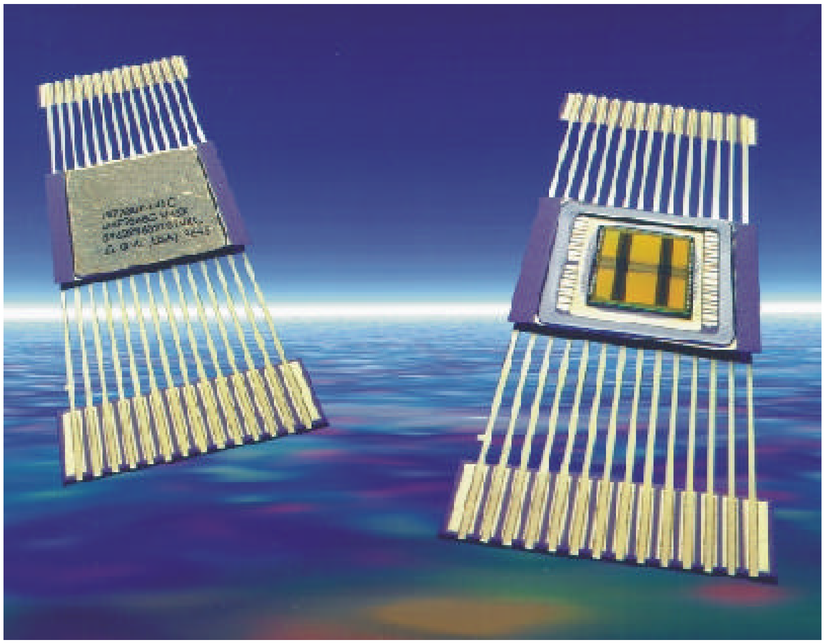
- Fabricated with Bulk CMOS 0.8 µm Process
- Total Dose Hardness through 2x10^5 rad(Si)
- Neutron Hardness through 1x10^{12} N/cm^2
- SEU Immune (No Latches)
- Latchup Free

Other

- Read/Write Cycle Times ≤100 ns (-55 °C to 125°C)
- SMD Number Pending
- Asynchronous Operation
- TTL Compatible I/O
- Single 3.3 V ±5% Power Supply
- Low Operating Power
- Packaging Options
  - 28-Lead Flat Pack (0.500” x 0.720”)

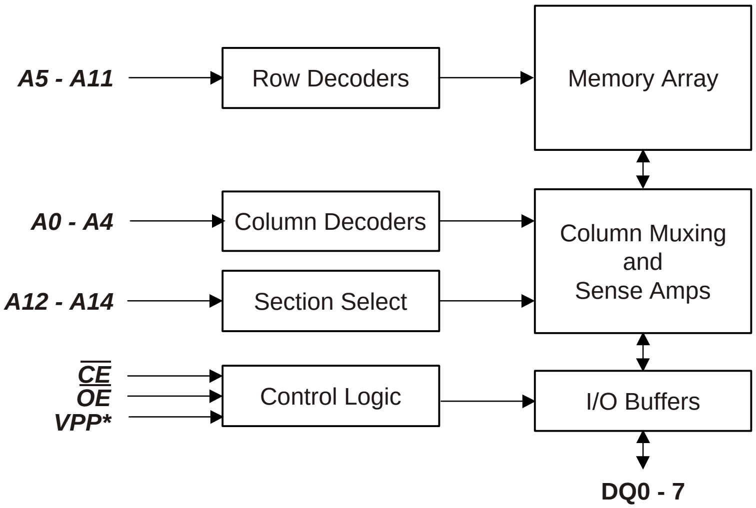
General Description

The 32K x 8 radiation hardened PROM is pinout, function and package compatible with commercial 28C256 series 32K x 8 EEPROMs, such as SEEQ 28C256 and Atmel AT28C256. The PROM is fabricated with BAE SYSTEMS’ QML-qualified radiation hardened technology, and is designed for use in systems operating in radiation environments. The radiation hardened Oxide-Nitride-Oxide (ONO) anti-fuse technology features 0.8 micron, 5 V transistors in the data path, and 1.0 micron, high voltage N and PFETs in the programming path circuitry. The PROM operates over the full military temperature range, requires a single 3.3 V ± 5% power supply, and is available with TTL compatible I/O. Power consumption is typically 15 mW/MHz in operation and is less than 10 mW/MHz in the low power disabled mode. The PROM operation is fully asynchronous, with an associated typical access time of 100 nanoseconds. Synchronous operation is also possible using CE as a clock.



BAE SYSTEMS’ enhanced bulk CMOS technology is radiation hardened through the use of advanced and proprietary design, layout, and process hardening techniques.

Functional Diagram



**PROM Programming Voltage*

Signal Definitions

A: 0-14 – Address input pins that select a particular eight-bit word within the memory array.

DQ: 0-7 – Bi-directional data pins that serve as data outputs during a read operation and as data inputs during a write operation.

$\overline{\text{OE}}$ – Negative output enable, when at a high level, holds the data output drivers in a high impedance state. In programming mode, with $\overline{\text{OE}}$ high and $\overline{\text{CE}}$ low, data driver state is in "Data-In" to enable programming.

$\overline{\text{CE}}$ – Chip enable, when at a low level with $\overline{\text{OE}}$ at low level, allows normal operation. When at a high level, $\overline{\text{CE}}$ forces the data output drivers in a high impedance state.

Truth Table

Mode	***Inputs$^{(1),(2)}$***				***Power $^{(3)}$***
	$\overline{\text{CE}}$	***$\overline{\text{OE}}$***	***VPP***	***I/O***	
Read	Low	Low	V_{DD}	Data-Out	Active
Tristate	Low	High	V_{DD}	High-Z	Active
Standby	V_{DD}	X	V_{DD}	High-Z	Standby1
Standby	High	X	V_{DD}	High-Z	Standby2
Program $^{(4)}$	Low	High	17V ± 0.5V	Data-In	Programming

Notes:

1) V_{IN} for don't care (X) inputs = V_{IL} or V_{IH}.
2) High: V_{IN} ³ 2.2 V for TTL inputs.
Low: V_{IN} £ 0.8 V for TTL inputs.
3) Minimum I_{DD} is drawn when standby mode is implemented with $\overline{\text{CE}}$ = V_{DD}(standby1 power).
4) Programming needs to be done using V_{DD} = 5V.

Absolute Maximum Ratings

Applied Conditions[1]	***Minimum***	***Maximum***
Storage Temperature Range (Ambient)	-65°C	+150°C
Operating Temperature Range	-55°C	+125°C
Positive Supply Voltage	-0.5 V	+7.0 V
Input Voltage(2)	-0.5 V	V_{DD}+ 0.5 V
Output Voltage(2)	-0.5 V	V_{DD}+ 0.5 V
Power Dissipation(3)		1.5 W
Lead Temperature (Soldering 5 sec)		+250°C
Electrostatic Discharge Sensitivity(4)	(Class I)	

Notes:

1) Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. All voltages are with reference to the module ground leads.

2) Maximum applied voltage shall not exceed +7.0 V.

3) Guaranteed by design; not tested.

4) Class as defined in MIL-STD-883, Method 3015.

Recommended Operating Conditions

Symbol	***Parameters***(1)	***Minimum***	***Maximum***	***Units***
V_{DD}	Supply Voltage	+3.14	+3.46	Volt
V_{PP}	Programming Voltage	V_{DD} (2)	V_{DD} (2)	Volt
GND	Supply Voltage Reference	0.0	0.0	Volt
T_C	Case Temperature	-55	+125	Celsius
V_{IL}	Input Logic “Low” - TTL	0.0	+0.8	Volt
V_{IH}	Input Logic “High” - TTL	+2.2	V_{DD}	Volt

Notes:

1) All voltages referenced to GND.
2) $V_{PP} = V_{DD}$ during non-programming mode.

Power Sequencing

Power shall be applied to the device only in the following sequences to prevent damage due to excessive currents:

- Power-Up Sequence: GND, V_{DD}, Inputs
- Power-Down Sequence: Inputs, V_{DD}, GND

DC Electrical Characteristics

Test	Symbol	Test Conditions[1]	Group A Subgroups	Device Type [2]	Limits		Units
					Minimum	Maximum	
Supply Current (Cycling Selected)	I_{DD1}	$F = F_{MAX} = 1/t_{AVAV(min)}$ CMOS Input No Output Load	1, 2, 3	All		150	mA
Supply Current (Standby)	I_{DD2}	$F = F_{MAX} = 1/t_{AVAV(min)}$ $\overline{CE} = V_{PP} = V_{IH} = V_{DD}$	1, 2, 3	All		2.0	mA
High Level Output Voltage	V_{OH}	I_{OH}= -2 mA I_{OH} = -200 µA	1, 2, 3	All	2.4 V_{DD} - 0.1 V		V
Low Level Output Voltage	V_{OL}	I_{OL}= 4 mA I_{OL} = 200 µA	1, 2, 3	All		0.4 0.1	V
High Level Input Voltage TTL Inputs	V_{IH}		1, 2, 3	All	2.2		V
Low Level Input Voltage TTL Inputs	V_{IL}		1, 2, 3	All		0.8	V
Input Leakage	I_{ILK}	$0\ V \le V_{IN} \le 5.5\ V$	1, 2, 3	All	-5	5	µA
Output Leakage	I_{OLK}	$0\ V \le V_{OUT} \le 5.5\ V$	1, 2, 3	All	-10	10	µA
C_{in}			4	All		7	pF
C_{out}			4	All		10	pF

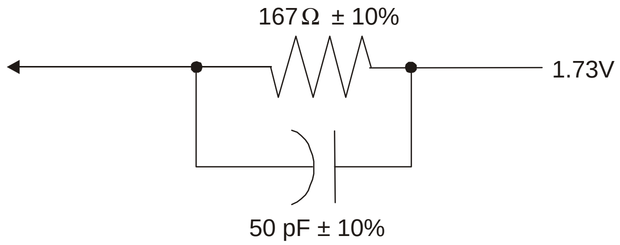
Note:

1) *-55 °C £ T_{case} £ +125°C; 3.14 V £ V_{DD} £ 3.46 V; unless otherwise specified. Test conditions for AC measurements:*

2) *Measured during initial device characterization.*

• *Input Levels*	*0 V to V_{DD}*
• *Input Rise and Fall Time*	*£ 2.0 ns/Volt*
• *Input and Output Timing Reference Levels (Except for Tristate Parameters)*	*1.5 V*
• *Input and Output Timing Reference Levels or Tristate Parameters*	*V_{OL} = 1.23 V; V_{OH} = 2.23 V*
• *Programmed Array Mix of '1's and '0's*	*50%*
• *Output Load*	*See Output Load Circuit Diagram*
• *Read Cycle*	*See Read Cycle Timing*

Output Load Circuit



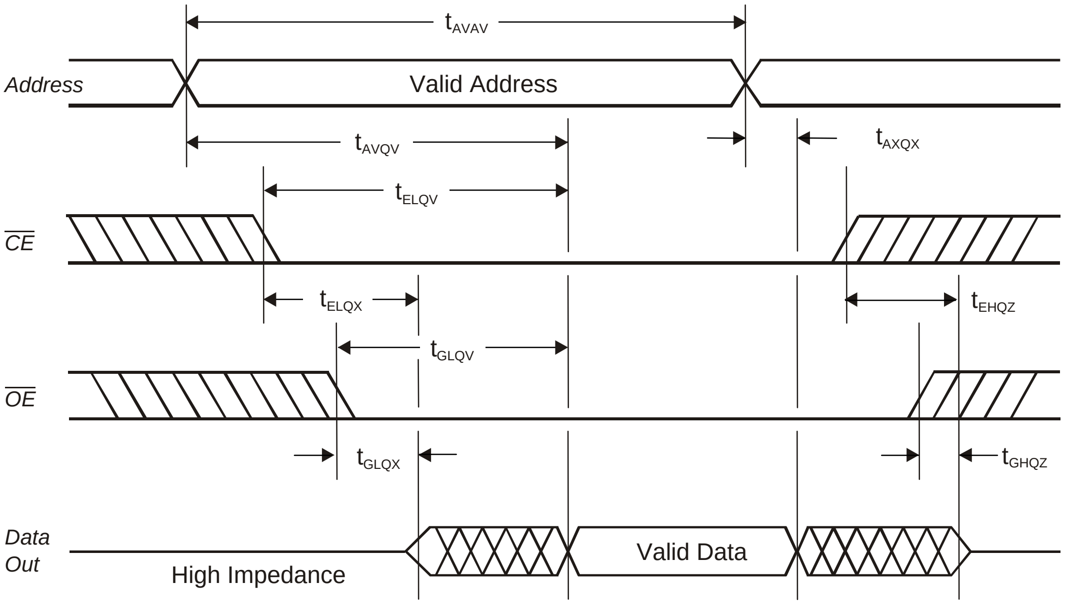
Read Cycle AC Timing Characteristics (1)

Test	Symbol	Device Type	Limits		Units
			Minimum	Maximum	
Read Cycle Time	t_{AVAV}	ALL	100		ns
Address Access Time	t_{AVQV}	ALL		100	ns
Chip Enable Access Time	t_{ELQV}	ALL		100	ns
Output Enable Access Time	t_{GLQV}	ALL		100	ns
Chip Enable to Output Active	t_{ELQX}		0		ns
Output Enable to Output Active	t_{GLQX}		0		ns
Output Hold After Address Change	t_{AXQX}		0		ns
Chip Enable to Output Disable	t_{EHQZ}			15	ns
Output Enable to Output Disable	t_{GHQZ}			15	ns

Note:

1) -55°C £ T_{case} £ +125°C; 3.14 V £ V_{DD} £ 3.46 V; unless otherwise specified.

Read Cycle Timing Diagram



Dynamic Electrical Characteristics

Read Cycle

The PROM is asynchronous in operation, allowing the read cycle to be controlled by address or chip enable ($\overline{\text{CE}}$) (refer to Read Cycle Timing diagram). To perform a valid read operation, both chip enable ($\overline{\text{CE}}$) and output enable ($\overline{\text{OE}}$) must be low. The output drivers can be controlled independently by the $\overline{\text{OE}}$ signal. Consecutive read cycles can be executed with $\overline{\text{CE}}$ held continuously low, and with $\overline{\text{OE}}$ held continuously low, and toggling the addresses.

For an address-activated read cycle, $\overline{\text{CE}}$ and $\overline{\text{OE}}$ must be valid prior to or coincident with the activating address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid t_{AVQV} time following the latest occurring address edge transition. The minimum address activated read cycle time is t_{AVAV}. When the PROM is operated at the minimum address-activated read cycle time, the data outputs will remain valid on the PROM I/O until t_{AXQX} time following the next sequential address transition.

To control a read cycle with $\overline{\text{CE}}$, all addresses and $\overline{\text{OE}}$ must be valid prior to or coincident with the enabling $\overline{\text{CE}}$ edge transition. Address or $\overline{\text{OE}}$ edge transitions can occur later than the specified setup times to $\overline{\text{CE}}$, however, the valid data access time will be delayed. Any address edge transition that occurs during the time when $\overline{\text{CE}}$ is low will initiate a new read access, and data outputs will not become valid until t_{AVQV} time following the address edge transition. Data outputs will enter a high impedance state t_{EHQZ} time following a disabling $\overline{\text{CE}}$ edge transition.

To control a read cycle with $\overline{\text{OE}}$, all addresses and $\overline{\text{CE}}$ must be valid prior to or coincident with the enabling $\overline{\text{OE}}$ edge transition. Address or $\overline{\text{CE}}$ edge transitions can occur later than the specified setup times to $\overline{\text{OE}}$; however, the valid data access time will be delayed. Any address edge transition that occurs during the time when $\overline{\text{OE}}$ is high will initiate a new read access, and data outputs will not become valid until t_{AVQV} time following the address edge transition. Data outputs will enter a high impedance state t_{GHQZ} time following a disabling $\overline{\text{OE}}$ edge transition.

Radiation Characteristics

Total Ionizing Radiation Dose

The PROM will meet all stated functional and electrical specifications over the entire operating temperature range after a total ionizing radiation dose of 5 x10^5 rad(Si). All electrical and timing performance parameters will remain within specifications after rebound at V_{DD} = 3.3 V and T = 125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and PROM product using 10 keV X-ray and Co60 radiation sources. Transistor gate threshold shift correlations have been made between 10 keV X-rays applied at a dose rate of 1x10^5 rad(Si)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Single Event Effects

The PROM has demonstrated no data upset when exposed to ion LETs ≤120 MeV/mg/cm^2. Given that the design uses an anti-fuse for data storage and programmability, Single Event Device Rupture (SEDR) testing was also performed. No SEDR was detected to an effective LET of 60 MeV/mg/cm^2.

Latchup

The PROM will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions.

Radiation Hardness Ratings (1),(2), (3)

Symbol	Characteristics	Conditions	Minimum	Maximum	Units
RTD	Total Dose	V_{DD} =3.3V during irradiation, static bias	500K		rad(Si)
SEL	Single Event Latchup	-55°C ≤ T_{case} ≤ 125°C V_{DD} =5.5 V		Immune	Fails/Device-Day
SEDR (4)	Single Event Dielectric Rupture (anti-fuse)	-55°C ≤ T_{case} ≤ 125°C V_{DD} =5.5 V		0	Upsets/Fuse-Day
SEU	Single Event Upset	-55°C ≤ T_{case} ≤ 125°C V_{DD} =4.5 V		0	Upsets/Bit-Day

Notes:

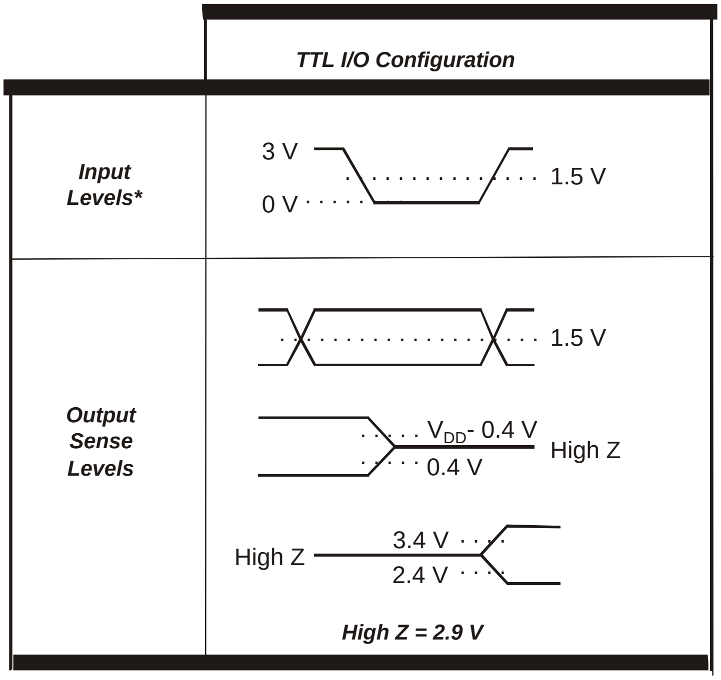
1) Measured at room temperature unless otherwise stated. Verification test per TRB approved test plan.

2) Device electrical characteristics are guaranteed for post irradiation levels at 25°C, per MIL-STD-883, Test Method 1019.5, Condition A.

3) There are no storage elements on this device.

4) Tested with ions having perpendicular incidence at LET of 60 MeV/mg/cm^2, 90% worst case particle environment, geosynchronous orbit, 0.025” of aluminum shielding. Testing performed according to ASTM Standard F1192.

Tester AC Timing Characteristics



**Input rise and fall times <5 ns*

Radiation Hardness Assurance

BAE SYSTEMS provides a superior quality level of radiation hardness assurance for our products. The excellent product quality is sustained via the use of our qualified QML operation which requires process control with statistical process control, radiation hardness assurance procedures and a rigid computer controlled manufacturing operation monitoring and tracking system.

The BAE SYSTEMS technology is built with resistance to radiation effects. Our product is designed to exhibit < $1e^{-11}$ fails/bit-day in a 90% worst case geosynchronous orbit under worst case operating conditions. Total dose hardness is assured by irradiating test structures on every lot and total dose exposure with Cobalt 60 testing performed quarterly on TCI lots to assure the product is meeting the QML radiation hardness requirements.

Screening Levels

BAE SYSTEMS has two QML screen levels (Q and V) to meet full compliant space applications. For limited performance and evaluation situations, BAE SYSTEMS offers an engineering screen level.

Reliability

BAE SYSTEMS’ reliability starts with an overall product assurance system that utilizes a quality system involving all employees including operators, process engineers and product assurance personnel. An extensive wafer lot acceptance methodology, using in-line electrical data as well as physical data, assures product quality prior to assembly. A continuous reliability monitoring program evaluates every lot at the wafer level, utilizing test structures as well as product testing. Test structures are placed on every wafer, allowing correlation and checks within-wafer, wafer-to-wafer, and from lot-to-lot.

Reliability attributes of the CMOS process are characterized by testing both irradiated and non-irradiated test structures. The evaluations allow design model and process changes to be incorporated for specific failure mechanisms, i.e., hot carriers, electromigration, and time dependent dielectric breakdown. These enhancements to the operation create a more reliable product.

The process reliability is further enhanced by accelerated dynamic life tests of both irradiated and non-irradiated test structures. Screening and testing procedures from the customer are followed to qualify the product.

A final periodic verification of the quality and reliability of the product is validated by a TCI (Technology Conformance Inspection).

Standard Screening Procedure

Flow	***QML Level***		***Comments***
	Q	***V***	
Wafer Lot Acceptance	X	X	Alternate Method Used
Serialization	X	X	Die Traceability
Destructive Bond Pull	Sample	Sample	
Internal Visual	X	X	MIL-STD-883, TM 2010
Temperature Cycle	X	X	
Constant Acceleration	X	X	
PIND	X	X	
Radiography		X	
Electrical Test	X	X	
Blank Array Dynamic Burn-In	X	X	
Electrical Test	X	X	
Test Row Dynamic Burn-In	X	X	
Final Electrical	X	X	Meets Group A
PDA	X	X	< 5% Fallout
Fine and Gross Leak	X	X	
External Visual	X	X	MIL-STD-883, TM 2009

Fuse Stress Methodology

There are two main areas of fuse-related failure concerns in programmable devices. The first area of concern is unprogrammed fuses becoming mistakenly programmed over time. The second concern is programmed fuses becoming unprogrammed.

With the ONO anti-fuse technology, it has been shown that the programmed anti-fuse actually becomes more reliable over time – that the repeated flow of current strengthens the programmed electrical connection and that the anti-fuse lifetime is greater than other forms of standard CMOS electromigration failure mechanisms.

In addition to the normal burn-in cycles, an electrical stress methodology has been implemented that allows screening at wafer test for unprogrammed anti-fuse infant mortality failures and weaker anti-fuses that could diminish programming yield. This is accomplished by applying a higher than normal voltage across all unprogrammed anti-fuses.

Specifically, there are two levels of high voltage (9V) stresses applied to unprogrammed anti-fuses at wafer test prior to burn-in, and a third cycle of unprogrammed fuse stress applied during the final programmer box personalization. Parts that fail any of these tests are rejected. After personalization, the PROM is operated at 3.14 - 3.46 V, and will not experience subsequent stressing, and does not require additional post-programmed electrical or temperature stressing. Because anti-fuse infant mortality failures can be detected and effectively screened, the PROM has as high a level of reliability as standard CMOS processed products. Additional justification for not performing post-programming burn-in will be provided on request.

Burn-In Methodology

There are two methods of burn-in defined: Blank Array Wordline burn-in and Test Row “Raster” Bitline burn-in.

The Blank Array Wordline burn-in is designed to exercise the array cells in a sequence which will activate any latent defects in the array area. This sequence also creates alternate biasing of adjacent lines to detect defects in the wiring levels of the chip.

The Test Row “Raster” Bitline burn-in is designed to exercise the device through a series of logic level shifts which simulate the active mode of operation of the device, i.e., exercises decode, sense amps, datapath, and peripheral circuitry. This mode is used to detect defects at the device level of the chip. Through the use of these two burn-in modes, the chip is subjected to an equivalent Q/V level burn-in.

All I/O pins specified in the burn-in pin lists are driven through individual series resistors (1.6KΩ ± 10%). Burn-in voltages are defined using the following notation:

Voltage Levels

- V1: +5.5V (-0% /+10%)
  - V_{DD} pin is tied to this level.
- Vin(0): 0.0 V to +0.4 V
  - Low level for all programmed signals.
- Vin(1): +5.5 V (-0% /+10%)
  - High level for all programmed signals.
- GND Pins:
  - All module GND pins shall be tied to ground.

Blank Array Wordline Burn-In Pin Listing (1)

		Input	**Signal**
Input	**Signal**	A9	F/16
A0	F	A10	F/32
A1	F/2	A11	F/64
A2	F/4	A12	F/128
A3	F/8	A13	F/256
A4	F/16	A14	F/512
A5	F	DQ0-7	F/1024
A6	F/2	$\overline{\text{CE}}$	Low
A7	F/4	$\overline{\text{OE}}$	Low
A8	F/8	V_{PP}	V_{DD}

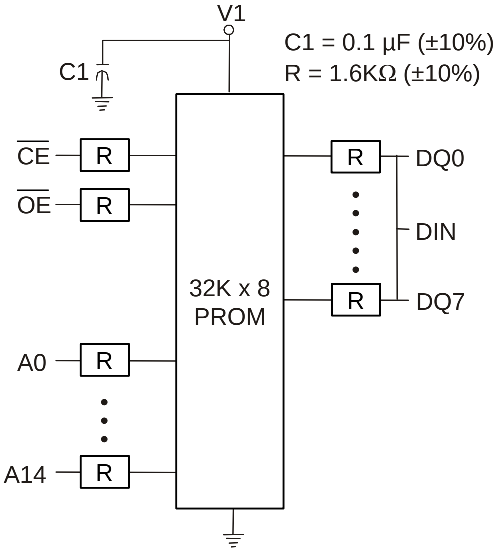
Test Row “Raster” Burn-In Pin Listing (1)

		Input	**Signal**
Input	**Signal**	A9	High
A0	F/2	A10	High
A1	F/4	A11	High
A2	F/8	A12	F/64
A3	F/16	A13	F/128
A4	F/32	A14	F/256
A5	F	DQ0-7	F/512
A6	High	$\overline{\text{CE}}$	Low
A7	High	$\overline{\text{OE}}$	Low
A8	High	V_{PP}	GND

Note:

1) F = square wave, 100 KHz to 1.0 MHz.

Burn-In Circuit



Device Programming

PROM programming is accomplished using the Unisite™ Universal Programmer made by Data I/O corporation. Unisite is a tool for programming device technologies and packaging. The Data I/O family of universal programs and corresponding software releases and updates are available direct from Data I/O Corporation (800) 3-DATAIO, Technical Support). A PPI adapter #1007 must also be purchased from Data I/O to interface the PROM flatpack to the Data I/O Programmer Box Unit. The PROM device ID number and programming algorithm information is contained in an internal silicon signature which is read by the programmer box and is transparent to the user.

Minimum System Requirements for Device Programming

Hardware	***Definition***	***Function***
Unisite	Data I/O Programmer Box	Program the PROMs
PPI Adapter #1007	Adapter Card for the BAE SYSTEMS 32K x 8 PROM	Interface with the Unisite Programmer
Host or PC	***Host*** • A Minicomputer, i.e., Sun, DEC or Apollo Workstation ***PC*** • A DOS-Based Personal Computer i.e., IBM PC or Compatible	Control the Programmer and Remote Storage of Data Files
Terminal	A Stand-Alone Terminal, i.e., DEC VT 200, Qume VT-101, and the Wyse WY-30/40/70 Family of Terminals	Programming

Programming Hints

The PROM array is built with all “1’s” and an anti-fuse technology is implemented to program “0’s.” All unused locations should remain unprogrammed as “1’s” to save programming time and allow for additional program locations.

Post Programming Hints

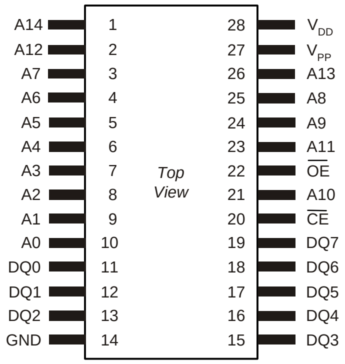
The Data I/O Programmer uses slow I/O timings to both program and verify programming of PROM devices. After programming, it is recommended that users test devices at speed over application temperature range to ensure that programmed devices meet the application requirements.
If the device fails the at-speed testing, the user is advised to program the device one additional time and then perform the at-speed testing.

Packaging

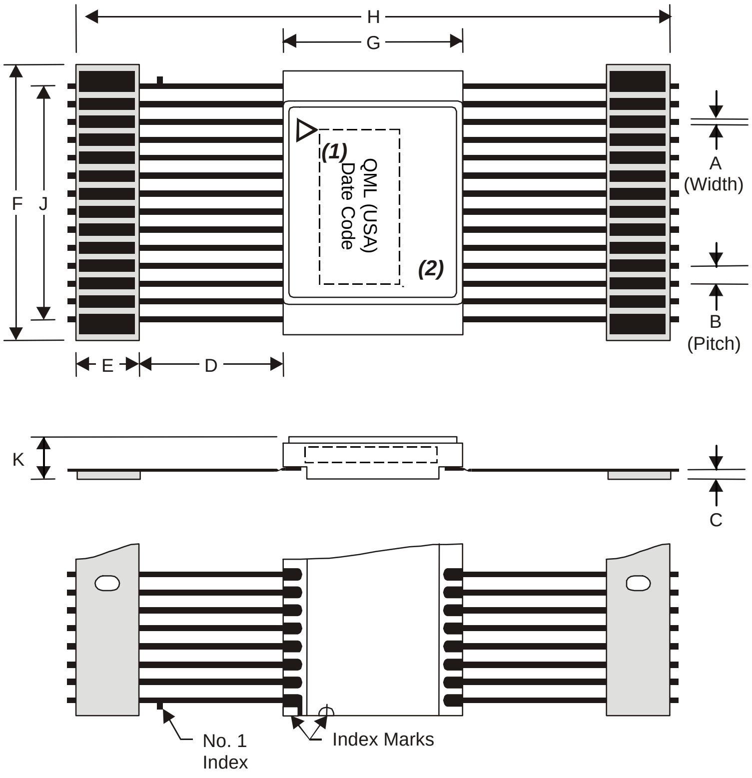
The 32K x 8 PROM is offered in a custom 28-lead FP. The package is constructed of multilayer ceramic (Al_2O_3) and feature internal power and ground planes. It also features a non-conductive ceramic tie bar on the lead frame. The purpose of the tie bar is to allow electrical testing of the device, while preserving the lead integrity during shipping and handling, up to the point of lead forming and insertion.

Optional capacitors can be mounted to the package to maximize supply noise decoupling and increase board packing density. These capacitors attach directly to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package, both of which are critical in a transient radiation environment. All NC pins must be connected to either V_{DD}, GND or an active driver to prevent charge build up in the radiation environment. (NC = no connect.)

28-Lead Flat Pack Pinout



28-Lead Flat Pack



A=.017 ± .002	F=.760 ± .008
B=.050 ± .003	G=.500 ± .008
C=.035 ± .014	H=1.650
D=.400 ± .020	J=.650
E=.175 ± .010	K=.109

Notes:

1) Part mark per device specification.

2) "QML" may not be required per device specification.

3) Dimensions are in inches.

4) Lead width: .008 ± .002.

5) Lead height: .006 ± .002.

6) Unless otherwise specified, all tolerances are ± .005".

BAE SYSTEMS

Ordering Information

32K x 8 PROM Memory Device
•Part Number 238A790 - ***W*** **X** ***Y*** **Z**

W ***Package Type***	***X*** ***Speed Designation***	***Screen Designation***	**Z** **Input Type**
1 = 28 Lead Flat Pack	1= 100 ns	1= QML VV 3 = Engineering 4 = QML VQ 5 = QML QQ 7 = Customer Specific	T = TTL

BAE SYSTEMS
An ISO 9001, AS9000, ISO 14001,
and SEI CMM Level 4 Company
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http://www.iews.na.baesystems.com/space/

0040_32K_8_PROM.ppt