----Feature----

- **2 Bank x 256k word x 32 bit**
- **Same interface as Synchronous DRAMs**
  Programmable CAS latency [2,3], programmable burst length [1,2,4,8,FP],
  burst type[S,I], Auto refresh, Self refresh, Auto precharge, DQM(0-3) byte masking
- **Graphic function :**
  8 col x32 bit Block Write (Mask able, with Color register)
  Write Per Bit (with Mask register)
- **Speed item : -7ns , -8ns, -10ns (cycle time)**
- **LVTTL interface (SSTL under consideration(option)**
- **Package : 100 pin thin QFP (20mm x14mm, 0.65 lead pitch)**
- **2,048 refresh cycle / 32ms**
- **CS/MP: Now**

REV

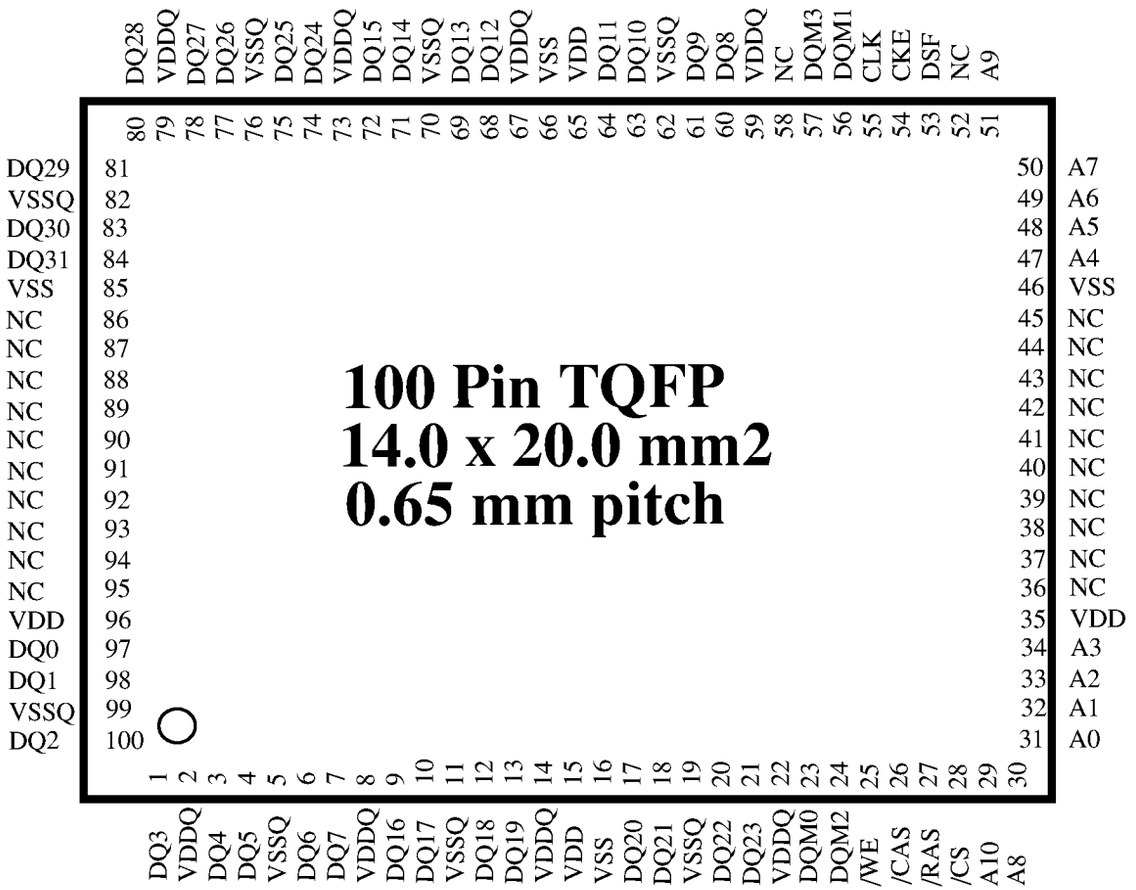
These values are preliminary data and subject to change.

Electrical Parameter Table

Speed Item		LVTTL		
		-7	-8	-10
RAS High time	tRP	20	24	30
RAS to CAS delay	tRCD	20	24	30
RAS Low time	tRAS	48	48	50
CAS Latency of 3	tCLK	7	8	10
	tAC	6	6	7
	tCAC*	20	22	27
	tRAC*	40	46	57
CAS Latency of 2	tCLK	10	12	13
	tAC	8	9	10
	tCAC*	18	21	23
	tRAC*	38	45	53

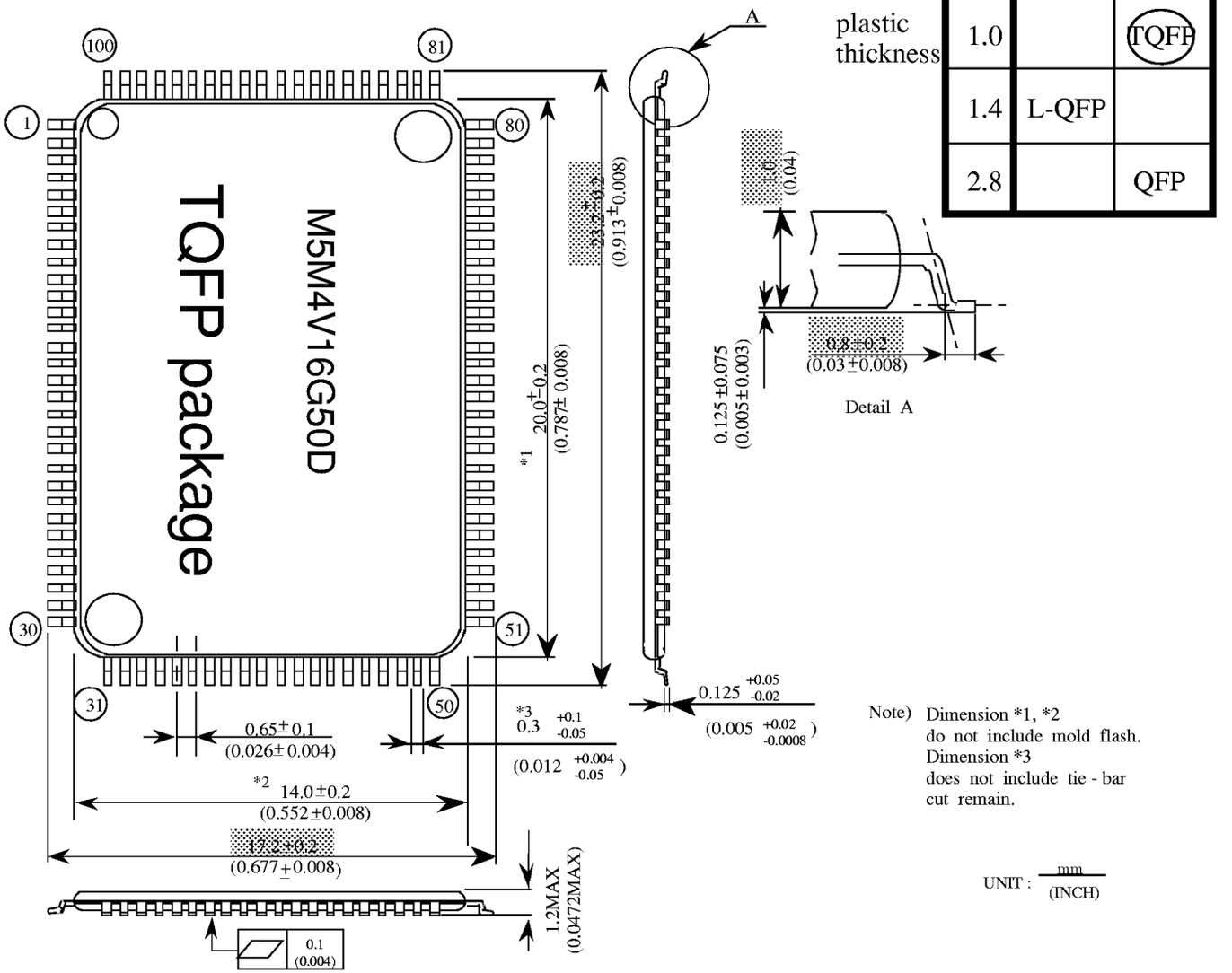
* tCAC=tCLKx(CL-1)+tAC, tRAC=tRCD+tCAC, under the same clock period.
* Vcc=3.1V~3.6V for -7 speed

16MSGRAM M5M4V16G50DFP



16MSGRAM (X32)
M5M4V16G50D

100PFD-B
(1.0mm)



Lead length

plastic thickness	1.0	1.6
1.0		TQFP
1.4	L-QFP	
2.8		QFP

Note) Dimension *1, *2
do not include mold flash.
Dimension *3
does not include tie - bar
cut remain.

UNIT : mm / (INCH)

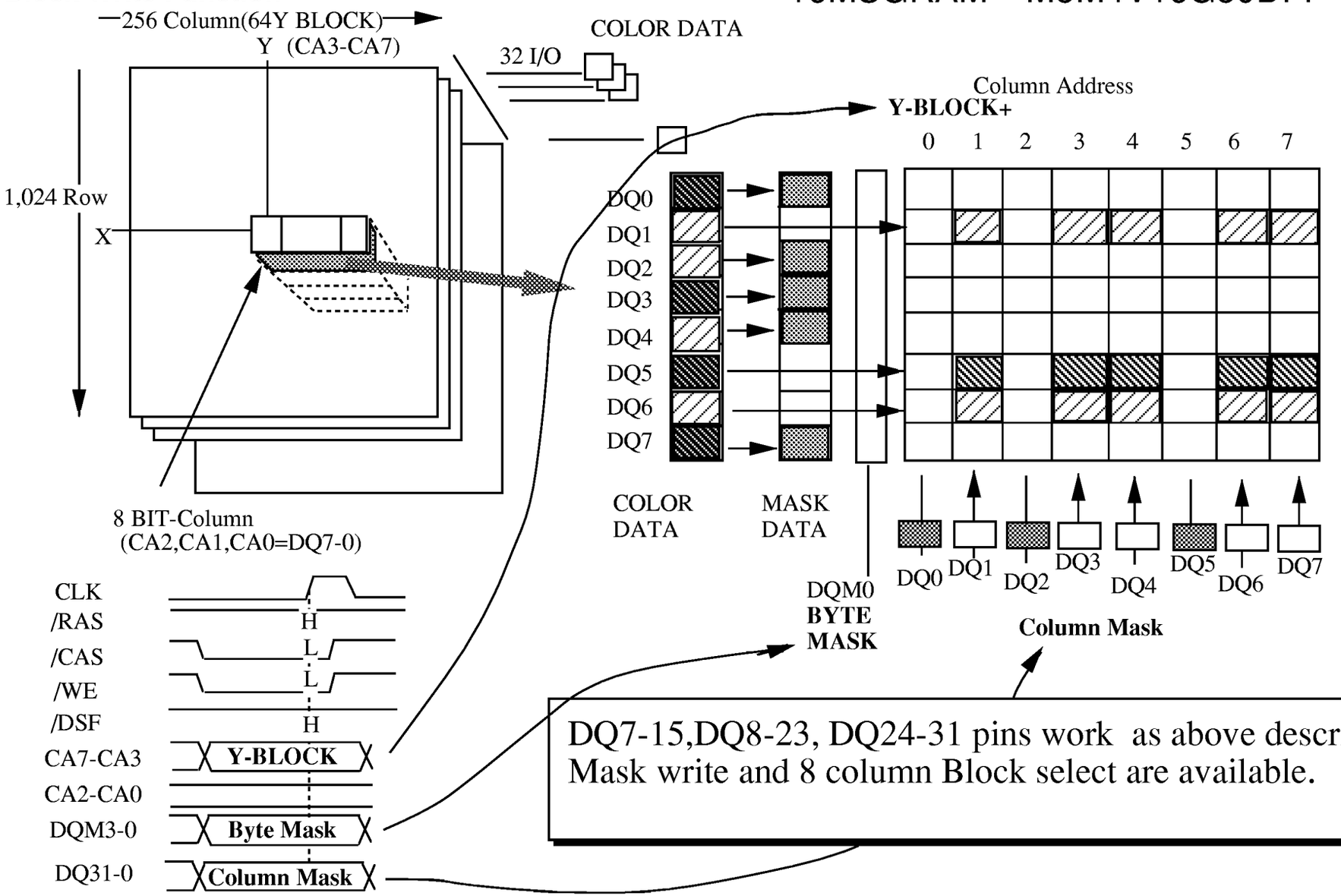
Truth Table 16MSGRAM M5M4V16G50DFP

Mnemonic	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	DSF	Bank A10	AP A9	A8-3	A2-0	DQ	Register			command
													Write Mask	Color	Mode	
DESEL	H	X	H	X	X	X	X	X	X	X	X	---	---	---	---	Deselect
NOP	H	X	L	H	H	H	L	X	X	X	X	---	---	---	---	No Operation
ACT	H	X	L	L	H	H	L	BA	Row	Add	Add	---	---	---	---	Row Address Entry & Bank Activate
ACTWPB	H	X	L	L	H	H	H	BA	Row	Add	Add	---	set	---	---	Row Address Entry & Bank Activate
PRE	H	X	L	L	H	L	L	BA	L	X	X	---	reset	---	---	Single Bank Precharge
PREA	H	X	L	L	H	L	L	X	H	X	X	---	reset	---	---	Precharge All Banks
WRITE	H	X	L	H	L	L	L	BA	L	Col	Col	Din	(use)	---	use	Column Address Entry & Write
WRITEA	H	X	L	H	L	L	L	BA	H	Col	Col	Din	(use)	---	use	Column Address Entry & Write with Auto-Precharge
BW	H	X	L	H	L	L	H	BA	L	Col	---	Select	use	use	use	Column Address Entry & Masked Block Write
BWA	H	X	L	H	L	L	H	BA	H	Col	---	Select	use	use	use	Masked Block Write with Auto-Precharge
READ	H	X	L	H	L	H	L	BA	L	Col	Col	Dout	---	---	use	Column Address Entry & Read
READA	H	X	L	H	L	H	L	BA	H	Col	Col	Dout	---	---	use	Column Address Entry & Read with Auto-Precharge
REFA	H	H	L	L	L	H	L	X	X	X	X	---	---	---	---	Auto-Refresh
REFS	H	L	L	L	L	H	L	X	X	X	X	---	---	---	---	Self-Refresh Entry
REFSX	L	H	H L	X H	X H	X H	X L	X	X	X	X	---	---	---	---	Self-Refresh Exit
TERM	H	X	L	H	H	L	L	X	X	X	X	---	---	---	---	Burst Terminate
MRS	H	X	L	L	L	L	L	OP-CODE				---	---	---	Load	Mode Register Set
SRS	H	X	L	L	L	L	H	OP-CODE				Color / Mask	Load	Load	---	Special Register Set

MITSUBISHI ELECTRIC

Block Write Function

16MSGRAM M5M4V16G50DFP



DQ7-15,DQ8-23, DQ24-31 pins work as above described.
Mask write and 8 column Block select are available.