TOSHIBA MOS INTEGRATED CIRCUIT

TC5316200 CP / CF / CFT (Seiko Instruments Inc)

SILICON GATE CMOS

16 MBIT (1 M WORD BY 16 BITS/2 M WORD BY 8 BITS) CMOS MASK ROM

DESCRIPTION

The TC5316200CP/CF/CFT is a 16,777,216-bit Read Only Memory organized as 1,048,576 words by 16 bits when $\overline{BYTE}$ is logical high, and as 2,097,152 words by 8 bits when $\overline{BYTE}$ is logical low.

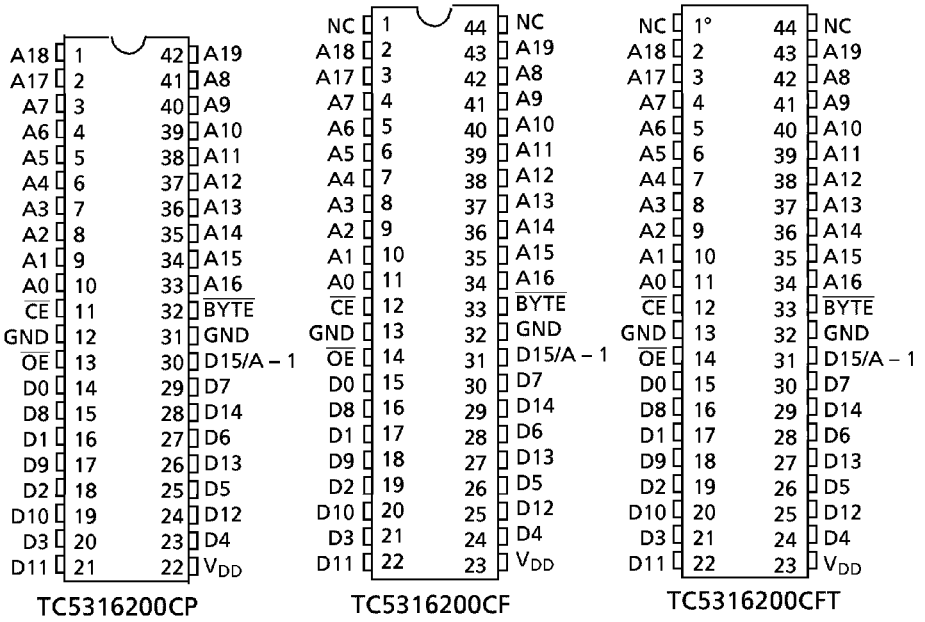
The TC5316200CP/CF/CFT is most suitable for application such as program memory, data memory, and character generators.

The TC5316200CP/CF/CFT is packaged in a standard 600 mil 42-pin DIP, or 600 mil 44-pin SOP or 400 mil 44-pin TSOP Type Ⅱ.

FEATURES

- Single 5 V Power Supply
- Access Time: 120 ns (max)
- Power Dissipation
  - Operating Current: 80 mA (max)
  - Standby Current : 100 μA (max)
- Fully Static Operation
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- TC5316200CP : DIP42−P−600
- TC5316200CF : SOP44−P−600
- TC5316200CFT: TSOP44−P−400

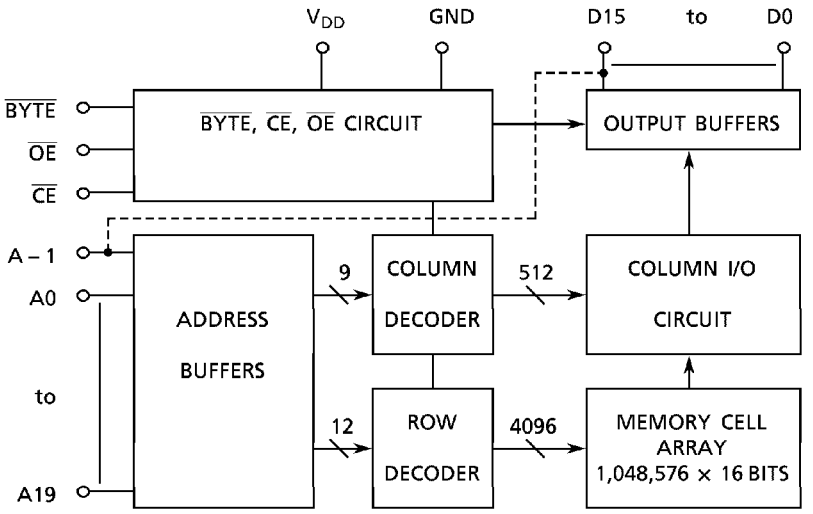
PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

A0 to A19	Address Inputs
D0 to D14	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15/A−1	Data Output/Addrss Input
$\overline{BYTE}$	Word, Byte Selection Input
V_{DD}	Power Supply
GND	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	D0 to D7	D8 to D14	D15/A – 1	POWER
Read (16-Bit)	L	L	H	Data Out			Active
Read (8-Bit)	L	L	L	Data Out (Lower 8 bits)	High Impedance	L	Active
Read (8-Bit)	L	L	L	Data Out (Upper 8 bits)	High Impedance	H	Active
Output Deselect	L	H	*	High Impedance			Active
Standby	H	*	*	High Impedance			Standby

H: V_{IH} L: V_{IL} *: V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	– 0.5 to 7.0	V
V_{IN}	Input Voltage	– 0.5 to V_{DD}	V
V_{OUT}	Output Voltage	0 to V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	– 55 to 150	°C
T_{OPR}	Operating Temperature	0 to 70	°C
T_{SOLDER}	Soldering Temperature (10 s)	260	°C

* SOP/TSOP

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	− 0.3	–	0.8	V

DC CHARACTERISTICS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 to V_{DD}	–	± 5.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to V_{DD}	–	± 5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4 V	− 1.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V	2.0	–	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	–	2	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2 V	–	100	μA
I_{DDO1}	Operating Current	V_{IN} = V_{IH}/V_{IL}, t_{cycle} = 120 ns I_{OUT} = 0 mA	–	90	mA
I_{DDO1}		V_{IN} = V_{IH}/V_{IL}, t_{cycle} = 150 ns I_{OUT} = 0 mA	–	80	mA
I_{DDO2}		V_{IN} = V_{DD} − 0.2 V/0.2 V t_{cycle} = 120 ns, I_{OUT} = 0 mA	–	80	mA
I_{DDO2}		V_{IN} = V_{DD} − 0.2 V/0.2 V t_{cycle} = 150 ns, I_{OUT} = 0 mA	–	70	mA

CAPACITANCE (f = 1 MHz, Ta = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0 V	–	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	–	12	pF

Note: This parameter is periodically sampled and is not tested for every component.

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = 0° to 70°C, V_{DD} = 5 V ± 10%)

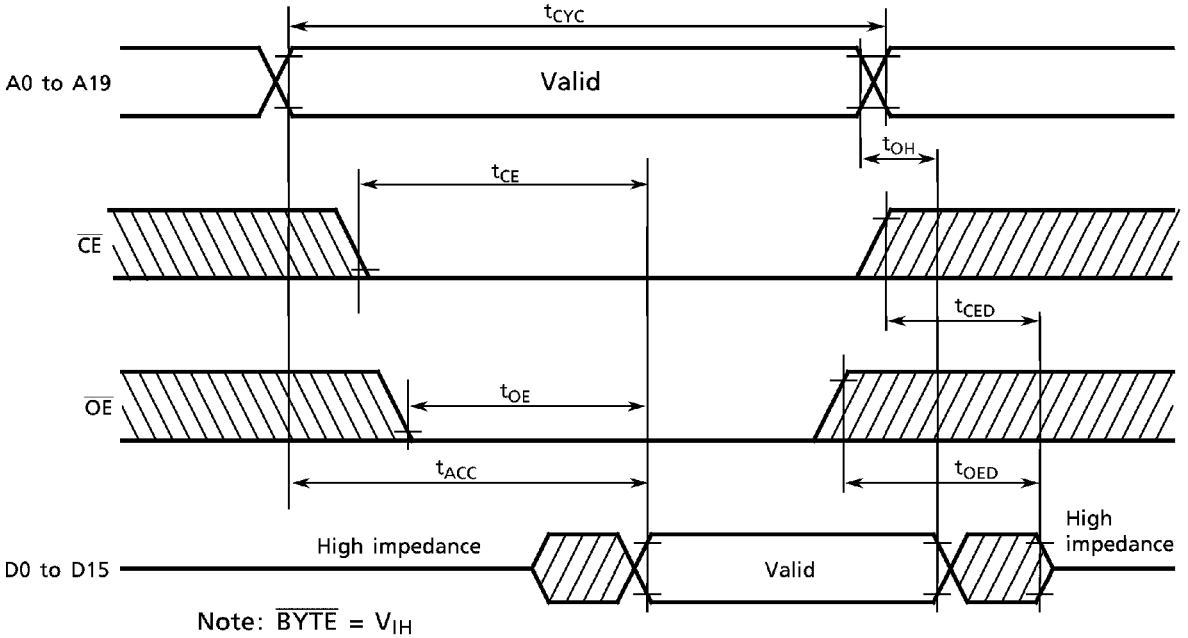
SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CYC}	Cycle Time	120	–	ns
t_{ACC}	Address Access Time	–	120	ns
t_{CE}	Chip Enable Access Time	–	120	ns
t_{BT}	$\overline{BYTE}$ Access Time	–	120	ns
t_{OE}	Output Enable Access Time	–	60	ns
t_{CED}	Output Disable Time from $\overline{CE}$	–	45	ns
t_{OED}	Output Disable Time from $\overline{OE}$	–	45	ns
t_{BTD}	Output Disable Time from $\overline{BYTE}$	–	45	ns
t_{OH}	Output Hold Time	5	–	ns

AC TEST CONDITIONS

Output Load		: 100 pF + 1 TTL
Input Levels		: 0.6 V, 2.4 V
Timing Measurement Reference Levels	Input	: 0.8 V, 2.2 V
	Output	: 0.8 V, 2.0 V
Input Rise and Fall Time		: 5 ns

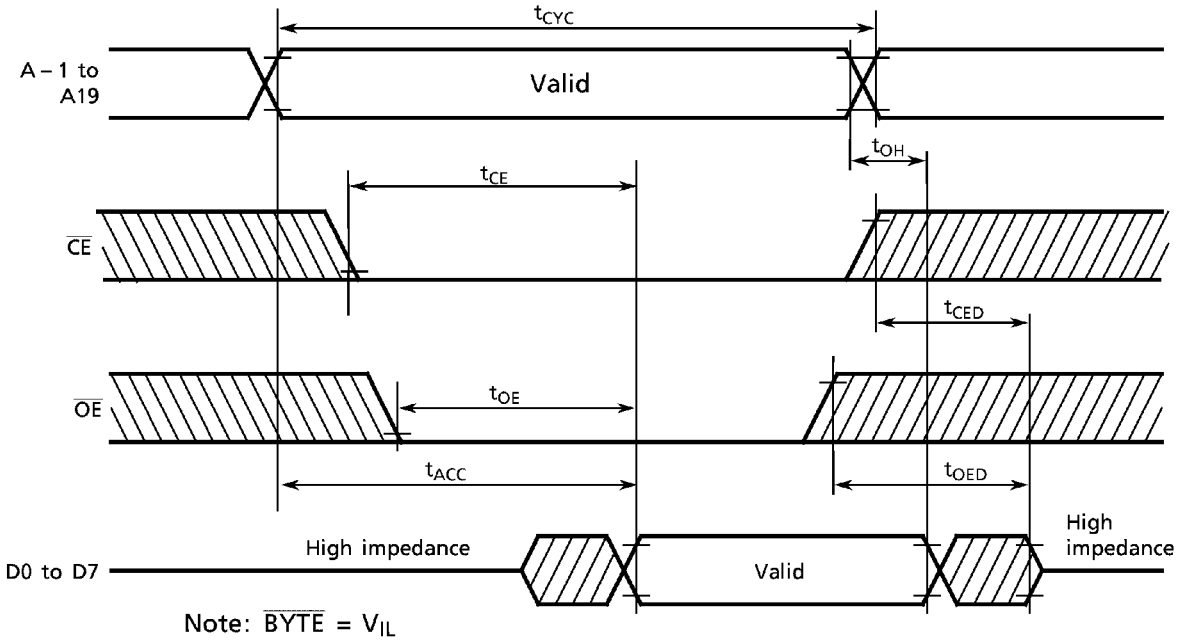
TIMING DIAGRAMS

WORD-WIDE READ MODE



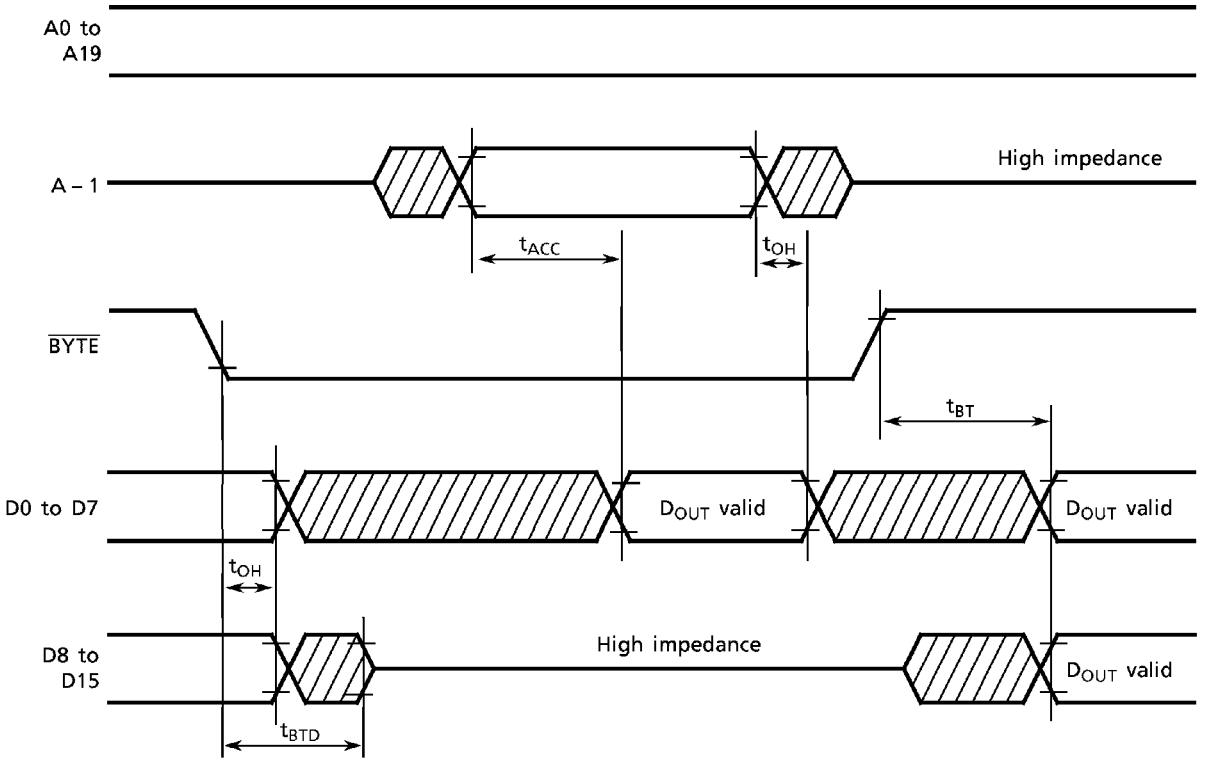
Note: $\overline{BYTE}$ = V_{IH}

BYTE-WIDE READ MODE



Note: $\overline{BYTE}$ = V_{IL}

$\overline{BYTE}$ TRANSITION



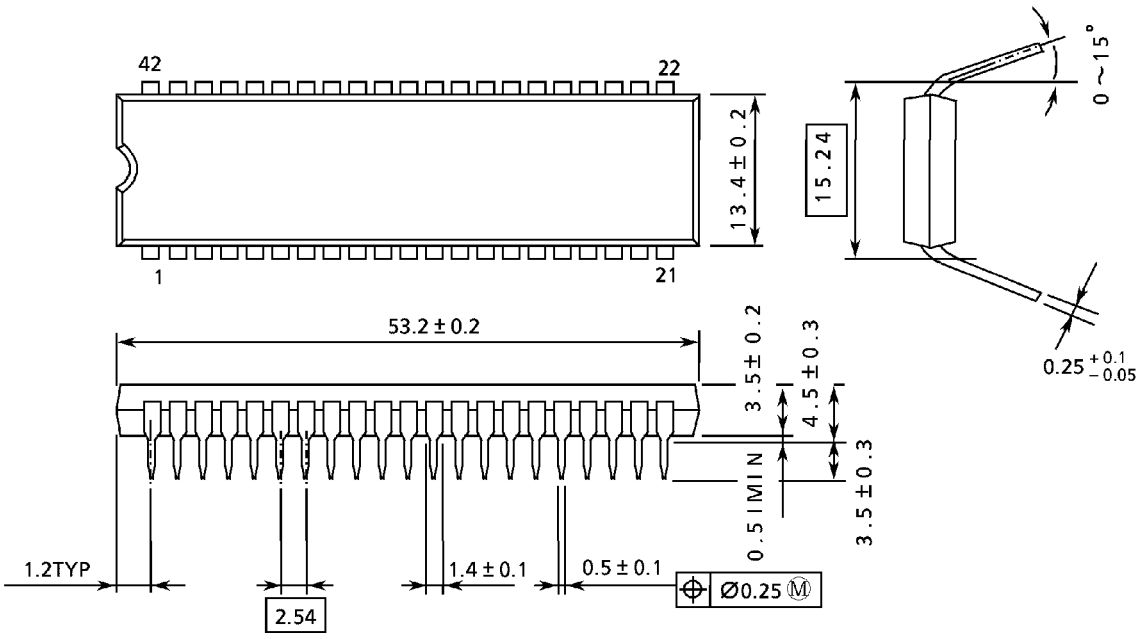
Note: $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}

PACKAGE DIMENSIONS

- Plastic DIP

DIP42−P−600

UNITS: mm



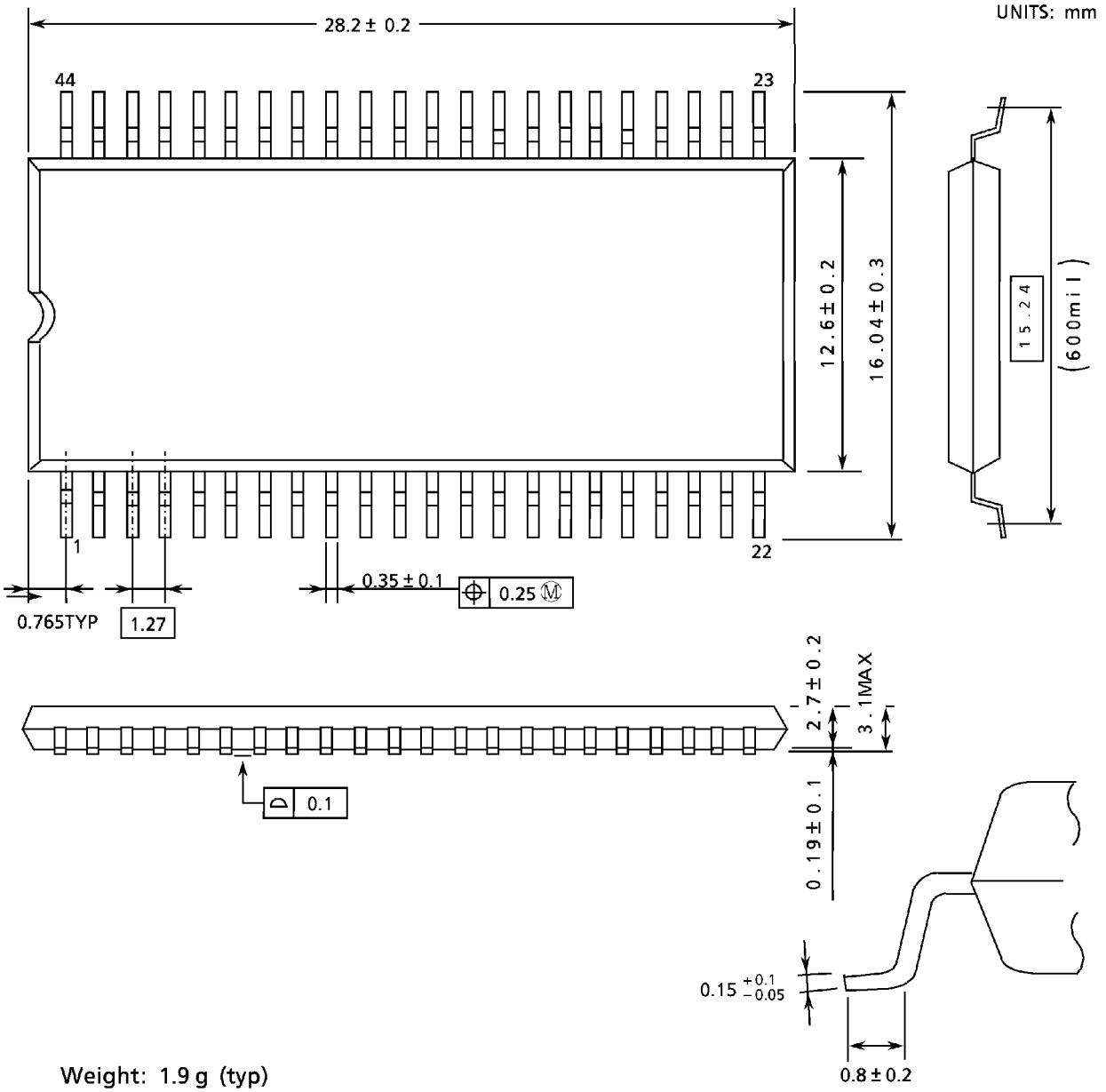
Weight: 5.7 g (typ)

Note: Package width and length do not include mold protrusion. The permissible mold protrusion is 0.15 mm.

PACKAGE DIMENSIONS

- Plastic SOP

  SOP44 – P – 600



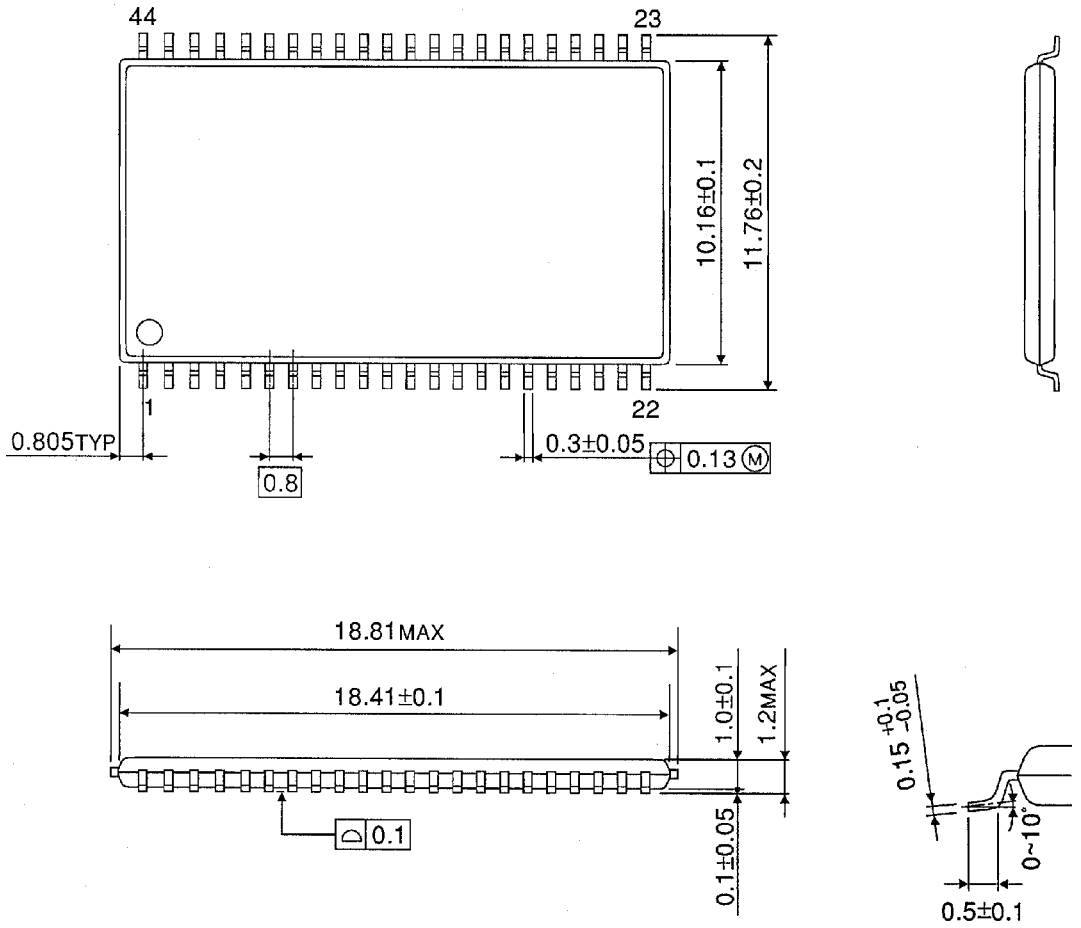
Weight: 1.9 g (typ)

Note: Package width and length do not include mold protrusion. The permissible mold protrusion is 0.15 mm.

PACKAGE DIMENSIONS

- TC5316200CFT

TSOP44－P－400



Weight: 0.5 g (typ)