P-Channel 30V Trench MOSFET, ESD Protection

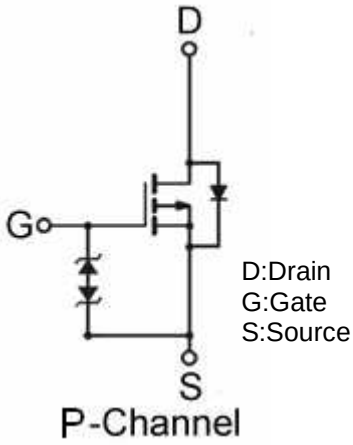
General Description

The LV20P03K is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance

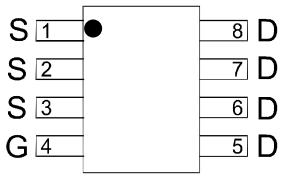
B_{VDSS}=-30V ,
$R_{DS(ON)}$ ≦20mΩ@V_{GS}=-10V
$R_{DS(ON)}$ ≦30mΩ@V_{GS}=-4.5V
I_D=-8.8A

Features

- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Marking: LV20P03K
- ESD Protection
- Qualified to MIL-STD-750E
- Moisture Sensitivity Level 3 per J-STD-020
- Weight: 0.08g
- RoHS Compliant



(SOP-8)
Top View



Application

- Power Management in Notebook
- Battery Powered System
- Load Switch
- DC/DC Converter

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

PARAMETER		SYMBOL	VALUE	UNIT
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current[1]	T_A=25℃	I_D	-8.8	A
	T_A=70℃		-7.1	
Pulsed Drain Current		I_{DM}	-35	A
Power Dissipation[1]	T_A=25℃	P_D	2.5	W
	T_A=70℃		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to150	℃

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNIT
Thermal Resistance Junction-to-Ambient[1]	R_{thJ_A}	50	℃ /W

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Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=-250uA	BV_{DSS}	-30	--	--	V
Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250uA	$V_{GS(th)}$	-0.8	--	-2	V
Gate-Source Leakage	V_{DS}=0V, V_{GS}=±16V	I_{GSS}	--	--	±10	uA
Zero Gate Voltage Drain Current	V_{DS}=-30V,V_{GS}=0V	I_{DSS}	--	--	-1	uA
Drain-Source On-Resistance[2]	V_{GS}=-10V,I_D=-5A	$R_{DS(ON)}$	--	14	20	mΩ
	V_{GS}=-4V,I_D=-5A		--	24	30	
DYNAMIC						
Total Gate Charge	V_{GS}=-10V,V_{DS}=-15V, I_D=-10A	Q_g	--	41.1	--	nC
Gate-Source Charge		Q_{gs}	--	7.9	--	
Gate-Drain Charge		Q_{gd}	--	11.9	--	
Input Capacitance	V_{GS}=0V,V_{DS}=-15V, F=1MHz	C_{iss}	--	1644	--	pF
Output Capacitance		C_{oss}	--	205	--	
Reverse Transfer Capacitance		C_{rss}	--	178	--	
Turn-On Delay Time	V_{GS} = -10V, V_{DS} = -15V, R_G = 4.7Ω, R_L=3Ω,I_D=-5A	$t_{d(on)}$	--	78	--	nS
Turn-On Rise Time		t_r	--	60.4	--	
Turn-Off Delay Time		$t_{d(off)}$	--	101	--	
Turn-Off Fall Time		t_f	--	31.6	--	
Source-Drain Diode						
Diode Forward voltage	Is=-10A, V_{GS}=0V	V_{SD}	--	--	-1.2	V

Notes:

(1). The device mounted on 1in^2 FR4 board with 2 oz copper

(2). Pulse test: Pulse width≦300us, duty cycle≦2%, guaranteed by design, not subject to production testing.

(3). LiteON Semiconductor reserves the right to improve product design, functions and reliability without notice

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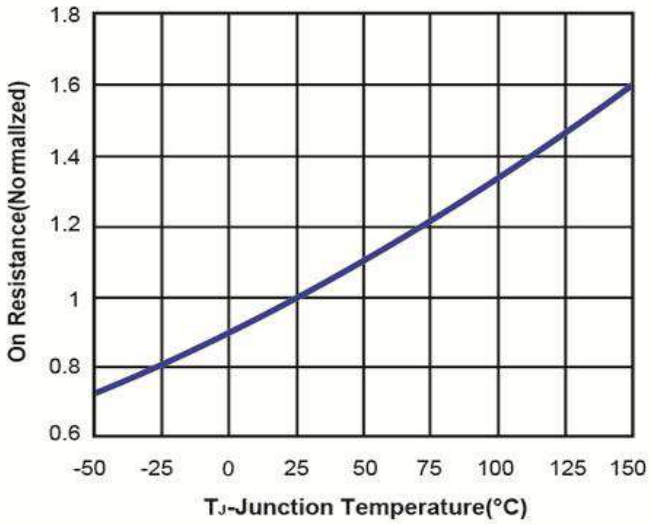
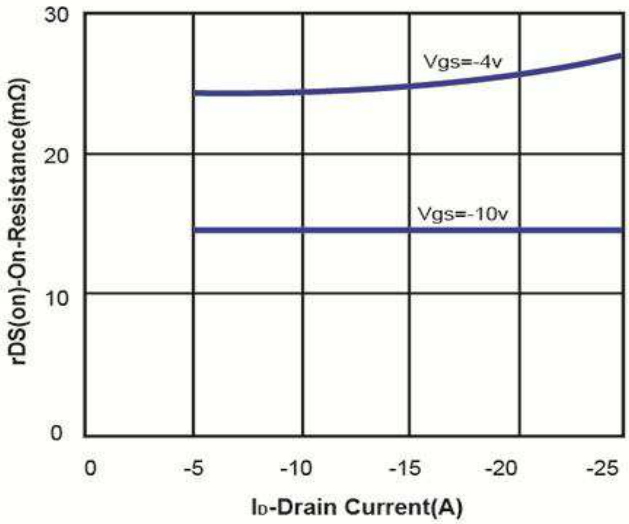
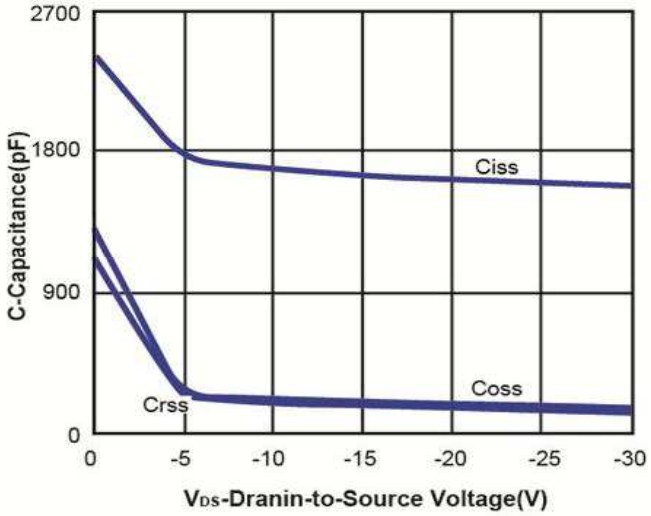
On Resistance vs. Junction Temperature



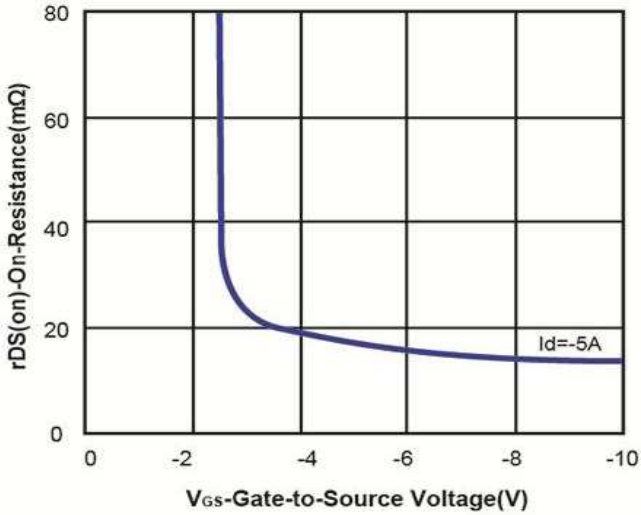
On Resistance vs. Drain Current



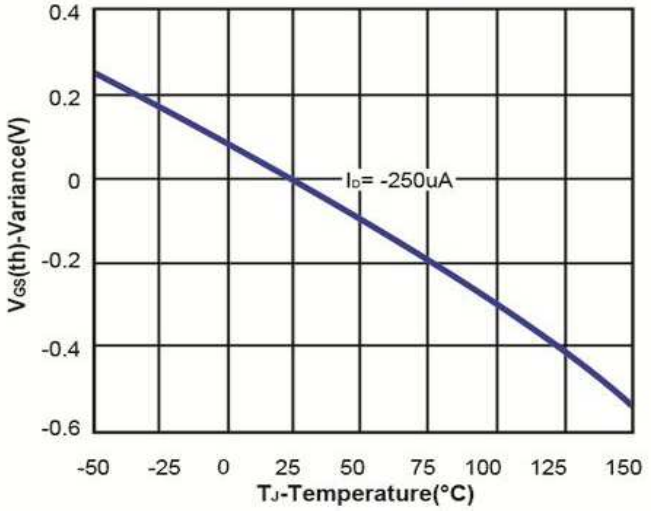
Capacitance



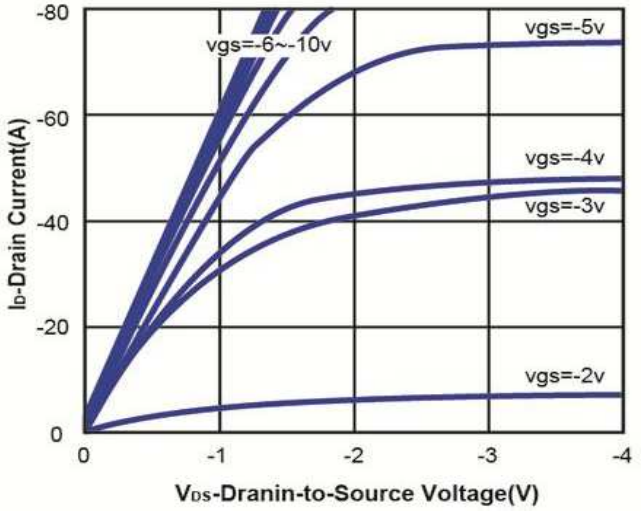
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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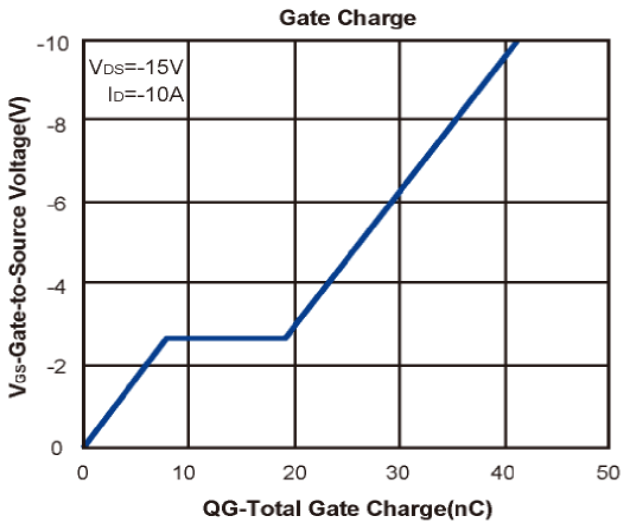

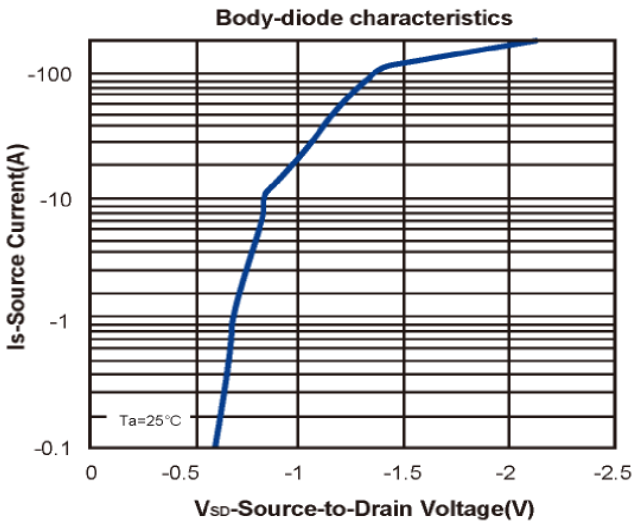

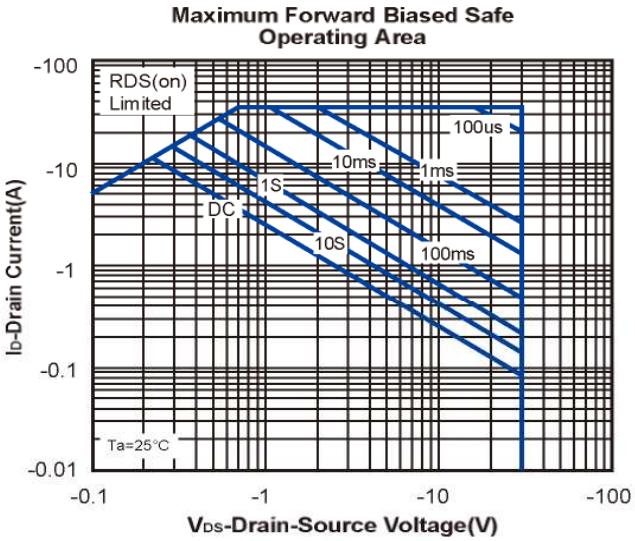

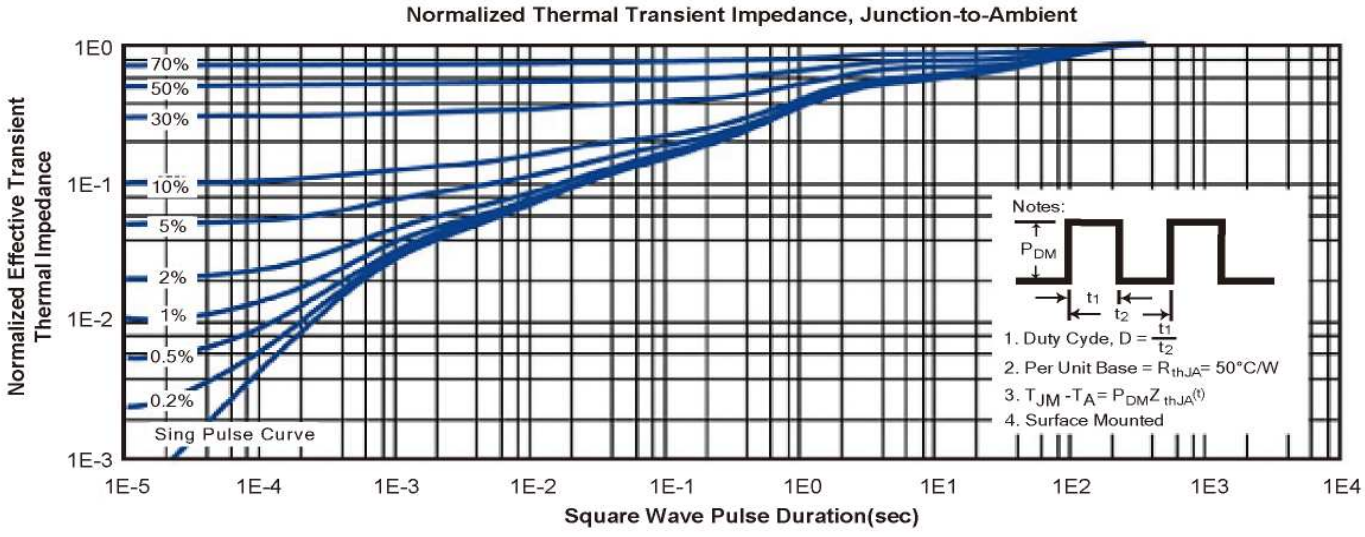

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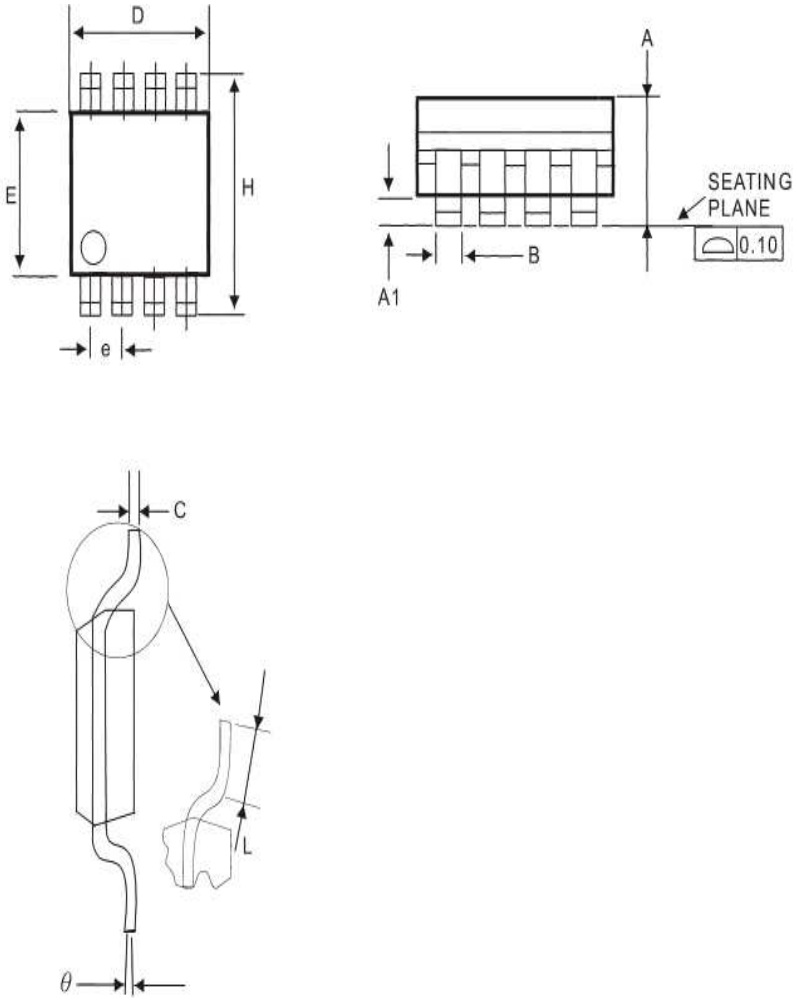
Package Outline Dimension

SOP-8



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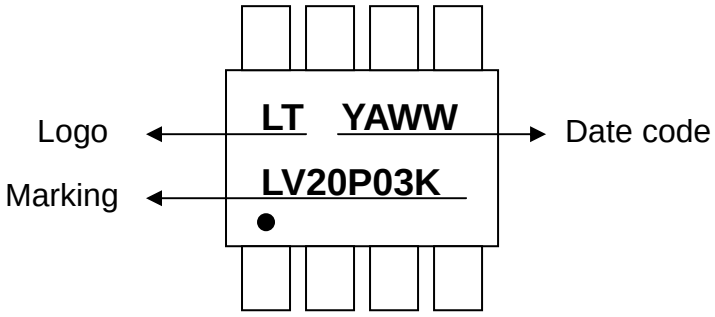
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27BSC	
H	5.80	6.20
L	0.40	1.25
Θ	0°	7°
All Dimensions in millimeter		

Marking information



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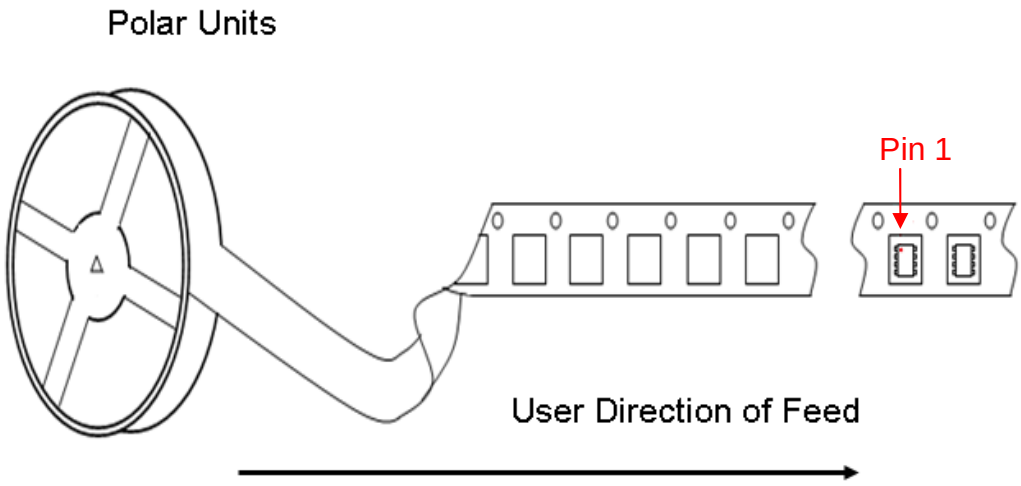
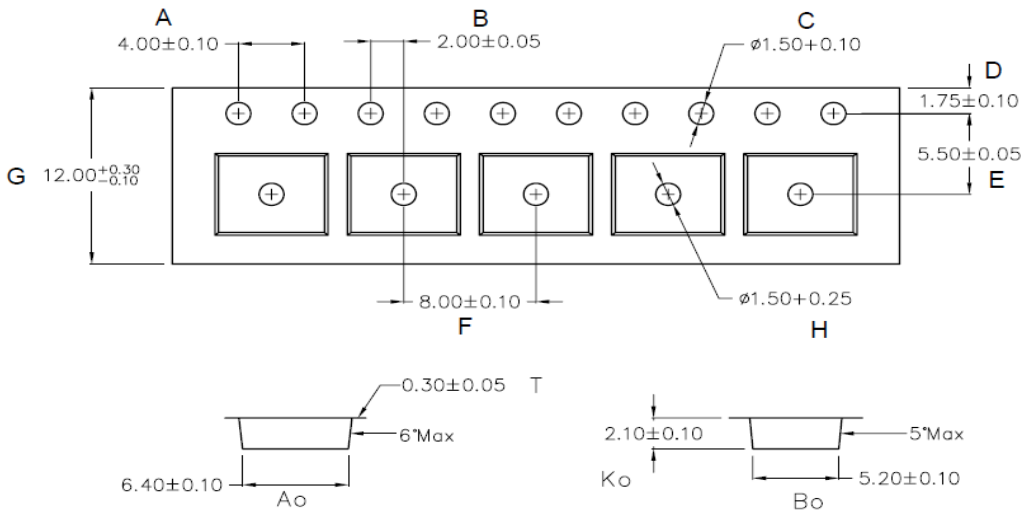
Packaging Information



DEVICE	Q'TY/REEL (PCS)	REEL DIA. (mm)	BOX SIZE (cm)	Q'TY/BOX (PCS)	CARTON SIZE (cm)	Q'TY/CARTON (PCS)
LV20P03K	2500	330	36.5x34x6	5K	39x39x38	30K

Embossed Carrier Dimensions Information



TAPE SIZE	A	B	C	D	E	F	Unit
12mm	4.00±0.10	2.00±0.05	1.50±0.10	1.75±0.10	5.50±0.05	8.00±0 .10	mm
	G	H	T	Ao	Ko	Bo	
	12.00+0.30/-0.10	Φ1.50+0.25	0.30±0.05	6.40±0.10	2.10±0.10	5.20±0.10	

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