DATA SHEET

NEC

LDMOS FIELD EFFECT TRANSISTOR
NEM091203P-28

N-CHANNEL SILICON POWER LDMOS FET
FOR 135 W UHF-BAND SINGLE-END POWER AMPLIFIER

DESCRIPTION

The NEM091203P-28 is an N-channel enhancement-mode lateral diffused MOS FET designed for 850 to 960 MHz applications, such as, GSM/EDGE/N-CDMA cellular base station. Dies are manufactured using our NEWMOS technology (our WSi gate lateral MOS FET), and its nitride surface passivation and quadruple layer aluminum silicon metallization offer a high degree of reliability.

FEATURES

- High 1 dB compression output power : $P_{O\ (1\ dB)}$ = 135 W TYP. (V_{DS} = 28 V, I_{Dset} = 1 200 mA, f = 850 to 960 MHz CW)
- High linear gain : G_L = 17.0 dB TYP. (V_{DS} = 28 V, I_{Dset} = 1 200 mA, f = 850 to 960 MHz CW)
- High drain efficiency : η_d = 58% TYP. (V_{DS} = 28 V, I_{Dset} = 1 200 mA, f = 850 to 960 MHz CW)
- Low intermodulation distortion : IM_3 = –40 dBc TYP. (V_{DS} = 28 V, I_{Dset} = 1 200 mA, f = 960/960.1 MHz, P_{out} = 45 dBm (2 tones))
  : IM_3 = –40 dBc TYP. (V_{DS} = 28 V, I_{Dset} = 1 200 mA, f = 880/880.1 MHz, P_{out} = 45 dBm (2 tones))
- Internal matched (Input and Output) for ease of use
- Low cost hollow plastic packages
- 100% screening
- Integrated ESD protection
- Effective prevention against humidity
- Excellent stability against HCI (Hot Carrier Injection)

APPLICATION

- Digital cellular base station PA : GSM/EDGE/N-CDMA etc.

ORDERING INFORMATION

Part Number	Order Number	Package	Supplying Form
NEM091203P-28	NEM091203P-28-A	T-97M (3P) (Pb-Free)	ESD protective envelope

Remark To order evaluation samples, contact your nearby sales office.
The unit sample quantity is 1 pcs.

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC Compound Semiconductor Devices representative for availability and additional information.

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ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	65	V
Gate to Source Voltage	V_{GS}	±7	V
Drain Current	I_D	12	A
Total Device Dissipation	P_{tot}	292	W
Channel Temperature	T_{ch}	200	°C
Storage Temperature	T_{stg}	–65 to +150	°C

THERMAL RESISTANCE (T_A = +25°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Thermal Resistance (Channel to case)	$R_{th\ (ch\text{-}c)}$		–	0.54	0.6	°C/W

RECOMMENDED OPERATING RANGE

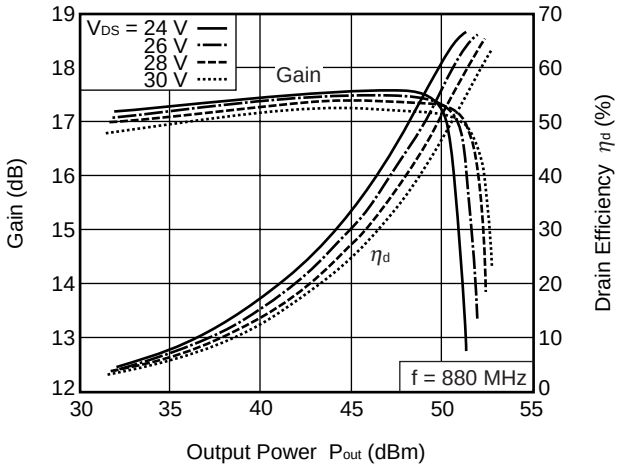
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	V_{DS}	–	28	30	V
Gate to Source Voltage	V_{GS}	2.5	3.0	4.0	V
Input Power	P_{in}	–	35	38	dBm

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

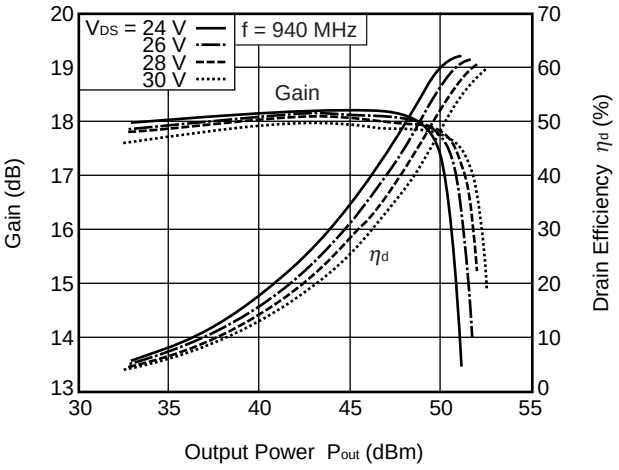
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
DC Characteristics						
Gate to Source Leak Current	I_{GSS}	V_{GSS} = 5V	–	–	1	μA
Drain to Source Leakage Current (Zero Gate Voltage Drain Current)	I_{DSS}	V_{DSS} = 65 V	–	–	1	mA
Gate Threshold Voltage	V_{th}	V_{DS} = 10 V, I_{DS} = 1 mA	1.7	2.2	2.8	V
Transconductance	g_m	V_{DS} = 20 V, I_{DS} = 1.2±0.1 A	–	5.6	–	S
Drain to Source Breakdown Voltage	BV_{DSS}	I_{DSS} = 10 μA	65	75	–	V
RF Characteristics						
Output Power	P_{out}	f = 920 to 960 MHz, P_{in} = 35 dBm,	50.8	51.3	–	dBm
Gain 1 dB Compression Output Power	$P_{O\ (1\ dB)}$	V_{DS} = 28 V, I_{Dset} = 1 200 mA	–	51.3	–	dBm
Drain Efficiency	η_d		50	58	–	%
Power Added Efficiency	η_{add}		–	57	–	%
Linear Gain	G_L	P_{in} = 25 dBm	16.5	18.0	–	dB
3rd Order Intermodulation Distortion	IM_3	f = 960/960.1 MHz, V_{DS} = 28 V, I_{Dset} = 1 200 mA, 2 tones P_{out} = 45 dBm	–	–40	–	dBc
Output Power	P_{out}	f = 880 MHz, P_{in} = 35 dBm,	–	52.0	–	dBm
Gain 1 dB Compression Output Power	$P_{O\ (1\ dB)}$	V_{DS} = 28 V, I_{Dset} = 1 200 mA	–	51.8	–	dBm
Drain Efficiency	η_d		–	60	–	%
Power Added Efficiency	η_{add}		–	58	–	%
Linear Gain	G_L	P_{in} = 29 dBm	–	17.0	–	dB
3rd Order Intermodulation Distortion	IM_3	f = 880/880.1 MHz, V_{DS} = 28 V, I_{Dset} = 1 200 mA, 2 tones P_{out} = 45 dBm	–	–40	–	dBc

TYPICAL CHARACTERISTICS (T_A = +25°C, V_{DS} = 28 V, I_{Dset} = 1 200 mA, unless otherwise specified)

GAIN, DRAIN EFFICIENCY vs. OUTPUT POWER



GAIN, DRAIN EFFICIENCY vs. OUTPUT POWER



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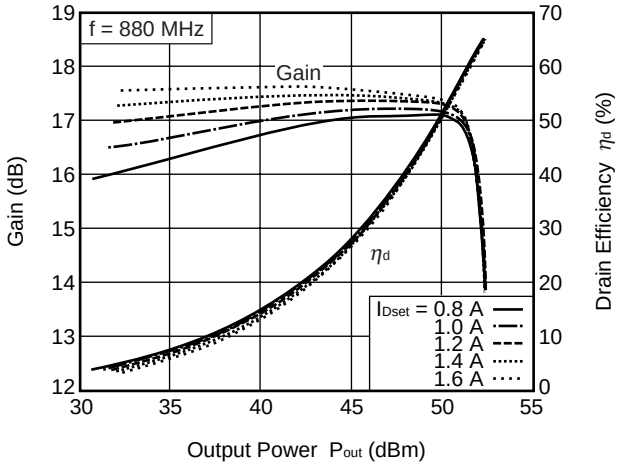

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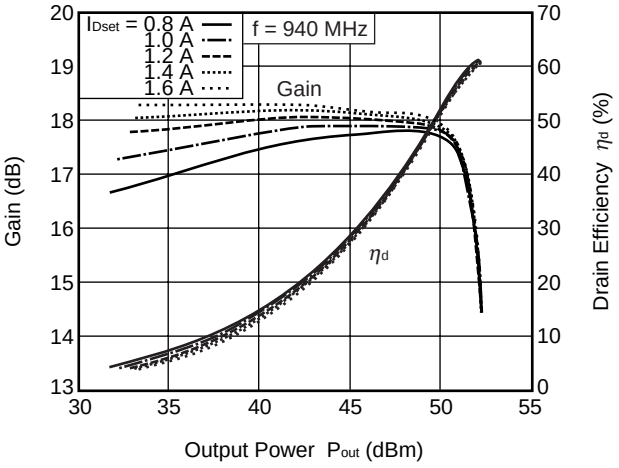
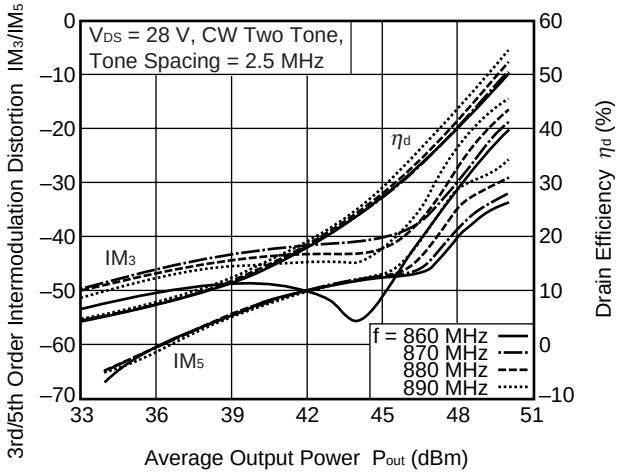
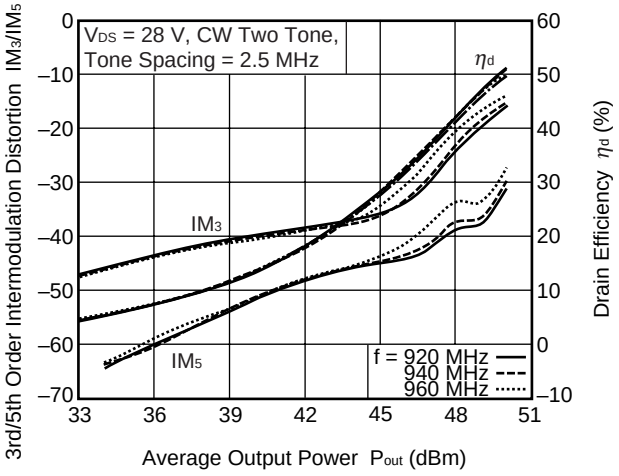


IM3/IM5, DRAIN EFFICIENCY vs. AVERAGE OUTPUT POWER

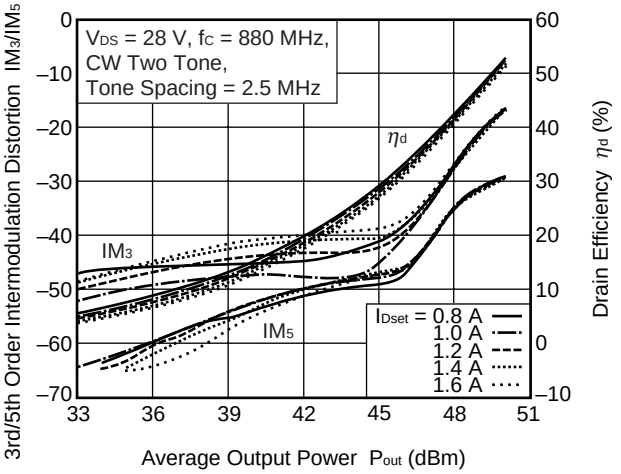


IM3/IM5, DRAIN EFFICIENCY vs. AVERAGE OUTPUT POWER

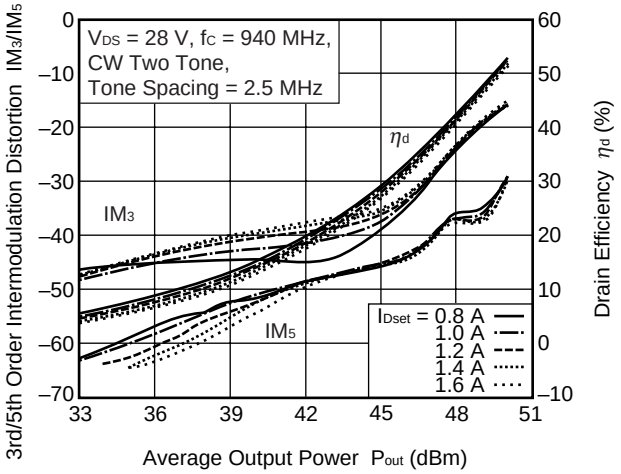


Remark The graphs indicate nominal characteristics.

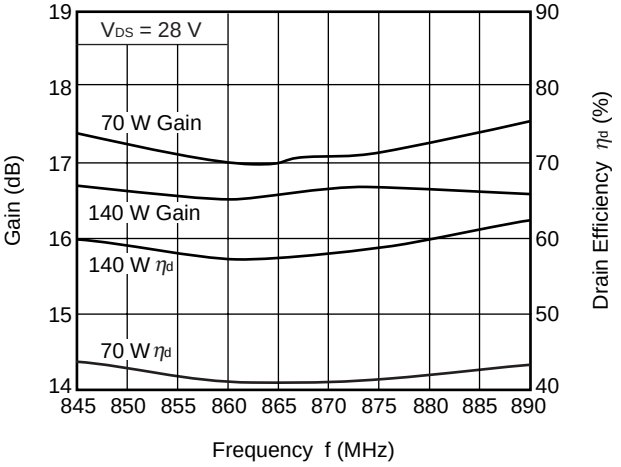
IM3/IM5, DRAIN EFFICIENCY vs. AVERAGE OUTPUT POWER



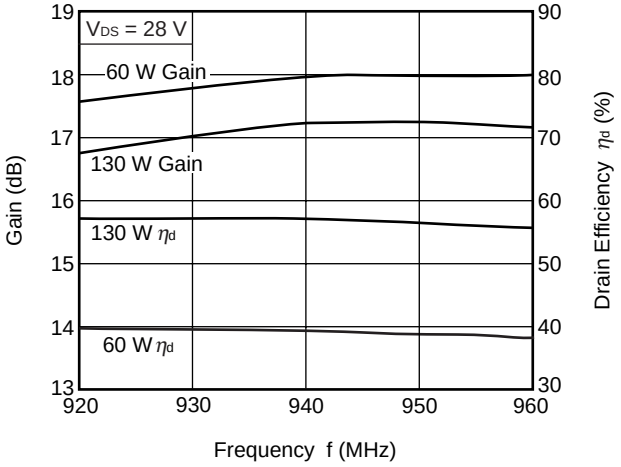
IM3/IM5, DRAIN EFFICIENCY vs. AVERAGE OUTPUT POWER



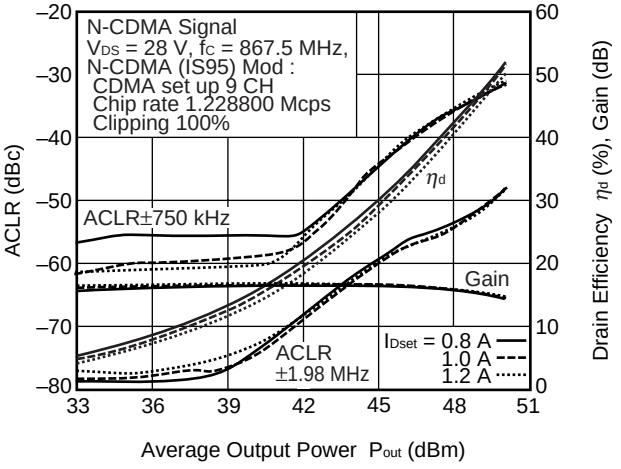
GAIN, DRAIN EFFICIENCY vs. FREQUENCY



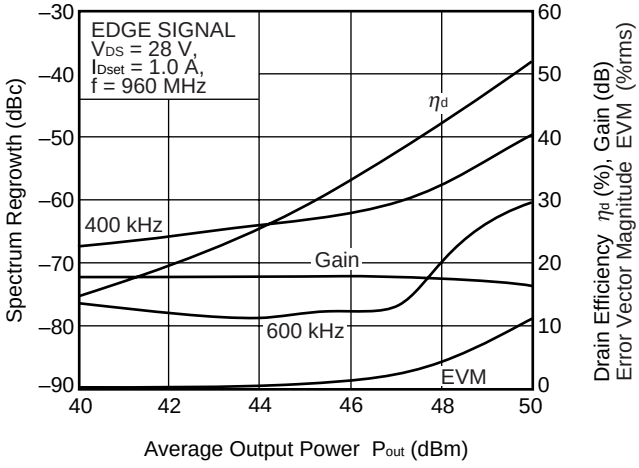
GAIN, DRAIN EFFICIENCY vs. FREQUENCY



ACLR, DRAIN EFFICIENCY, GAIN vs. AVERAGE OUTPUT POWER

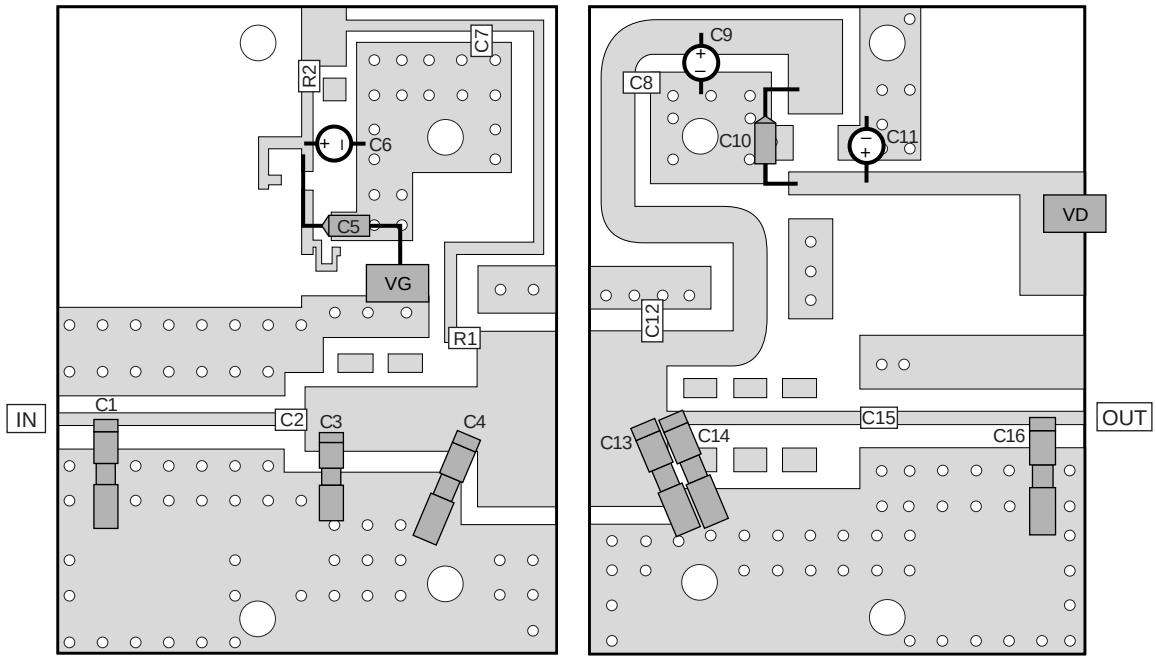


SPECTRUM REGROWTH, ηd, GAIN EVM vs. AVERAGE OUTPUT POWER

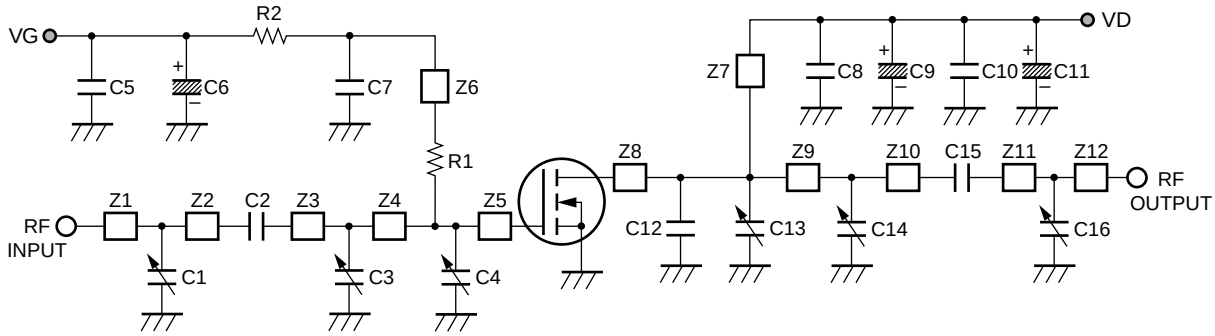


Remark The graphs indicate nominal characteristics.

COMPONENT LAYOUT OF TEST CIRCUIT FOR 920 TO 960 MHz



TEST CIRCUIT SCHMATIC FOR 920 TO 960 MHz



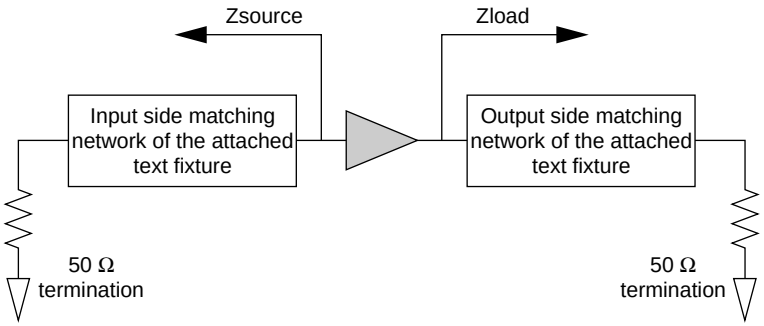
Symbol	Value	Symbol	Value
C2	43 pF Chip Capacitor	Z1	Line, 6.0 × 1.0 mm
C15	47 pF Chip Capacitor	Z2	Line, 16.4 × 1.0 mm
C7, C8	0.1 μF Chip Capacitor	Z3	Line, 1.9 × 5.5 mm
C12	6 pF Chip Capacitor	Z4	Line, 13.7 × 5.5 mm
C3	0.4 to 4 pF Variable Capacitor	Z5	Line, 7.0 × 15.0 mm
C1, C4, C13, C14, C16	0.8 to 8 pF Variable Capacitor	Z6	Line, 39.5 × 1.0 mm
C5, C10	1 000 pF EMI Suppression Filter	Z7	Line, 42.5 × 3.0 mm
C6, C11	47 μF Electrolytic Capacitor	Z8	Line, 5.7 × 15.0 mm
C9	1 μF Electrolytic Capacitor	Z9	Line, 3.0 × 1.0 mm
R1	10 Ω Chip Resistor	Z10	Line, 17.2 × 1.0 mm
R2	100 Ω Chip Resistor	Z11	Line, 12.4 × 1.0 mm
Circuit Board	Rogers 4350, εr = 3.55, Thickness 0.51 mm	Z12	Line, 3.5 × 1.0 mm

LARGE SIGNAL IMPEDANCE OF TEST BOARD FOR 920 TO 960 MHz

Measurement Condition: V_{DS} = 28 V, I_{Dset} = 1.2 A

f (MHz)	Z_{in} (Ω)	Z_{out} (Ω)
920	5.20+j1.78	1.36+j0.91
940	5.18+j2.20	1.15+j0.60
960	5.06+j2.56	1.05+j0.23

Remark Z_{in} = Conjugate of Zsource, Z_{out} = Conjugate of Zload



S-PARAMETERS

S-parameters/Noise parameters are provided on the NEC Compound Semiconductor Devices Web site in a form (S2P) that enables direct import to a microwave circuit simulator without keyboard input.

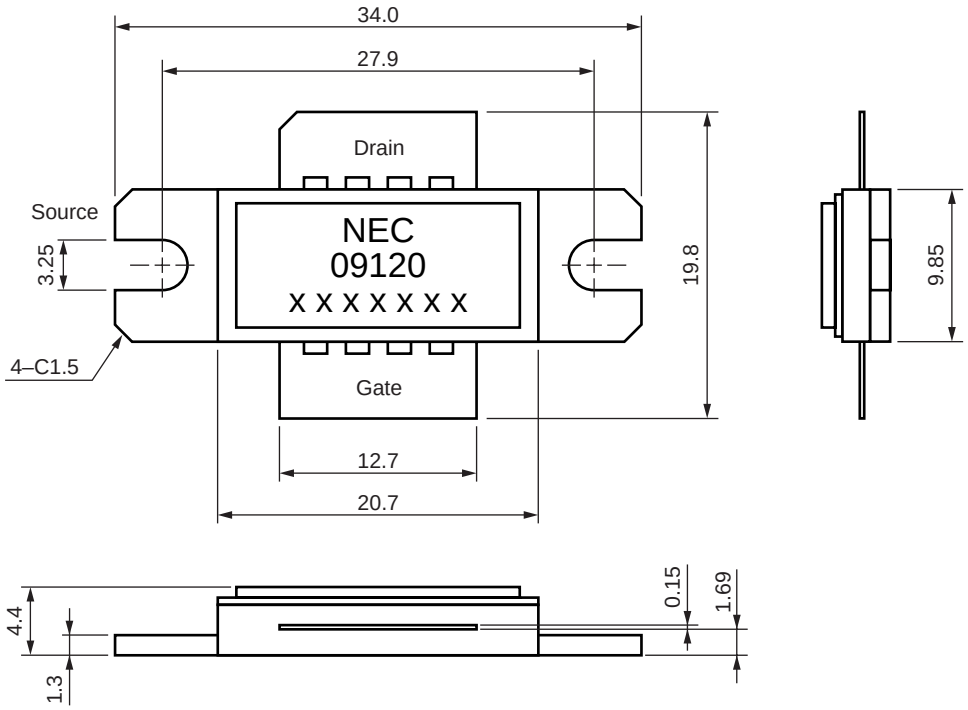
Click here to download S-parameters.

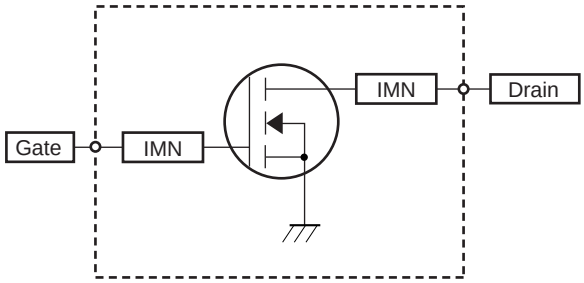
[RF and Microwave] → [Device Parameters]

URL http://www.ncsd.necel.com/

PACKAGE DIMENSIONS

T-97M (3P) (UNIT: mm)





IMN : Internal Matching Network

RECOMMENDED MOUNTING CONDITIONS FOR CORRECT USE

(1) Fix to a heat sink or mount surface completely with screws at the two holes of the flange.

(2) The recommended torque strength of the screws is 29.4 N·cm typical using M3 type screws.

(3) The recommended flatness of the mount surface is less than ±10 μm (roughness of surface is $\nabla\nabla\nabla$).

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions		Condition Symbol
Partial Heating	Peak temperature (terminal temperature)	: 350°C or below	HS350-P3
	Soldering time (per terminal of device)	: 3 seconds or less	
	Maximum chlorine content of rosin flux (% mass)	: 0.2%(Wt.) or below	

Caution Do not use different soldering methods together (except for partial heating).

When the product(s) listed in this document is subject to any applicable import or export control laws and regulation of the authority having competent jurisdiction, such product(s) shall not be imported or exported without obtaining the import or export license.

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M8E 00.4-0110

▶**For further information, please contact**

NEC Compound Semiconductor Devices, Ltd. **http://www.ncsd.necel.com/**
E-mail: salesinfo@ml.ncsd.necel.com (sales and general)
techinfo@ml.ncsd.necel.com (technical)
Sales Division TEL: +81-44-435-1573 FAX: +81-44-435-1579

NEC Compound Semiconductor Devices Hong Kong Limited
E-mail: ncsd-hk@elhk.nec.com.hk (sales, technical and general)
Hong Kong Head Office TEL: +852-3107-7303 FAX: +852-3107-7309
Taipei Branch Office TEL: +886-2-8712-0478 FAX: +886-2-2545-3859
Korea Branch Office TEL: +82-2-558-2120 FAX: +82-2-558-5209

NEC Electronics (Europe) GmbH **http://www.ee.nec.de/**
TEL: +49-211-6503-0 FAX: +49-211-6503-1327

California Eastern Laboratories, Inc. **http://www.cel.com/**
TEL: +1-408-988-3500 FAX: +1-408-988-0279

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