Z8036/8536

Counter/Timer and Parallel I/O Unit

DISTINCTIVE CHARACTERISTICS

- Two independent 8-bit, double-buffered, bidirectional I/O ports plus a 4-bit special purpose I/O port. I/O ports feature programmable polarity, programmable direction (Bit mode), "pulse catchers" and programmable open-drain outputs.
- Four handshake modes, including 3-wire (like the IEEE-488).
- REQUEST/$\overline{\text{WAIT}}$ signal for high-speed data transfer.
- Flexible pattern-recognition logic, programmable as a 16-vector interrupt controller.
- Three independent 16-bit counter/timers with up to four external access lines per counter/timer (count input, output, gate, and trigger), and three output duty cycles (pulsed, one-shot, and square-wave), programmable as retriggerable or nonretriggerable.
- Easy to use since all registers are read/write and directly addressable.

GENERAL DESCRIPTION

The Z8036* CIO Counter/Timers and Parallel I/O elements are general-purpose peripheral circuits, satisfying most counter/timer and parallel I/O needs encountered in system designs. These versatile devices contain three I/O ports and three counter/timers. Many programmable options tailor their configuration to specific applications.

The use of these devices is simplified by making all internal registers (command, status, and data) readable and (except for status bits) writable. Each register is given its own unique address so that it can be accessed directly on the Z8036. The Z8036 is directly Z-Bus compatible.

CIO BLOCK DIAGRAM

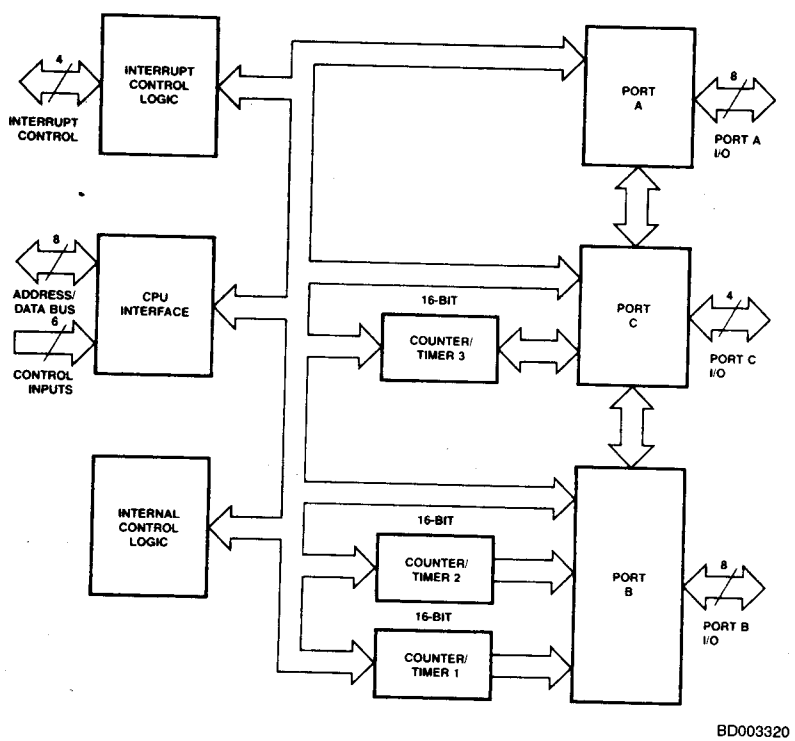

Figure 1.

*Z8000 is a trademark of Zilog, Inc.

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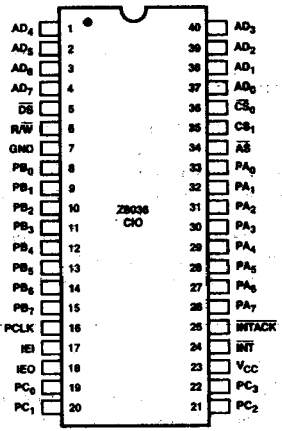
Refer to page 7-1 for Essential Information on Military Devices

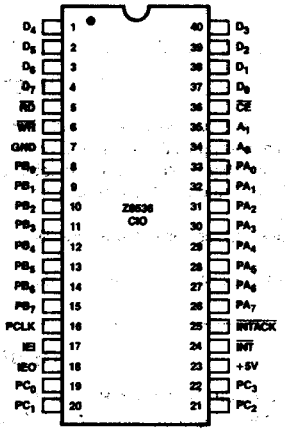
CONNECTION DIAGRAM
Top View

D-40-1, P-40-1



CD005140

D-40-1, P-40-1



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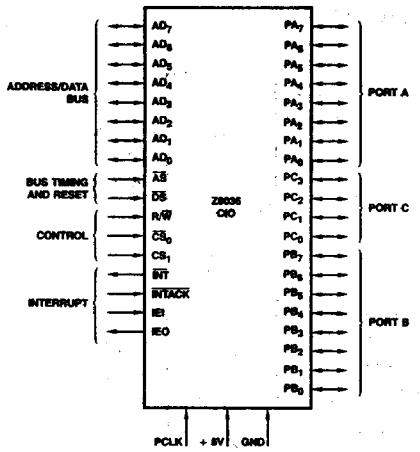
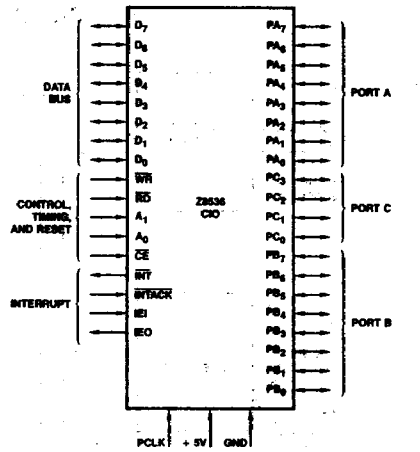
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



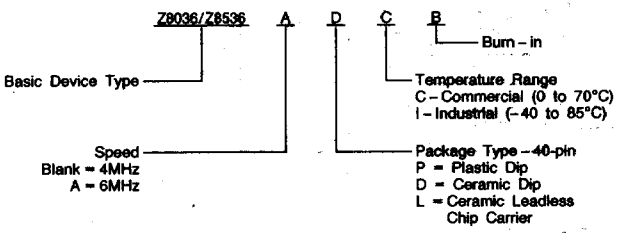
LS001180



LS001190

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations		
Z8036[1]	4MHz 6MHz	DC, PC, DI, ADC, APC
Z8536	4MHz 6MHz	DC, PC, DI, ADC, APC

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
23	V_{CC}		+5V Power Supply
7	GND		Ground
17	IEI	I	Interrupt Enable In. IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device on the system bus. A HIGH IEI indicates to the CIO that no other higher priority device has an interrupt under service or is requesting an interrupt.
18	IEO	O	Interrupt Enable Out. IEO is normally connected to the next lower priority device's IEI input and inhibits interrupts from lower priority devices. IEO is HIGH only if IEI is HIGH and the CIO has not requested an interrupt.
24	$\overline{INT}$	O	Interrupt Request (Open Drain). This signal is active LOW when the CIO is requesting an interrupt and stays active until the end of the interrupt acknowledge sequence.
25	$\overline{INTACK}$	I	Interrupt Acknowledge. This signal, when active LOW, indicates to the CIO that an interrupt acknowledge cycle is in progress. $\overline{INTACK}$ is sampled while $\overline{AS}$ is LOW.
33-26	PA_0-PA_7	I/O	Port A I/O lines (Bidirectional, 3-state, or Open Drain). These eight I/O lines transfer information between Port A and external devices.
8-15	PB_0-PB_7	I/O	Port B I/O lines (Bidirectional, 3-state, or Open Drain). These eight I/O lines transfer information between Port B and external devices. The lines can also be programmed to provide external access to Counters/Timers 1 and 2.
19-22	PC_0-PC_3	I/O	Port C I/O lines (Bidirectional, 3-state, or Open Drain). These four I/O lines provide Handshake, WAIT and REQUEST lines for Ports A and B, or provide external access to Counter/Timer 3 or access to Port C.
16	PCLK	I	Peripheral Clock. PCLK may be synchronous or asynchronous to the CPU's clock and may be of lower frequency than the CPU's clock. It is used with timers and Request/Wait logic. The input is TTL compatible.
Z8036 Only			
37-40, 1-4	AD_0-AD_7	I/O	Address/Data Bus (Bidirectional, 3-state). Multiplexed address/data lines for transfers between the CPU and CIO.
34	$\overline{AS}$*	I	Address Strobe. Register addresses on AD_0 -AD_7 lines, $\overline{INTACK}$, and $\overline{CS_0}$ are sampled while $\overline{AS}$ is LOW, and latched while $\overline{AS}$ is HIGH.
36, 35	$\overline{CS_0}$ and $\overline{CS_1}$	I	Chip Select 0 and Chip Select 1. Chip Select 0 and Chip Select 1 must be LOW and HIGH, respectively, to select the device. $\overline{CS_0}$ is latched by $\overline{AS}$.
5	$\overline{DS}$*	I	Data Strobe. An active LOW $\overline{DS}$ provides t he timing for transfer of data to or from the CIO. The R/$\overline{W}$ input indicates the direction of data transfer.
6	R/$\overline{W}$	I	Read/Write. R/$\overline{W}$ is active HIGH when the CPU is reading from the CIO and active LOW when the CPU is writing to the CIO.
Z8536 Only			
34, 35	A_0-A_1	I	Address Lines. These two lines are used to select the register involved in the CPU transaction: Port A's Data register, Port B's Data register, Port C's Data register, or a control register.
36	$\overline{CE}$	I	Chip Enable (Active LOW). A LOW level on this input enables the CIO to be read from or written to.
37-40, 1-4	D_0-D_7	I/O	Data Bus (Bidirectional, 3-state). These eight data lines are used for transfers between the CPU and the CIO.
5	$\overline{RD}$**	I	Read (Active LOW). This signal indicates that a CPU is reading from the CIO. During an interrupt acknowledge cycle, this signal gates the interrupt vector onto the data bus if the CIO is the highest priority device requesting an interrupt.
6	$\overline{WR}$**	I	Write (Active LOW). This signal indicates a CPU write to the CIO.

*When $\overline{AS}$ and $\overline{DS}$ are detected LOW at the same time (normally an illegal condition), the CIO is reset.
**When $\overline{RD}$ and $\overline{WR}$ are detected LOW at the same time (normally an illegal condition), the CIO is reset.

Refer to page 7-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... 65 to +150°C
Voltage at any Pin Relative V_{SS} ..... −0.5 to +7.0V
Power Dissipation 1.75W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

	4MHz	6MHz
Commercial Operating Range T_A = 0 to +70°C V_{CC} = 5V ±5% V_{SS} = 0V	Z8036DC Z8036PC Z8536DC Z8536PC	Z8036ADC Z8036APC Z8536ADC Z8536APC
Industrial Operating Range T_A = −40 to +85°C V_{CC} = 5V ±10% V_{SS} = 0V	Z8036DI Z8536DI	

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Note 1)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
V_{IL}	Input LOW Voltage		−0.5		+0.8	Volts
V_{IH}	Input HIGH Voltage	Standard	2.0		V_{CC}	Volts
		Industrial	2.4			
V_{OL}	Output LOW Voltage	I_{OL} = 2.0mA			0.4	Volts
		I_{OL} = 3.2mA			0.5	
V_{OH}	Output HIGH Voltage	I_{OH} = −250µA	2.4			Volts
I_{OZL}	Output Leakage Current	V_{OUT} = 0.4V			10	µA
I_{OZH}	Output Leakage Current	V_{OUT} = V_{CC}			10	µA
I_I	Input Leakage Current				±10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, T_A = 0°C			200	mA
C_{IN}	Input Capacitance	Unmeasured pins returned to ground f = 1MHz			10	pF
C_{OUT}	Output Capacitance				15	pF
$C_{I/O}$	Bidirectional Capacitance				20	pF

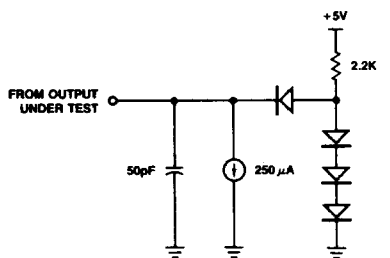
Note: See table for operating range. Typical conditions apply at T_A = 25°C, V_{CC} = 5.0V.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

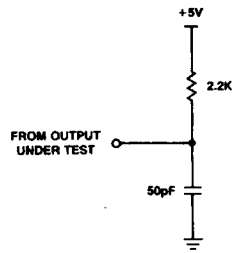
+4.75V ≤ V_{CC} ≤ +5.25V
GND = 0V
0°C ≤ T_A ≤ +70°C

Standard Test Load



TC001600

Open-Drain Test Load



TC001610

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Z8036/Z8536 HANDSHAKE TIMING (Figures 2, 3, 4)

Number	Parameters	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TsDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ Setup Time	0		0		ns
2	ThDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ Hold Time – Strobed HS	500		500		ns
3	TdACKf(RFD)	$\overline{ACKIN}$ ↓ to RFD ↓ Delay	0		0		ns
4	TwACKl	$\overline{ACKIN}$ Low Width – Strobed HS	250		250		ns
5	TwACKh	$\overline{ACKIN}$ High Width – Strobed HS	250		250		ns
6	TdRFDr(ACK)	RFD ↑ to $\overline{ACKIN}$ ↓ Delay	0		0		ns
7	TsDO(DAV)	Data Out to $\overline{DAV}$ ↓ Setup Time (Note 1)	25		20		ns
8	TdDAVf(ACK)	$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ Delay	0		0		ns
9	ThDO(ACK)	Data Out to $\overline{ACKIN}$ ↓ Hold Time	1		1		$\overline{AS}$ cycle
10	TdACK(DAV)	$\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ Delay	1		1		$\overline{AS}$ cycle
11	ThDI(RFD)	Data Input to RFD ↓ Hold Time – Interlocked HS	0		0		ns
12	TdRFDf(ACK)	RFD ↓ to $\overline{ACKIN}$ ↑ Delay – Interlocked HS	0		0		ns
13	TdACKr(RFD)	$\overline{ACKIN}$ ↑ ($\overline{DAV}$ ↑) to RFD ↑ Delay – Interlocked and 3-Wire HS	0		0		ns
14	TdDAVr(ACK)	$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↑ (RFD ↑) – Interlocked and 3-Wire HS	0		0		ns
15	TdACK(DAV)	$\overline{ACKIN}$ ↑ (RFD ↑) to $\overline{DAV}$ ↓ Delay – Interlocked and 3-Wire HS	0		0		ns
16	TdDAVlf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay – Input 3-Wire HS	0		0		ns
17	ThDI(DAC)	Data Input to DAC ↑ Hold Time – 3-Wire HS	0		0		ns
18	TdDACOr(DAV)	DAC ↑ $\overline{DAV}$ ↑ Delay – Input 3-Wire HS	0		0		ns
19	TdDAVlr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay – Input 3-Wire HS	0		0		ns
20	TdDAVOf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay – Output 3-Wire HS	0		0		ns
21	ThDO(DAC)	Data Output to DAC ↑ Hold Time – 3-Wire HS	1		1		$\overline{AS}$ cycle
22	TdDAClr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ Delay – Output 3-Wire HS	1		1		$\overline{AS}$ cycle
23	TdDAVOr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay – Output 3-Wire HS	0		0		ns

Note: 1. This time can be extended through the use of the Deskew Timers.
*Timings are all preliminary and subject to change. All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0."

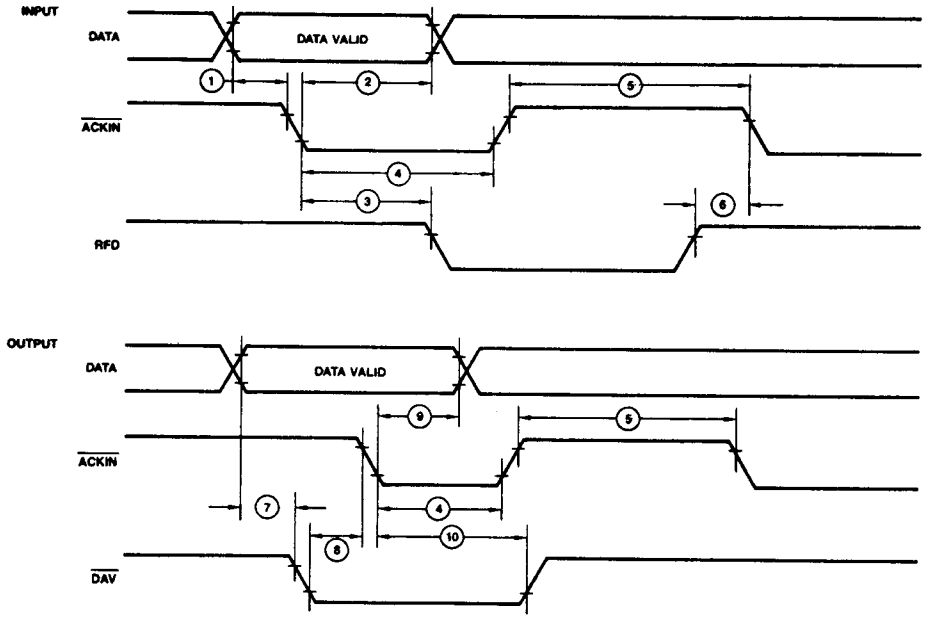


Figure 2. Strobed Handshake

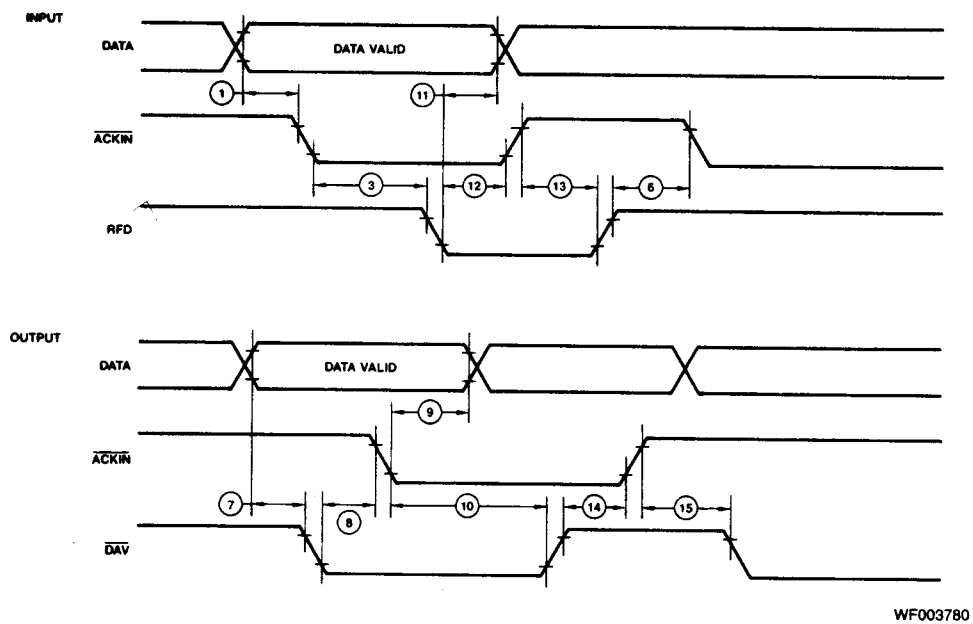


Figure 3. Interlocked Handshake

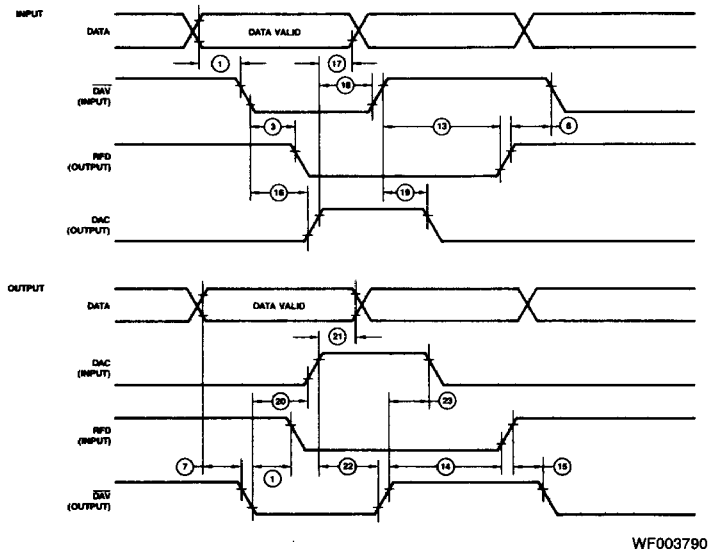


Figure 4. Three-Wire Handshake

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Z8036 COUNTER/TIMER TIMING (Figure 5)

Number	Parameters	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TcPC	PCLK Cycle Time (Note 1)	250	4000	165	4000	ns
2	TwPCh	PCLK High Width	105	2000	70	2000	ns
3	TwPCl	PCLK Low Width	105	2000	70	2000	ns
4	TfPC	PCLK Fall Time		20		10	ns
5	TrPC	PCLK Rise Time		20		15	ns
6	TcCl	Counter Layout Cycle Time	500		330		ns
7	TCIh	Counter Input High Width	230		150		ns
8	TwCIl	Counter Input Low Width	230		150		ns
9	TfCl	Counter Input Fall Time		20		15	ns
10	TrCl	Counter Input Rise Time		20		15	ns
11	TsTI(PC)	Trigger Input to PCLK Setup Time (Timer Mode) (Note 2)	150		150		ns
12	TsTI(Cl)	Trigger Input to Counter Input Setup Time (Counter Mode) (Note 2)	150		150		ns
13	TwTI	Trigger Input Pulse Width (High or Low)	200		200		ns
14	TsGI(PC)	Gate Input to PCLK ↓ Setup Time (Timer Mode) (Note 2)	100		100		ns
15	TsGI(Cl)	Gate Input to Counter Input ↓ Setup Time (Counter Mode) (Note 2)	100		100		ns
16	ThGI(PC)	Gate Input to PCLK ↓ Hold Time (Timer Mode) (Note 2)	100		100		ns
17	ThGI(Cl)	Gate Input to Counter Input ↓ Hold Time (Counter Mode) (Note 2)	100		100		ns
18	TdPC(CO)	PCLK to Counter Output Delay (Timer Mode)		475		475	ns
19	TdCl(CO)	Counter Input to Counter Output Delay (Counter Mode)		475		475	ns

Notes: 1. PCLK is only used with the counter/timers (in Timer mode), the deskew timers, and the REQUEST/$\overline{\text{WAIT}}$ logic. If these functions are not used, the PCLK input can be held low.
2. These parameters must be met to guarantee that either the trigger or gate is valid for the next counter/timer cycle.

*Timings are preliminary and subject to change. All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0."

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Refer to page 7-1 for Essential Information on Military Devices

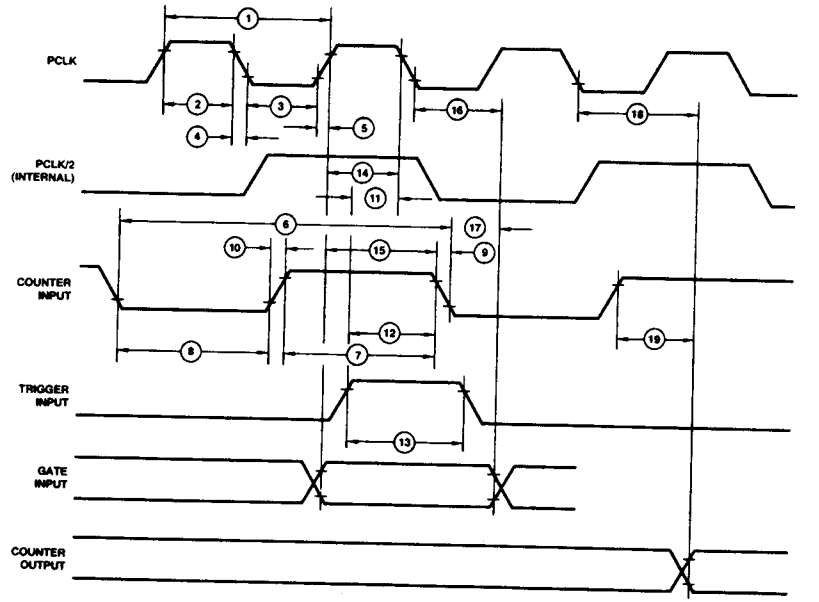

Figure 5. Counter/Timer Timing

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Z8036 RESET TIMING (Figure 6)

Number	Parameters	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TdDSQ(AS)	Delay from $\overline{DS}$ ↑ to $\overline{AS}$ ↓ for No Reset	40		15		ns
2	TdASQ(DS)	Delay from $\overline{AS}$ ↑ to $\overline{DS}$ ↓ for No Reset	50		30		ns
3	TwRES	Minimum Width of $\overline{AS}$ and $\overline{DS}$ both Low for Reset (Note 1)	250		170		ns

Note: 1. Internal circuitry allows for the reset provided by the Z8 ($\overline{DS}$ held Low while $\overline{AS}$ pulses) to be sufficient.
*Timings are preliminary and subject to change. All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0".

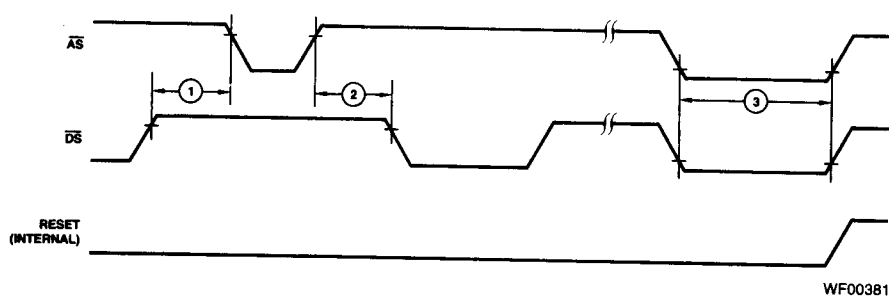

Figure 6. Reset Timing

Refer to page 7-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Z8036/Z8536 MISCELLANEOUS PORT TIMING (Figure 7)

Number	Parameters	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	Trl	Any Input Rise Rate Time		100		100	ns
2	Tfl	Any Input Fall Time		100		100	ns
3	Tw1's	1's Catcher High Width (Note 1)	250		170		ns
4	TwPM	Pattern Match Input Valid (Bit Port)	750		500		ns
5	TsPMD	Data Latched on Pattern Match Setup Time (Bit Port)	0		0		ns
6	ThPMD	Data Latched on Pattern Match Hold Time (Bit Port)	1000		650		ns

Note: 1. If the input is programmed inverting, a Low-going pulse of the same width will be detected.
*Timings are preliminary and subject to change. All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0."

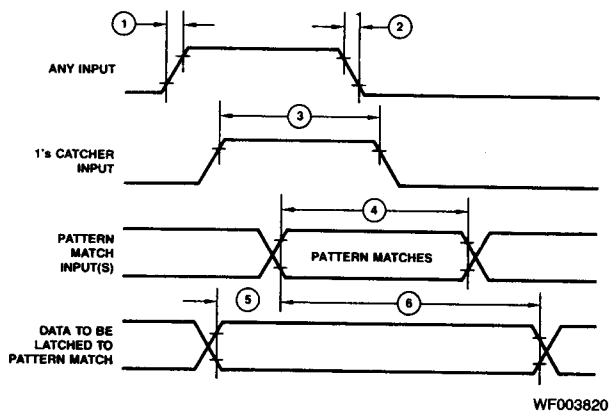

Figure 7. Miscellaneous Port Timing

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Z8036 CPU INTERFACE TIMING (Figure 8)

Number	Parameters	Description	4MHz Min	4MHz Max	6MHz Min	6MHz Max	Units
1	TwAs	$\overline{AS}$ Low Width	70	2000	50	2000	ns
2	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time (Note 1)	30		10		ns
3	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time (Note 1)	50		30		ns
4	TsA(DS)	Address to $\overline{DS}$ ↓ Setup Time (Note 1)	130		100		ns
5	TsCSO(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Setup Time (Note 1)	0		0		ns
6	ThCSO(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Hold Time (Note 1)	60		40		ns
7	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay (Note 1)	60		40		ns
8	TsCSI(DS)	CS_1 to $\overline{DS}$ ↓ Setup Time	100		80		ns
9	TsRWR(DS)	R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Setup Time	100		80		ns
10	TsRWW(DS)	R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Setup Time	0		0		ns
11	TwDS	$\overline{DS}$ Low Width	390		250		ns
12	TsDW(DSf)	Write Data to $\overline{DS}$ ↓ Setup Time	30		20		ns
13	TdDS(DRV)	$\overline{DS}$ (Read) ↓ to Address Data Bus Driven	0		0		ns
14	TdDSf(DR)	$\overline{DS}$ ↓ to Read Data Valid Delay		250		180	ns
15	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	30		20		ns
16	TdDSr(DR)	$\overline{DS}$ ↑ to Read Data Not Valid Delay	0		0		ns
17	TdDS(DRz)	$\overline{DS}$ ↑ Read Data Float Delay (Note 2)		70		45	ns
18	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time	55		40		ns
19	ThCSI(DS)	CS_1 to $\overline{DS}$ ↑ Hold Time	55		40		ns
20	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	50		25		ns
21	Trc	Valid Access Recover Time (Note 3)	1000		650		ns
Z8036 INTERRUPT TIMING (Figure 9)							
22	TdPM(INT)	Pattern Match to INT Delay (Bit Port)		$\overline{AS}$ cycle + 800ns		1	AS cycle + ns
23	TdACK(INT)	$\overline{ACKIN}$ to $\overline{INT}$ Delay (Port with Handshake) (Note 4)		4 $\overline{AS}$ cycles + 600ns		4	AS cycle + ns
24	TdCI(INT)	Counter Input to $\overline{INT}$ Delay (Counter Mode)		$\overline{AS}$ cycle + 700ns		1	AS cycle + ns
25	TdPC(INT)	PCLK to $\overline{INT}$ Delay (Timer Mode)		$\overline{AS}$ cycle + 700ns		1	AS cycle + ns
26	TdAS(INT)	$\overline{AS}$ to $\overline{INT}$ Delay		300			ns
Z8036 INTERRUPT ACKNOWLEDGE TIMING (Figure 10)							
27	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	0		0		ns
28	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250		250		ns
29	TsAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ (Acknowledge) ↓ Setup Time (Note 5)	350		250		ns
30	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Data Valid Delay		250		180	ns
31	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	390		250		ns
32	TdAS(IEO)	$\overline{AS}$ ↓ to IEO ↓ Delay ($\overline{INTACK}$ Cycle) (Note 5)		350		250	ns
33	TdIEI(IEO)	IEI to IEO Delay (Note 5)		150		100	ns
34	TsIEI(DSA)	IEI to $\overline{DS}$ (Acknowledge) ↓ Setup Time (Note 5)	100		70		ns
35	ThIEI(DSA)	IEI to $\overline{DS}$ (Acknowledge) ↑ Hold Time	100		70		ns
36	TdDSA(INT)	$\overline{DS}$ (Acknowledge) ↓ to $\overline{INT}$ ↑ Delay		600		600	ns

Notes:
1. Parameters do not apply to Interrupt Acknowledge transactions.
2. Float Delay is measured to the time when the output has changed 0.5V from steady state with minimum AC load and maximum DC load.
3. This is the delay from $\overline{DS}$↑ of one CIO access to $\overline{DS}$↓ of another CIO access.
4. The delay is from $\overline{DAV}$↓ for 3-Wire Input Handshake. The delay is from DAC↑ for 3-Wire Output Handshake. One additional $\overline{AS}$ cycle is required for ports in the Single Buffered mode.
5. The parameters for the devices in any particular daisy chain must meet the following constraints: the delay from $\overline{AS}$↑ to $\overline{DS}$↓ must be greater than the sum of TdAS(IEO) for the highest priority peripheral, TsIEI(DSA) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.

*Timings are all preliminary and subject to change. All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0".

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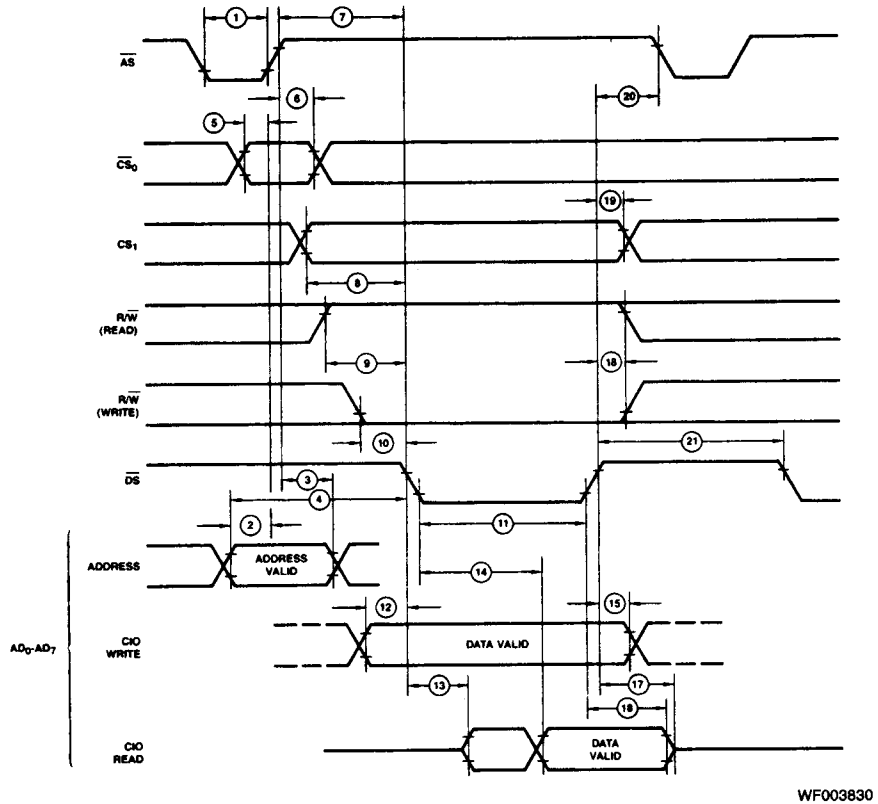

Figure 8. Z8036 CPU Interface Timing

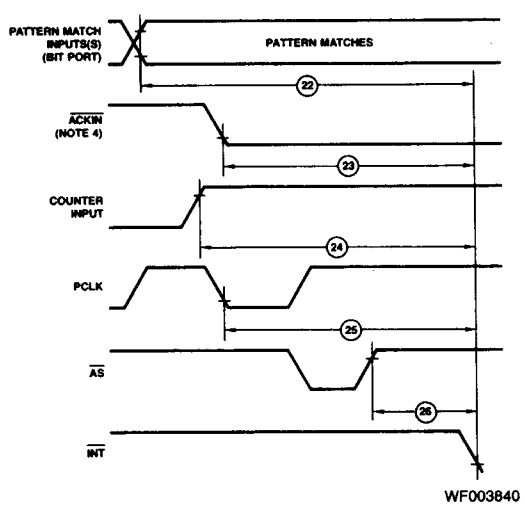

Figure 9. Z8036 Interrupt Timing

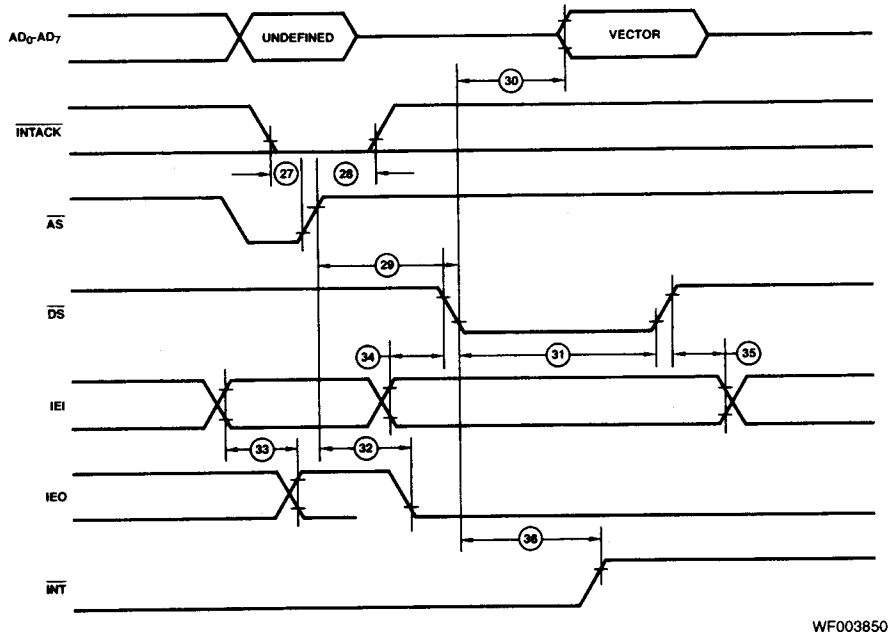

Figure 10. Z8036 Interrupt Acknowledge Timing

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Z8536 CPU INTERFACE TIMING (Figure 11)

Number	Parameters	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TcPC	PCLK Cycle Time	250	4000	165	4000	ns
2	TwPCh	PCLK Width (High)	105	2000	70	2000	ns
3	TwPCl	PCLK Width (Low)	105	2000	70	2000	ns
4	TrPC	PCLK Rise Time		20		10	ns
5	TfPC	PCLK Fall Time		20		15	ns
6	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Setup Time	100		100		ns
7	ThIA(PC)	$\overline{INTACK}$ to PCLK ↑ Hold Time	0		0		ns
8	TsIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Setup Time (Note 1)	200		200		ns
9	ThIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0		0		ns
10	TsIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Setup Time	200		200		ns
11	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0		0		ns
12	TsA(RD)	Address to $\overline{RD}$ ↓ Setup Time	80		80		ns
13	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0		0		ns
14	TsA(WR)	Address to $\overline{WR}$ ↓ Setup Time	80		80		ns
15	ThA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0		0		ns
16	TsCEl(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time (Note 1)	0		0		ns
17	TsCEh(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Setup Time (Note 1)	100		70		ns
18	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time (Note 1)	0		0		ns
19	TsCEl(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time	0		0		ns
20	TsCEh(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Setup Time	100		70		ns
21	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ Hold Time	0		0		ns
22	TwRDl	$\overline{RD}$ Low Width (Note 1)	390		250		ns
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0		0		ns
24	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay		250		180	ns
25	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0		0		ns
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay (Note 2)		70		45	ns
27	TwWRl	$\overline{WR}$ Low Width	390		250		ns
28	TsDW(WR)	Write Data to $\overline{WR}$ ↓ Setup Time	0		0		ns
29	ThDW(WR)	Write Data To $\overline{WR}$ ↑ Hold Time	0		0		ns
30	Trc	Valid Access Recovery Time (Note 3)	1000*		650*		ns
Z8536 INTERRUPT TIMING (Figure 12)							
31	TdPM(INT)	Pattern Match to $\overline{INT}$ Delay (Bit Port)		2		2	TcPC + ns
32	TdACK(INT)	$\overline{ACKIN}$ to $\overline{INT}$ Delay (Port with Handshake) (Note 4)		10		10	TcPC + ns
33	TdCl(INT)	Counter Input to $\overline{INT}$ Delay (Counter Mode)		2		2	TcPC + ns
34	TdPC(INT)	PCLK to $\overline{INT}$ Delay (Timer Mode)		3		3	TcPC + ns

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SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Z8536 INTERRUPT ACKNOWLEDGE TIMING (Figure 13)

Number	Parameters	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
35	TsIA(RDA)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Setup Time (Note 5)	350		250		ns
36	TwRDA	$\overline{RD}$ (Acknowledge) Width	350		250		ns
37	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay		255		180	ns
38	TdIA(IEO)	$\overline{INTACK}$ ↓ to IEO↓ Delay (Note 5)		350		250	ns
39	TdIEI(IEO)	IEI to IEO Delay (Note 5)		150		100	ns
40	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Setup Time (Note 5)	100		70		ns
41	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time	100		70		ns
42	TdRDA(INT)	$\overline{RD}$ ↓ (Acknowledge) to $\overline{INT}$ ↑ Delay		600		600	ns

Notes: 1. Parameters do not apply to Interrupt Acknowledge transactions.
2. Float Delay is measured to the time when the output has changed 0.5V with minimum AC load and maximum DC load.
3. Trc is 1μs or 3 TcPC, whichever is longer.
4. The delay is from $\overline{DAV}$↓ for 3-Wire Input Handshake. The delay is from DAC↑ for 3-Wire Output Handshake.
5. The parameters for the devices in any particular daisy chain must meet the following constraints: the delay from $\overline{INTACK}$↓ to $\overline{RD}$↓ must be greater than the sum of TdIA(IEO) for the highest priority peripheral, TsIEI(RDA) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.

*Timings are preliminary and subject to change.

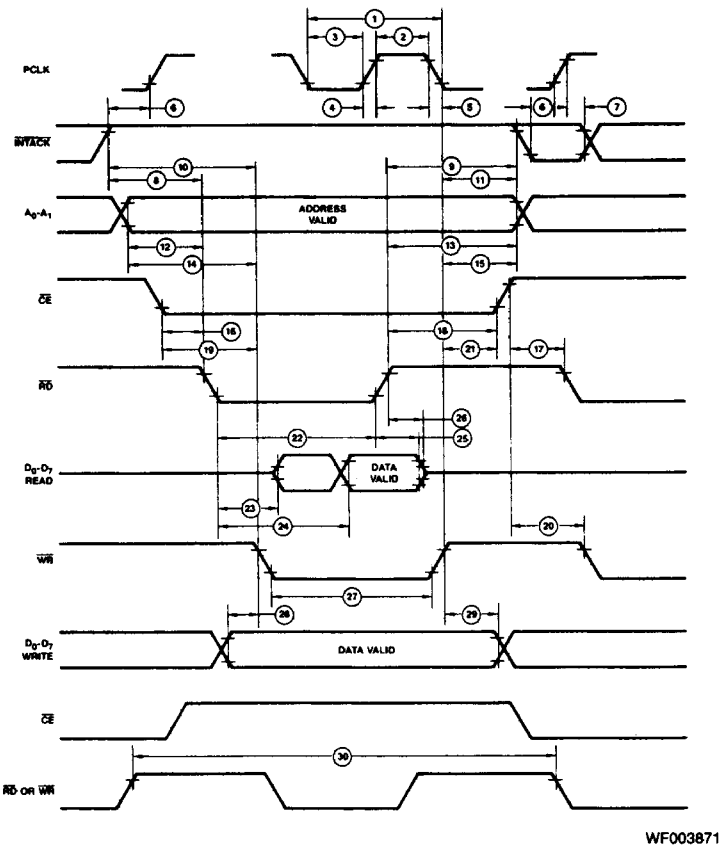

Figure 11. Z8536 CPU Interface Timing

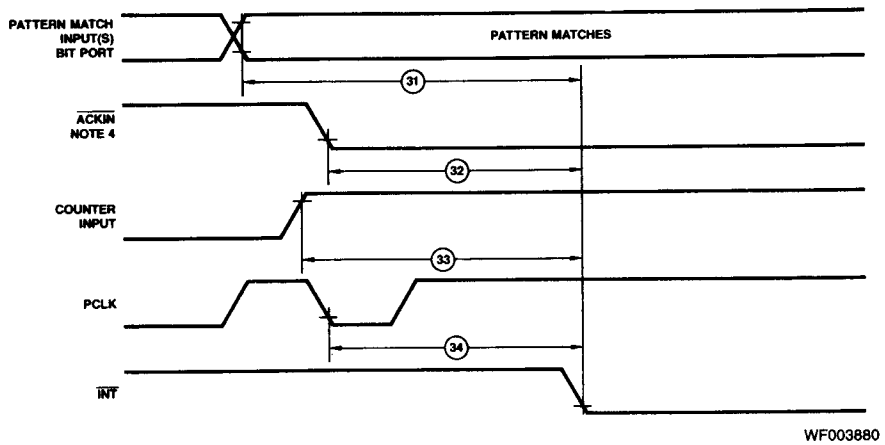

Figure 12. Interrupt Timing

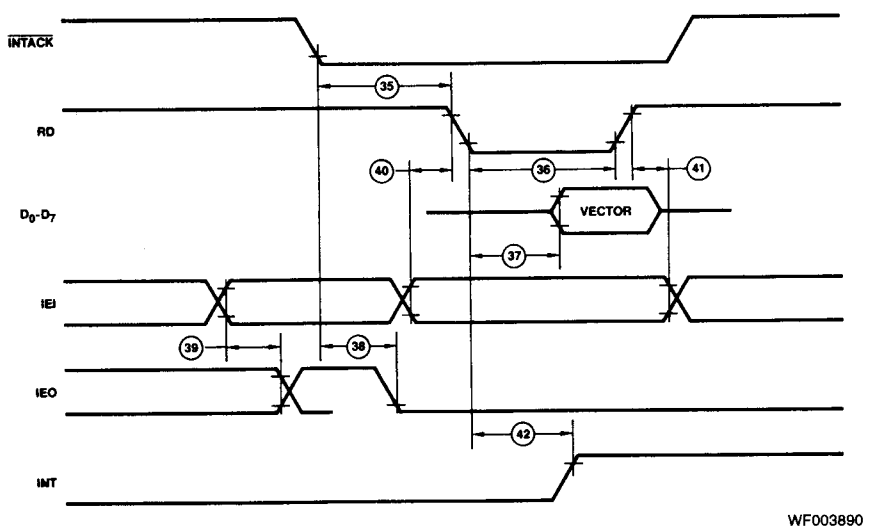

Figure 13. Interrupt Acknowledge Timing

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Z8036 REQUEST/$\overline{\text{WAIT}}$ TIMING (Figure 14)

Number	Parameters	Description	4MHz		Units
			Min	Max	
1	TdDS(REQ)	$\overline{DS}$ ↓ to REQ ↓ Delay		500	ns
2	TdDS(WAIT)	$\overline{DS}$ ↓ to $\overline{WAIT}$ ↓ Delay		500	ns
3	TdPC(REQ)	PCLK ↓ to REQ ↑ Delay		300	ns
4	TdPC(WAIT)	PCLK ↓ to $\overline{WAIT}$ ↑ Delay		300	ns
5	TdACK(REQ)	$\overline{ACKIN}$ ↓ to REQ ↑ Delay (Note 1)		3 $\overline{AS}$ + 2PCLK + 1000ns	$\overline{AS}$ cycles + PCLK cycles + ns
6	TdACK(WAIT)	$\overline{ACKIN}$ ↓ to $\overline{WAIT}$ ↑ Delay		10 PCLK + 600ns	PCLK cycles + ns

Note: 1. The delay is from $\overline{DAV}$↓ for 3-Wire Input Handshake. The delay is from DAC↑ for 3-Wire Output Handshake.
*Timings are preliminary and subject to change. All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0".

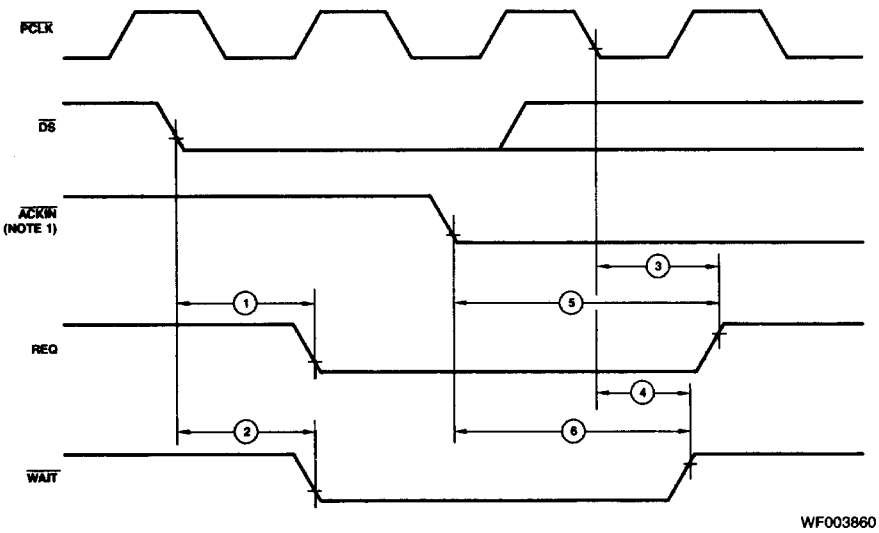

Figure 14. REQUEST/WAIT Timing

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Z8036 REQUEST/$\overline{\text{WAIT}}$ TIMING (Figure 15)

Number	Parameters	Description	4MHz		Units
			Min	Max	
1	TdRD(REQ)	$\overline{RD}$ ↓ to REQ ↓ Delay		500	ns
2	TdRD(WAIT)	$\overline{RD}$ ↓ to $\overline{WAIT}$ ↓ Delay		500	ns
3	TdWR(REQ)	$\overline{WR}$ ↓ to REQ ↓ Delay		500	ns
4	TdWR(WAIT)	$\overline{WR}$ ↓ to $\overline{WAIT}$ ↓ Delay		500	ns
5	TdPC(REQ)	PCLK ↓ to REQ ↑ Delay		300	ns
6	TdPC(WAIT)	PCLK ↓ to $\overline{WAIT}$ ↑ Delay		300	ns
7	TdACK(REQ)	$\overline{ACKIN}$ ↓ to REQ ↑ Delay (Note 1)		8 + 100	TcPC + ns
8	TdACK(WAIT)	$\overline{ACKIN}$ ↓ to $\overline{WAIT}$ ↑ Delay (Note 1)		10 + 600	TcPC + ns

Note: 1. The delay is from $\overline{DAV}$↓ for 3-Wire Input Handshake. The delay is from DAC↑ for 3-Wire Output Handshake.
*Timings are preliminary and subject to change. All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0".

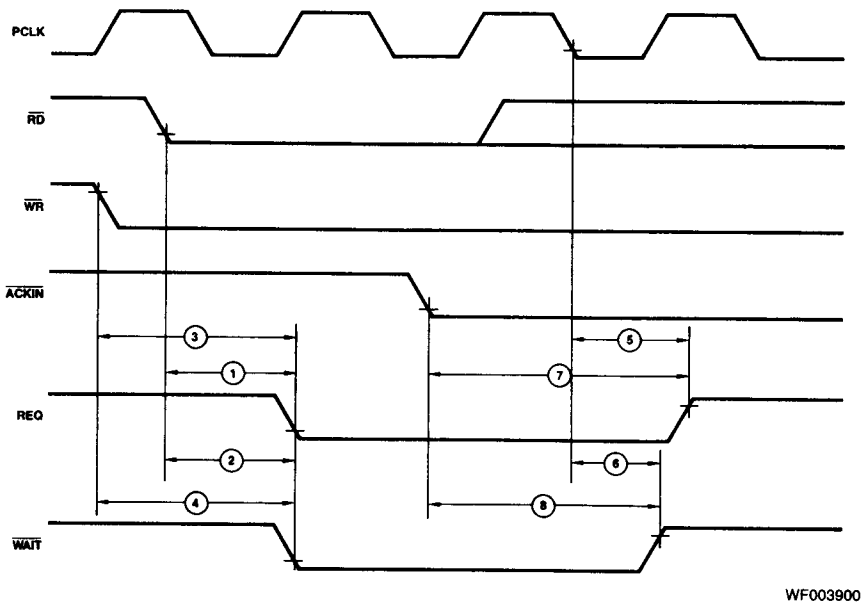

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Figure 15. Request/$\overline{\text{WAIT}}$ Timing