VL7C212A

300/1200 BIT-PER-SECOND MODEM

FEATURES

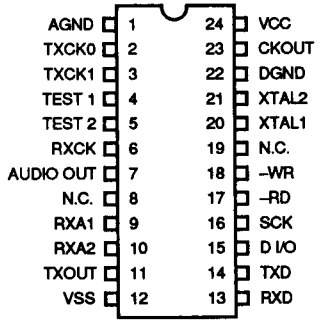
- FSK and PSK modulators and demodulators, high-band and low-band filters with compromise amplitude and group delay equalizers
- Built-in call progress mode and tone generators for DTMF V.21 and V.22 guard tones
- Bell 212A and CCITT V.21 and V.22 compatible; V.22 notch filters included
- Serial control interface
- Programmable audio output port
- Analog, digital, and remote digital loopback capabilities
- 24-pin DIP and 28-pin plastic leaded chip carrier available
- High level of integration provides a highly cost effective 300/1200 bit-per- second modems
- Eliminates external components, easing design of intelligent modems
- Usable in North American and European modem designs
- Simple board layout
- Simple speaker interface for monitoring phone line
- Testable signal path
- Reduced board area
- Direct replacement for Sierra SC11004 and SC11014

DESCRIPTION

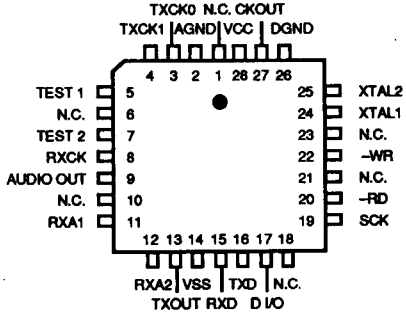
The VL7C212A is a complete 300/1200 bit-per-second modem. All of the signal processing functions needed for a full duplex, 300/1200 bit-per-second 212A (V.21 or V.22) modem, including both FSK and PSK modulators and demodulators and the high-band and low-band filters, are integrated on a single chip. It is built using a three-micron CMOS double-polysilicon process that allows analog and digital functions to be combined on the same chip. This design includes capabilities for progress monitoring and for generating DTMF as well as V.21 or V.22 guard tones. The two-to-four wire hybrid is also included, simplifying the interface to a DAA. The VL7C212A also includes analog loopback and remote digital loopback functions for self-testing.

PIN DIAGRAMS

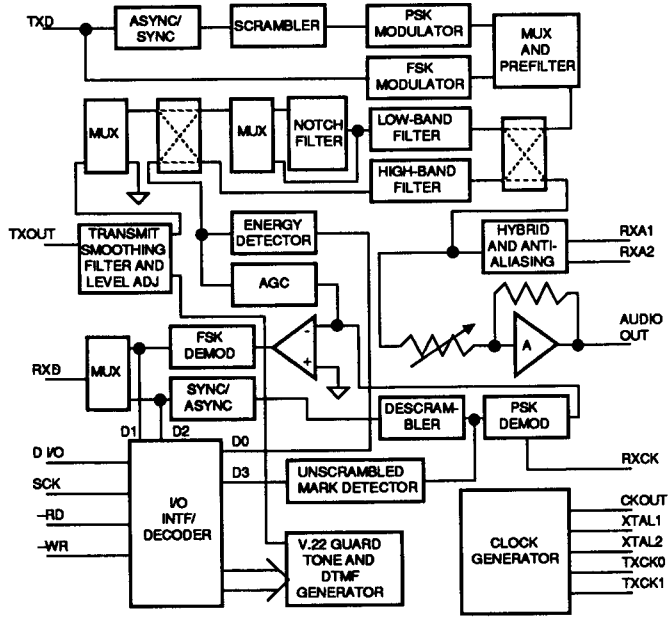
VL7C212A-PC



VL7C212A-QC



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C212A-PC	Plastic DIP
VL7C212A-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number (Note)	Signal Description
TXD	14	Transmit Data- Data on this input is modulated by the modem and output on TXOUT pin. A logic low is space and a logic high is mark.
RXD	13	Receive data- The modem demodulates the received carrier and outputs data on this pin. A logic low level is space and a logic high level is mark. The controller can force the demodulator output to the mark state by sending the code 02.
D I/O	15	Data I/O- Data is shifted in serially when WR is low on rising edges of SCK clock. Data is transferred to a latch when WR goes high. Up to seven data bits can be sent. Input codes are defined in Table 1. Data is read from the modem serially when RD is low, on rising edges of SCK clock. Up to four data bits can be read. Output codes are defined in Table 1.
–WR	18	Strobe output from the controller for shifting data to the modem.
–RD	17	Strobe output from the controller for serially reading data from the modem.
SCK	16	Serial shift clock is applied to this pin. It is normally high until data is sent to, or read from, the modem.
TXOUT	11	Transmit data carrier output.
RXA1, RXA2	9, 10	Received data carriers.
AUDIO OUT	7	Output of the hybrid is passed through a programmable attenuator and brought out on this pin. Four levels of received signal can be programmed using the control codes listed in Table 1.
XTAL1, XTAL	20, 21	Pins for connecting a 7.3728 MHz crystal. An external clock signal can be applied to the XTAL1 pin.
CKOUT	23	Buffered crystal oscillator signal is output on this pin. It can drive one LS TTL load.
TXCKO	2	Transmitter Clock Output- In high speed, synchronous internal mode, this output supplies a 1200 Hz clock to the DTE.
TXCK1	3	In high speed, synchronous external mode this pin is an input for receiving a 1200 Hz clock from the DTE.
RXCK	6	Receiver Clock Output- In high speed, synchronous, external mode, the modem supplies a 1200 Hz clock on this output.
VCC	24	+ 5 V power supply.
VSS	12	– 5 V power supply.
DGND	22	Digital ground.
AGND	1	Analog ground.
TEST1, 2	4, 5	Used by VLSI for testing. Make no connection to these pins. They must be left floating.
N.C.	8, 19	No Connect- No internal connection is made to these pins and they may be left floating.

Note: Pin numbers refer to the DIP package.

FUNCTIONAL DESCRIPTION

With the addition of a digital controller, such as an 8-bit microcontroller and a data access arrangement (DAA), a highly cost effective, integrated, intelligent modem can be built. When used with the VLSI VL7C213A modem controller, which is an 8-bit processor combined with a UART, a complete Hayes command set compatible modem can be configured, taking up a minimum of board area. For stand-alone applications, the VL7C212A modem, the VL7C213 controller, a DAA and an RS232-interface are all that are required.

The VL7C212A is truly a modem on a chip. All of the signal processing functions needed for a full duplex, 300/1200 bps Bell 212A or CCITT V.21 or V.22 modem are integrated on a single chip. It operates in a synchronous or asynchronous mode and handles 8, 9, 10, or 11 bit words.

Like all modems, the VL7C212A needs a controller to determine the mode of operation, initiate the call to the remote modem (either pulse or tone dialing), set up the handshaking sequence with the remote modem, monitor the call progress tones on the line (ringing, busy, answer tone, and voice) and switch into the data mode. A simple four-line serial data interface was designed for the VL7C212A, enabling it to work with just about any 8-bit microcontroller or microprocessor. The control lines are: DATA INPUT/OUTPUT, SHIFT CLOCK, READ and WRITE.

MODEM

Major sections of the VL7C212A modem are a transmitter, a receiver, low-band and high-band filters, a two-to-four wire hybrid, tone generators and interface logic. It also contains an energy detector that's used for detecting the carrier and call progress monitoring and an audio output for monitoring the line.

The VL7C212A modem requires plus and minus five volts and is available in a 24-pin DIP as well as a 28-pin plastic chip carrier with "J" leads for surface mount applications. The transmitter section consists of an async/sync converter, scrambler, PSK modulator. and FSK modulator. In the high speed mode (1200 bps), the PSK modulator is connected to the filter. In the low speed mode (300 bps), the FSK modulator is connected to the filter.

TRANSMITTER

Since data terminals and computers may not have the timing accuracy required for 1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 1200 Hz + 1%, –2.5%. It outputs serial data at a fixed rate of 1200 Hz +/- 0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is supplied to the D input of the shift register. Outputs from the first two stages of the shift register form the dibit that is applied to the PSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest. The high-band being centered at 2400 Hz or the low-band, centered at 1200 Hz. A 1200 bps modem actually sends two bits at a time, called a dibit; dibits are sent at 600 baud, the actual rate of transmission; 600 baud is the optimum rate that can be transmitted over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

The dibit applied to the PSK modulator produces one of four differential phase shifts of the square wave carrier signal (1200 Hz or 2400 Hz) at the 600 Hz baud rate. The resultant waveform is passed through a wave shaping circuit that performs a raised cosine function (this is the shape factor called out in the CCITT V.21 and V.22 specifications, and it also meets the Bell 212A requirement for optimum transmission). The wave shaped signal is then passed through either the low-band or high-band filter depending upon originate or answer mode selection.

For low speed operation the FSK modulator is used. It produces one of four precision frequencies depending on originate or answer mode and the 1 (mark) or 0 (space) level of the transmit data. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.21 or V.22 applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop. In the call progress monitoring mode the filter response is scaled down by 2.5, moving the center frequency to 480 Hz.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics,

producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second order low-pass switched-capacitor filter that adds the modem transmit signal to the DTMF (V.21 or V.22) guard tones. It also provides a 3 dB per step programmable gain function to set the output level.

RECEIVER

The receiver section consists of an energy detector, AGC, PSK demodulator, FSK demodulator, descrambler, and sync/async converter.

The received signal is routed through the appropriate band-pass filter and applied to both the energy detector and AGC circuit. The energy detector is based on a peak detection algorithm. It provides a detection within 17 to 24 ms. It is set to turn on when the signal exceeds -43 dBm and turn off when the signal falls below -48 dBm. A 2 dB minimum hysteresis is provided between the turn on and turn off levels.

The AGC circuit is a programmable gain amplifier that covers a range of 28 dB in seven steps. The gain is controlled by a 3 bit up/down counter. Output of the AGC amplifier is rectified and compared with two preset levels corresponding to desired high and low limits. Outputs of the comparators control the up/down counter such that the received signal is amplified to the desired level.

The PSK demodulator uses a coherent demodulation technique. Output of the AGC amplifier is applied to a dual phase splitter that produces an in-phase and 90 degree out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by the recovered carrier. The baseband components are low-pass filtered to produce I and Q (In-phase and Quadrature) channel outputs. The I and Q channel outputs are rectified, summed, and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled to produce the received dibit data. The recovered carrier for the demodulator is generated by another PLL which is controlled by the amplitude of the error signal formed by the difference of the I and Q outputs.

The descrambler is similar to the scrambler. The received dibit data is applied to the D input of a 17 bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with input data to produce received data.

In the asynchronous mode, data from the descrambler is applied to the sync/async converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are reinserted. Underspeed data is passed essentially unchanged. Output of the sync/async converter along with the output of the FSK demodulator is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed, and outputs received data on the RXD pin.

For low speed operation, the FSK demodulator is used. The output of the AGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate four times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

HYBRID

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. This matching provided by an external resistor connected between the RXA1 and RXA2 pins on the VL7C212A. The filter section provides sufficient attenuation of the out of band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter.

TONE GENERATOR

The tone generator section consists of a DTMF generator and a V.21 (or V.22) guard tone generator. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and * and # keys. The V.21 (or V.22) guard tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the Data I/O pin. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to the individual rows or column of the DTMF signal.

AUDIO OUTPUT STAGE

A programmable attenuator that can drive a load impedance of 50 KΩ is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation: no attenuation, 6 dB attenuation, 12 dB attenuation and squelch are provided through the ALC1, ALC0 and audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

VL7C213 AND VL7C214 CONTROLLERS

The VL7C213 modem controller, implemented in VLSI's two-micron CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including an 8-bit microprocessor, 8K by 8 bytes of ROM,

and 128 by 8 bytes of RAM, it also contains the functionality of a VL82C50 UART, greatly simplifying the interface to a parallel system bus, such as used in an IBM PC-compatible personal computer (PC). In fact, a complete, Hayes compatible modem for the PC consists of the VL7C213 controller, the VL7C212A modem and the DAA. All of the popular communications software written for the PC will work with the VL7C212A/VL7C213 set.

Another version of the controller, the VL7C214, is intended for RS-232 applications. It contains the same processor, memory, and UART as the VL7C213 and has the same interface to the modem chip. The difference is that the UART is turned around so that serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation. All of the switch settings can be done through software.

The VL7C214 provides a standard five volt logic level interface. RS-232 drivers are required to interface to the port. Like the VL7C213, the VL7C214 comes preprogrammed with the Hayes "AT" command set, and when used with the VL7C212A modem, emulates a Hayes-type stand-alone modem. The VL7C213 and VL7C212A emulate a Hayes-type IBM PC plug-in card modem. But the chip set is by no means limited to implementing a Hayes-type smart modem. VLSI is in the custom IC business and both chips were designed with this in mind. For example, only about 6K bytes of the VL7C213's ROM is used for the handshaking and smart modem code, leaving 2K bytes for additional features that a customer may specify. Since the controller is ROM programmable, any command set, not just the Hayes "AT" set, can be implemented.

Both the VL7C213 and VL7C214 require plus five volts and are available in either a 28-pin DIP or a 28-pin plastic chip carrier with "J" leads for surface mount applications. Besides the four-line interface for the VL7C212A modem, the VL7C213 controller has an 8-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 8250B UART. It also has control lines for ring indication, the off-hook relay and a data/voice relay; these three lines connect to the DAA.

In the VL7C214, the 8-bit port becomes the switch input lines and the address, chip select, DIST and DOST lines become the six lines for the RS-232 interface. These six lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control. The primary difference between the VL7C213 and VL7C214 is the ROM code. It also contains the same modem and DAA interface lines as the VL7C213.

The VL7C213 and VL7C214 are truly ASIC controllers. They are designed to control a modem or other peripheral that operates at a moderately slow data rate up to 1200 bits per second. The VL7C213 allows a slow peripheral to interface to a high speed bus, without making the main processor slow down.

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communication software has to have unrestrained access to the UART registers. To make the VL7C213 compatible with this software, the registers were included.

The internal processor monitors the registers to determine the mode of operation. Command mode or data mode: at power-up it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until escape sequence is three "+" signs (+++) in the default mode, but it can be changed in software.

The actual processor contains an 8-bit data path and can execute 19 instructions with five different addressing modes: direct, indirect, immediate, register direct, and register indirect. There is 8K by 8 of ROM on-chip for program storage.

To the system bus, the VL7C213 looks and acts just like a VL82C50 UART. All of the communications software written for this UART will work with the VL7C213 and VL7C214. The VLSI chip set is a Hayes-type modem in two chips.

The VL7C212A AND VL7C213/VL7C214 System

The only external components required by the VL7C212A are the 600 Ω line matching resistor, a 7.3728 MHz crystal (a standard frequency) and a 20 pF capacitor from each leg of the crystal to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the VL7C212A can directly drive a high impedance (50 kΩ) earphone-type transducer.

The VL7C213 modem controller's clock in line is driven by the VL7C212A's clock out line, so only one crystal is needed. The VL7C213 interfaces directly to an IBM PC bus -- no buffers are required. The only external parts may be an eight input NAND gate for COM1 and COM2 decoding inside the PC.

For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off-hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

All modems require a DAA. A DAA (data access arrangement) is a piece of equipment required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 Ω to 600 Ω; a relay for disconnecting the modem from the line; a ring detector, typically an opto-isolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by any of many consultants and labs around the country. Another alternative is to buy a DAA, supplied by several manufacturers.

212A is a Bell specification that calls for 1200 bit per second, full or half duplex data transmission with a fallback mode

of 300 baud (Bell 103). It is not 1200 baud; the spec calls for transmission of dibits, or 2 bits per baud so the 1200 bps transmission takes place at 600 baud. The same is true for V.22; it's 1200 bps or 600 baud. V.22 does not call for a 300 baud fallback; the CCITT standard for 300 baud is V.21. It is not a required fallback for V.22, however, it is included in the VL7C212A.

V.22 also calls for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The VL7C212A modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone when in the receive mode.

All modems require a hybrid. Hybrid is a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the VL7C212A, this is done with op amps, but the separate signals (TXOUT and RXA2) are also brought out so an external hybrid can be used, if desired. The combined signal comes out on the RXA1 pin and a matching resistor (typically 600 Ω) is connected between RXA1 and RXA2.

TABLE 1. DEFINITION OF I/O CODES

1. Instructions to the modem IC

Data on the D I/O pin is shifted into the modem when WR is low, on rising edges of the SCK clock. Data is transferred into a latch when WR goes high. (See Figure 2 for write cycle waveforms.) Up to seven data bits (D0--D6) can be sent to the device. These bits control the operating modes of the modem as show below:

D6	D5	D4	D3-D0	Mode/Function
				Non-Tone Mode:
0	1/0	0	0	Reset (set default values)
0	1/0	0	1	Tone On/Off
0	1/0	0	2	Force Receive Data to Mark Off/On
0	1/0	0	3	TLC0 Transmit Level Control Bit 0 (default 0)
0	1/0	0	4	TLC1 Transmit Level Control Bit 1 (default 0)
0	1/0	0	5	TX Transmitter On/Off
0	1/0	0	6	ALB Analog Loopback On/Off
0	1/0	0	7	CPM Call Progress Monitor Mode On/Off
0	1/0	0	8	Connection Indicator (CI) On/Off
0	1/0	0	9	ALC0 Audio Output Level Control Bit 0 (default 0)
0	1/0	0	A	ALC1 Audio Output Level Control Bit 1 (default 0)
0	1/0	0	B	WLS0 Word Length Select 0 (default 0)
0	1/0	0	C	WLS1 Word Length Select 1 (default 1)
0	1/0	0	D	Sync/Async
0	1/0	0	E	LS/HS: Low Speed/High Speed
0	1/0	0	F	A/0: Answer/Originate
0	1/0	1	0	Transmit Mark On/Off
0	1/0	1	1	Transmit Space On/Off
0	1/0	1	2	Scrambler Disable On/Off
0	1/0	1	3	DLB Digital Loopback On/Off
0	1/0	1	4	TXDP Transmit Dotting Pattern On/Off
0	1/0	1	5	Locked/Internal
0	1/0	1	6	External/Slave
0	1/0	1	7	2100 Hz Tone On/Off (Must select low speed mode for operation)
0	1/0	1	8	1300 Hz Tone On/Off (Must select low speed mode for operation)
0	1/0	1	9	V.21 On/Off (Must select low speed mode for operation)

TABLE 1. DEFINITION OF I/O CODES (Cont.)

D6	D5	D4	D3-D0	Mode/Function
				Tone Mode:
1	1/0	0	0	Dial 0
1	1/0	0	1	Dial 1
1	1/0	0	2	Dial 2
1	1/0	0	3	Dial 3
1	1/0	0	4	Dial 4
1	1/0	0	5	Dial 5
1	1/0	0	6	Dial 6
1	1/0	0	7	Dial 7
1	1/0	0	8	Dial 8
1	1/0	0	9	Dial 9
1	1/0	0	A	Dial *
1	1/0	0	B	Dial #
1	1/0	0	C	Output 550 Hz and Insert 550 Hz Notch in Low-Band Filter
1	1/0	0	D	Output 1800 Hz and Insert 1800 Hz Notch inLow-Band Filter
1	1/0	0	E	Row Disable On/Off
1	1/0	0	F	Column Disable On/Off

WLS1	WLS0	Word Length
0 0	0	8 Bits
0 1	1	9 Bits
1 0	0	10 Bits (default)
1 1	1	11 Bits

TLC1	TLC0	Transmitter Output Level (dBm) at the Phone Line
0 0	0	–12 (default)
0 1	1	–9
1 0	0	–6
1 1	1	0

ALC1	ALC0	Audio Output Level
0 0	0	Output Off (default)
0 1	1	12 dB Attenuation
1 0	0	6 dB Attenuation
1 1	1	No Attenuation

2. Information from the Modem IC

Data is read serially from the modem when RD is low, on rising edges of the SCK clock. (See Figure 1 for read cycle waveforms.) Up to four data bits (D0--D3) can be read as defined below:

D0	Energy Detect	0 - No Energy	1 - Energy Present

In the CPM mode, the energy detector is connected to the output of the high-band filter, if ALB is off, or the scaled low-band filter, if ALB is on.

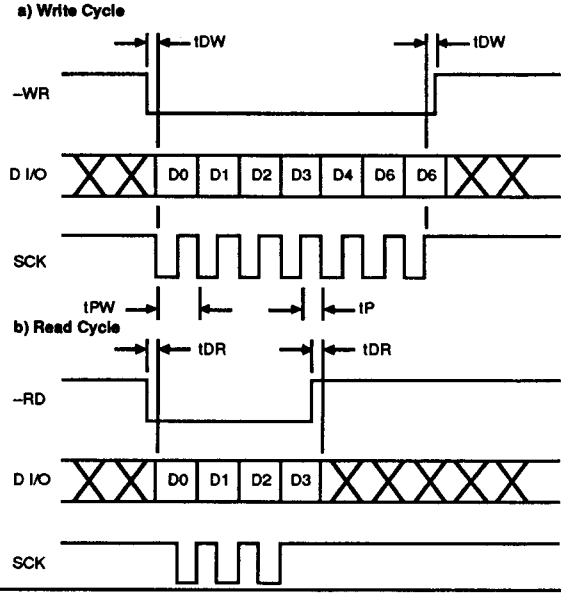
D1	Received Data (FSK)	1 - Mark	0 - Space
D2	Received Data (PSK)	1 - Mark	0 - Space
D3	Unscrambled Mark	1 - Detected	0 - Not Detected

Notes:
1. Default values for the operating modes on power-up are those shown to the right of the "/" unless otherwise specified.
2. Data is shifted in and out of the modem with LSB first.

TABLE 2. AC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
tDW	Delay Time to Write	200			ns	
tDR	Delay Time to Read	200			ns	
tPW	Complete SCK Cycle	1.0			ms	
tP	SCK High Pulse Duration	30		70	%	Duty Cycle
fC	Crystal Frequency	7.3721	7.3728	7.3735	MHz	

FIGURE 1. WAVEFORMS FOR WRITE AND READ CYCLES



DTMF GENERATOR CRYSTAL FREQUENCY = 7.372800 MHz ±0%

Parameter	Nominal Frequency	Allowable Error	Actual Error
Row 1	697 Hz	± 1%	+ 0.17%
Row 2	770 Hz	± 1%	– 0.26%
Row 3	852 Hz	± 1%	+ 0.16%
Row 4	941 Hz	± 1%	– 0.47%
Column 1	1209 Hz	± 1%	– 0.74%
Column2	1336 Hz	± 1%	–0.89%
Column 3	1477 Hz	± 1%	– 0.01%
Guard Tones	550 Hz	± 20 Hz	– 1.4 Hz
	1800 Hz	± 20 Hz	+ 7 Hz

DTMF GENERATOR (Cont.)

Parameter	Conditions	Min	Typ	Max	Units
Second Harmonic Distortion	VCC = + 5 V		– 40		dB
Row Output Level	VSS = – 5 V		0		dBm
Column Output Level	TLC0 = 1		2		dBm
550 Hz Guard Tone Level	TLC1 = 1		– 3		dB (Note 2)
1800 Hz Guard Tone Level	Measured at TXOUT Pin		– 6		dB (Note 2)

Note: Guard tone levels are referenced to the TX signal level. When guard tones are added, the TXOUT level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is –0.97 dB; for 550 Hz, the adjustment is –1.76 dB, per the CCITT specification.

MODEM TRANSMIT SIGNALS CRYSTAL FREQUENCY = 7.372800 MHz ±0%

Mode		Bell 103		CCITT V.21		Bell 212A / CCITT V.22	
		Nominal	Actual	Nominal	Actual	Nominal	Actual
Answer	Mark	2225 Hz	2226 Hz	1650 Hz	1649.4 Hz	2400 Hz	2400 Hz
	Space	2025 Hz	2024.4 Hz	1850 Hz	1850.6 Hz		
Originate	Mark	1270 Hz	1269.4 Hz	980 Hz	978.34 Hz	1200 Hz	1200 Hz
	Space	1070 Hz	1070.4 Hz	1180 Hz	1181.53 Hz		
Calling Tone				1300 Hz	1301.7 Hz	1300 Hz	1301.7 Hz
Answer Tone				2100 Hz	2096.9 Hz	2100 Hz	2096.9 Hz

RECEIVER

Parameter	Conditions	Min	Typ	Max	Units
Input Signal Range	At RXA1 (pin 9)	– 45		0	dBm
Intra - Character Bit Rate	At RXD (pin 13)	1170	1200	1224	bps
Carrier Detect	At RXA1 (pin 9)	– 48		– 43	dBm
Carrier Detect Hysterisis		2			dB
Carrier Detect Delay	For 103, 212A and V.22	10	20	30	ms
Carrier Detect Hold	For 103, 212A and V.22	15	20	24	ms
Carrier Detect Delay	For V.21 mode	15	30	40	ms
Carrier Detect Hold	For V.21 mode	20	30	50	ms

TRANSMITTER

Parameter	Conditions	Min	Typ	Max	Units
Input Character Length	Start Bit + Data Bit + Stop Bit	8		11	bits
Intra - Character Bit Rate	At TXD (pin 14)	1170	1200	1212	bps
Input Break Sequence Length	M = Character Length	2M + 3			bits
Output Level Tolerance			± 1		dB

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
Under Bias: –10°C to +80°C

Storage Temperature
Range: –65°C to +140°C

Maximum Supply
Voltage: VCC = +7.0 V, VSS = –7.0 V

Input Voltage Range:
Analog Pins; VSS –0.6 V to VCC+0.6 V
Digital Pins; DGND–0.6 V to VCC+0.6 V

Maximum Power
Dissipation @25°C: 500 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional Operation of this device at these or any other conditions above those in the operational sections of this specification is not implied and exposure to absoute maximum rating conditions for extended periods may effect device reliability.

DC CHARACTERISTICS TA= 0°C to 70° C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VCC	Positive Supply Voltage	4.5	5.0	5.5	V	
VSS	Negative Supply Voltage	–4.5	–5.0	–5.5	V	
ICC	Quiescent Current		15		mA	VCC = 5 V
ISS	Quiescent Current			15	mA	VSS = –5 V
VIH	High Level Input Voltage	2.0			V	Digital Signal Pins: –RD, –WR, DI/O, SCK,TXCK1,TXD
VIL	Low Level Input Voltage			0.8	V	Digital Signal Pins:–RD, –WR, DI/O, SCK, TXCK1, TXD
VOH	High Level Output Voltage	4.0 2.0			V V	@IOH= 40 µA (D S Pins: D I/O, CKOUT, @IOH= 500 µA RXD, TXCK0, RXCK)
VOL	Low Level Output Voltage			0.4	V	@IOL=160 µA (D S Pins: D I/O, CKOUT, RXD, TXCK0, RXCK)
VOM	Maximum Output Signal	4.0			Vp-p	TXOUT, RL=1200 Ω (TLC1=1, TLC0=0)
VOM	Maximum Output Signal	1.0			Vp-p	Audio Out, RL= 50 kΩ
VIM	Maximum Input Signal			2.0	Vp-p	RXA1, RXA2