*September 1990*
*Edition 1.0*

FUJITSU

*DATA SHEET*

# *MB98A608A-25/609A-25/610A-25*
# *EPROM MEMORY CARD*

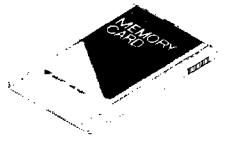
## UV ERASABLE READ ONLY MEMORY CARD
## 256K/512K/1M-BYTE

The Fujitsu MB98A608A, MB98A609A and MB98A610A are UV Erasable Read Only Memory (EPROM) cards capable of storing and retrieving large amounts of data. Each EPROM card contains multiple MBM27C1001 devices.

The EPROM memory circuits are housed in a credit-card sized 68-pin package. Internal circuitry is protected by metal plates on the top and bottom of the card to help reduce chip damage from electro-static discharge.

A unique feature of the Fujitsu memory cards allows the user to organize the card into either an 8-bit or a 16-bit organization. All cards are portable and operate at high speed with low power needs.

- Card Dimensions: 85.6 length x 54.0 width x 4.05 thickness (mm)
- Connector Type: Two-piece 68-pin (Built-in 68-pin receptacle, 2-row type)
- Complete static operation: No clock required
- TTL compatible inputs/outputs
- Three-state outputs
- Single + 5.0 V ±5% power supply




**CRD–68P–M03**

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### AVAILABLE ORGANIZATIONS

| Part Number | Mounted Memory Device | Access Time | Memory Organization * |
|---|---|---|---|
| MB98A608A–25 | MBM27C1001 x 2 pcs | 250 ns | 256K x 8 bits/128K x 16 bits |
| MB98A609A–25 | MBM27C1001 x 4 pcs | 250 ns | 512K x 8 bits/256K x 16 bits |
| MB98A610A–25 | MBM27C1001 x 8 pcs | 250 ns | 1 M x 8 bits/512K x 16 bits |

* To be configured by user.

### ABSOLUTE MAXIMUM RATINGS (see NOTE.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | –0.3 to +7.0 | V |
| Input Voltage | $V_{IN}$ | –0.5 to $V_{CC}$ +0.5 | V |
| Output Voltage | $V_{I/O}$ | –0.5 to $V_{CC}$ +0.5 | V |
| Programming Voltage | $V_{CC}/V_{PP1}$, $V_{CC}/V_{PP2}$ | –0.5 to +13.5 | V |
| Temperature under Bias | $T_{BIAS}$ | –10 to +60 | °C |
| Storage Temperature | $T_{STG}$ | –30 to +70 | °C |

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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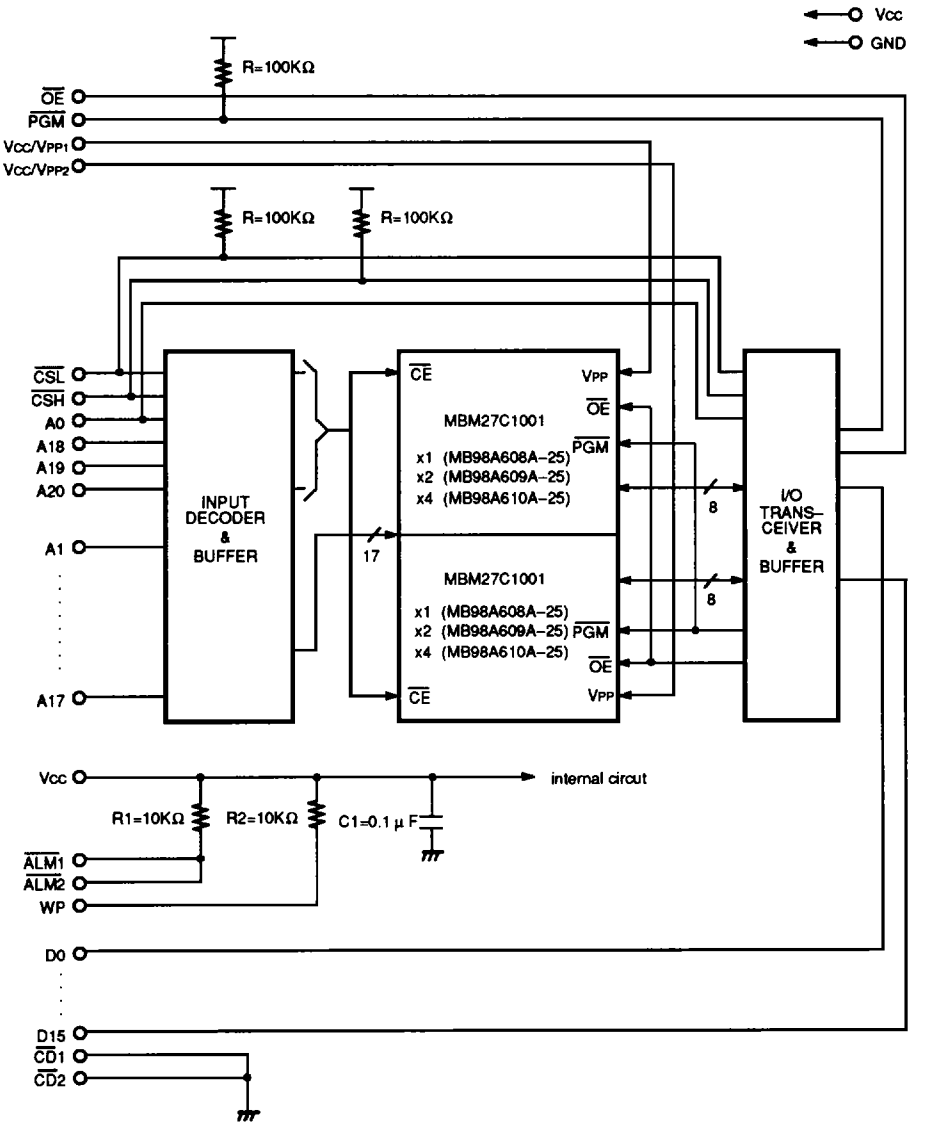
**Fig. 1 — MB98A608A/609A/610A BLOCK DIAGRAM**



# PIN DESCRIPTION

| Symbol | Pin Name | Input/Output | Function |
|---|---|---|---|
| A0 to A20 | Address Input | Input | Address Inputs, A0–A20 |
| D0 to D15 | Data Input/Output | Input/Output | Data Inputs/Outputs<br>This data bus size (8–bit or 16–bit) selected with $\overline{CSL}$ and $\overline{CSH}$. |
| $\overline{CSL}$ | Chip Select for Lower Byte | Input | Active Low<br>–Lower byte (D0–D7) is selected for read/write function.<br>(Refer to FUNCTION TRUTH TABLE.) |
| $\overline{CSH}$ | Chip Select for Upper Byte | Input | Active Low<br>–Upper byte (D8–D15) is selected for read/write function.<br>(Refer to FUNCTION TRUTH TABLE.) |
| $\overline{OE}$ | Output Enable | Input | Active Low<br>–Output enable for EPROM cards |
| $\overline{PGM}$ | Programming Enable | Input | Active Low<br>–Programming enable for EPROM cards |
| $V_{CC}/V_{PP1}$ | Power Supply/Programming Voltage 1 | Input | $V_{CC}$<br>–Power supply voltage for lower byte<br>Active $V_{PP}$<br>–Programming voltage for lower byte |
| $V_{CC}/V_{PP2}$ | Power Supply/Programming Voltage 2 | Input | $V_{CC}$<br>–Power supply voltage for upper byte<br>Active $V_{PP}$<br>–Programming voltage for upper byte |
| $\overline{CD1}$, $\overline{CD2}$ | Card Detect | Output | These pins detect if the card has been correctly inserted. Both pins are tied to GND internally. |
| WP | Write Protect | Output | This pin outputs high level for programmed OTP ROM cards and low level for blank cards. |
| $\overline{ALM1}$, $\overline{ALM2}$ | Battery Alarm | Output | Both pins are tied to Vcc internally. |
| Vcc | Power Supply | – | Power Supply Voltage (+5.0V ±5%) |
| GND | Ground | – | System Ground |
| NC | Non Connection | – | |

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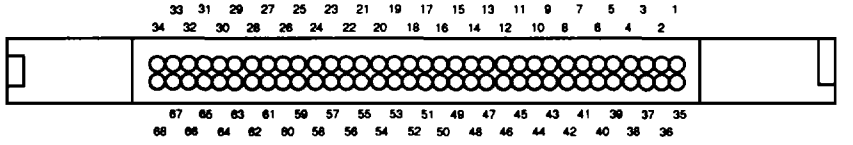
# PIN ASSIGNMENTS

| MB98A608A | MB98A609A | MB98A610A | Pin No. | | MB98A608A | MB98A609A | MB98A610A |
|---|---|---|---|---|---|---|---|
| GND | GND | GND | 1 | 35 | GND | GND | GND |
| D3 | D3 | D3 | 2 | 36 | $\overline{CD1}$ | $\overline{CD1}$ | $\overline{CD1}$ |
| D4 | D4 | D4 | 3 | 37 | D11 | D11 | D11 |
| D5 | D5 | D5 | 4 | 38 | D12 | D12 | D12 |
| D6 | D6 | D6 | 5 | 39 | D13 | D13 | D13 |
| D7 | D7 | D7 | 6 | 40 | D14 | D14 | D14 |
| $\overline{CSL}$ | $\overline{CSL}$ | $\overline{CSL}$ | 7 | 41 | D15 | D15 | D15 |
| A10 | A10 | A10 | 8 | 42 | $\overline{CSH}$ | $\overline{CSH}$ | $\overline{CSH}$ |
| $\overline{OE}$ | $\overline{OE}$ | $\overline{OE}$ | 9 | 43 | NC | NC | NC |
| A11 | A11 | A11 | 10 | 44 | NC | NC | NC |
| A9 | A9 | A9 | 11 | 45 | NC | NC | NC |
| A8 | A8 | A8 | 12 | 46 | A17 | A17 | A17 |
| A13 | A13 | A13 | 13 | 47 | A18 * | A18 | A18 |
| A14 | A14 | A14 | 14 | 48 | A19 * | A19 * | A19 |
| $\overline{PGM}$ | $\overline{PGM}$ | $\overline{PGM}$ | 15 | 49 | A20 * | A20 * | A20 * |
| NC | NC | NC | 16 | 50 | NC | NC | NC |
| Vcc | Vcc | Vcc | 17 | 51 | Vcc | Vcc | Vcc |
| $V_{CC}/V_{PP1}$ | $V_{CC}/V_{PP1}$ | $V_{CC}/V_{PP1}$ | 18 | 52 | $V_{CC}/V_{PP2}$ | $V_{CC}/V_{PP2}$ | $V_{CC}/V_{PP2}$ |
| A16 | A16 | A16 | 19 | 53 | NC | NC | NC |
| A15 | A15 | A15 | 20 | 54 | NC | NC | NC |
| A12 | A12 | A12 | 21 | 55 | NC | NC | NC |
| A7 | A7 | A7 | 22 | 56 | NC | NC | NC |
| A6 | A6 | A6 | 23 | 57 | NC | NC | NC |
| A5 | A5 | A5 | 24 | 58 | NC | NC | NC |
| A4 | A4 | A4 | 25 | 59 | NC | NC | NC |
| A3 | A3 | A3 | 26 | 60 | NC | NC | NC |
| A2 | A2 | A2 | 27 | 61 | NC | NC | NC |
| A1 | A1 | A1 | 28 | 62 | $\overline{ALM1}$ | $\overline{ALM1}$ | $\overline{ALM1}$ |
| A0 | A0 | A0 | 29 | 63 | $\overline{ALM2}$ | $\overline{ALM2}$ | $\overline{ALM2}$ |
| D0 | D0 | D0 | 30 | 64 | D8 | D8 | D8 |
| D1 | D1 | D1 | 31 | 65 | D9 | D9 | D9 |
| D2 | D2 | D2 | 32 | 66 | D10 | D10 | D10 |
| WP | WP | WP | 33 | 67 | $\overline{CD2}$ | $\overline{CD2}$ | $\overline{CD2}$ |
| GND | GND | GND | 34 | 68 | GND | GND | GND |

**Note:** A18, A19 and A20 pins asterisked " * " are non connection.

# PIN LOCATIONS

Fig. 2 – BOTTOM VIEW (CONNECTOR SIDE)

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# FUNCTION TRUTH TABLE

| $\overline{CSH}$ | $\overline{CSL}$ | A0 | $\overline{OE}$ | $\overline{PGM}$ | $V_{CC}/V_{PP1}$ | $V_{CC}/V_{PP2}$ | Mode | Data Input/Output | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | D15–D8 | D7–D0 |
| H | H | X | X | X | 5 V | 5 V | Standby | High–Z | |
| H | L | L | L | H | 5 V | 5 V | Read (x8) | High–Z | $D_{OUT}$ ( Lower Byte ) |
| H | L | H | L | H | 5 V | 5 V | Read (x8) | High–Z | $D_{OUT}$ ( Upper Byte ) |
| H | L | L | H | L | 6 V | 12.5 V | Write (x8) | High–Z | $D_{IN}$ ( Lower Byte ) |
| H | L | H | H | L | 12.5 V | 6 V | Write (x8) | High–Z | $D_{IN}$ ( Upper Byte ) |
| L | H | X | H | L | 12.5 V | 6 V | Write (x8) | $D_{IN}$ ( Upper Byte ) | High–Z |
| L | H | X | L | H | 5 V | 5 V | Read (x8) | $D_{OUT}$ ( Upper Byte ) | High–Z |
| L | L | X | L | H | 5 V | 5 V | Read (x16) | $D_{OUT}$ | |
| L | L | X | H | L | 12.5 V | 12.5 V | Write (x16) | $D_{IN}$ | |
| X | X | X | H | L | 5 V | 5 V | Output Disable | High–Z | |

Definition: H = $V_{IH}$, L = $V_{IL}$, X = Either $V_{IL}$ or $V_{IH}$

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### ADDRESS CONFIGURATION USING 8-BIT BUS ($\overline{CSH}$ = H, $\overline{CSL}$ = L)

| A20 to A0 | $\overline{CSH}$ | $\overline{CSL}$ | D15–D8 | D7–D0 |
|---|---|---|---|---|
| 0 0000 0000 0000 0000 0000 | H | L | High–Z | 0 Add. |
| 0 0000 0000 0000 0000 0001 | H | L | High–Z | 1 Add. |
| 0 0000 0000 0000 0000 0010 | H | L | High–Z | 2 Add. |
| 0 0000 0000 0000 0000 0011 | H | L | High–Z | 3 Add. |
| ↓ ↓ ↓ ↓ ↓ ↓ | ↓ | ↓ | ↓ ↓ | ↓ ↓ |
| 1 1111 1111 1111 1111 1100 | H | L | High–Z | 2097148 Add. |
| 1 1111 1111 1111 1111 1101 | H | L | High–Z | 2097149 Add. |
| 1 1111 1111 1111 1111 1110 | H | L | High–Z | 2097150 Add. |
| 1 1111 1111 1111 1111 1111 | H | L | High–Z | 2097151 Add. |

### ADDRESS CONFIGURATION USING 8-BIT BUS ($\overline{CSH}$ = L, $\overline{CSL}$ = H)

| A20 to A0 | $\overline{CSH}$ | $\overline{CSL}$ | D15–D8 | D7–D0 |
|---|---|---|---|---|
| 0 0000 0000 0000 0000 000X | L | H | 1 Add. | High–Z |
| 0 0000 0000 0000 0000 001X | L | H | 3 Add. | High–Z |
| 0 0000 0000 0000 0000 010X | L | H | 5 Add. | High–Z |
| 0 0000 0000 0000 0000 011X | L | H | 7 Add. | High–Z |
| ↓ ↓ ↓ ↓ ↓ ↓ | ↓ | ↓ | ↓ ↓ | ↓ ↓ |
| 1 1111 1111 1111 1111 100X | L | H | 2097145 Add. | High–Z |
| 1 1111 1111 1111 1111 101X | L | H | 2097147 Add. | High–Z |
| 1 1111 1111 1111 1111 110X | L | H | 2097149 Add. | High–Z |
| 1 1111 1111 1111 1111 111X | L | H | 2097151 Add. | High–Z |

Definition: X = Either "0" or "1". Even addresses are not available in this mode.

### ADDRESS CONFIGURATION USING 16-BIT BUS ($\overline{CSH}$ = L, $\overline{CSL}$ = L)

| A20 to A0 | $\overline{CSH}$ | $\overline{CSL}$ | D15–D8 | D7–D0 |
|---|---|---|---|---|
| 0 0000 0000 0000 0000 000X | L | L | 1 Add. | 0 Add. |
| 0 0000 0000 0000 0000 001X | L | L | 3 Add. | 2 Add. |
| 0 0000 0000 0000 0000 010X | L | L | 5 Add. | 4 Add. |
| 0 0000 0000 0000 0000 011X | L | L | 7 Add. | 6 Add. |
| ↓ ↓ ↓ ↓ ↓ ↓ | ↓ | ↓ | ↓ ↓ | ↓ ↓ |
| 1 1111 1111 1111 1111 100X | L | L | 2097145 Add. | 2097144 Add. |
| 1 1111 1111 1111 1111 101X | L | L | 2097147 Add. | 2097146 Add. |
| 1 1111 1111 1111 1111 110X | L | L | 2097149 Add. | 2097148 Add. |
| 1 1111 1111 1111 1111 111X | L | L | 2097151 Add. | 2097150 Add. |

Definition: X = Either "0" or "1".

# RECOMMENDED OPERATING CONDITIONS

**(Referenced to GND)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V |
| Programming Voltage during Read Mode | $V_{PP}$ | $V_{CC}$–0.6 | $V_{CC}$ | $V_{CC}$+0.6 | V |
| Input High Voltage | $V_{IH}$ | 2.4 | | $V_{CC}$+0.3 | V |
| Input Low Voltage | $V_{IL}$ | –0.1 | | 0.8 | V |
| Ambient Temperature | $T_A$ | 0 | | 50 | °C |

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# DC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted.)**

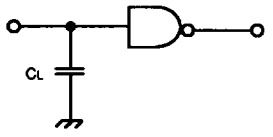
| Parameter | Test Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Standby Supply Current | $\overline{CSL}$=$\overline{CSH}$≥$V_{CC}$–0.2V | $I_{SB1}$ | | 100 | µA |
| | $\overline{CSL}$=$\overline{CSH}$=$V_{IH}$ | $I_{SB2}$ | | 10 | mA |
| Active Supply Current | $V_{IN}$=$V_{IH}$ or $V_{IL}$<br>$\overline{CSL}$=$\overline{CSH}$=$V_{IL}$, $I_{OUT}$=0mA | $I_{CC1}$ | | 100 | mA |
| Operating Supply Current | Cycle=Min.<br>Duty=100%, $I_{OUT}$=0mA | $I_{CC2}$ | | 100 | mA |
| Input Leakage Current (except $\overline{CSL}$, $\overline{CSH}$, $\overline{PGM}$) | $V_{IN}$=0V or $V_{CC}$ | $I_{LI}$ | –10 | 10 | µA |
| Output Leakage Current (except $\overline{ALM1}$, $\overline{ALM2}$, WP, $\overline{CD1}$, $\overline{CD2}$) | $\overline{V_{OUT}}$=0V or $V_{CC}$<br>$\overline{CSL}$=$\overline{CSH}$=$V_{IH}$<br>$\overline{OE}$=$V_{IH}$ or $\overline{PGM}$=$V_{IL}$ | $I_{LI/O}$ | –10 | 10 | µA |
| Output High Voltage (except $\overline{ALM1}$, $\overline{ALM2}$, WP) | $V_{OH}$=–1.0mA | $V_{OH}$ | 2.4 | | V |
| Output Low Voltage (except $\overline{CD1}$, $\overline{CD2}$) | $V_{OL}$=2.1mA | $V_{OL}$ | | 0.4 | V |

**Note:** All voltages are referenced to GND.

# CAPACITANCE ($T_A$=25°C, f=1MHz, $V_{IN}$=$V_{I/O}$=GND)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance (except $\overline{CSL}$, $\overline{CSH}$, $\overline{PGM}$) | $C_{IN}$ | | | 50 | pF |
| I/O Capacitance (except $\overline{ALM1}$, $\overline{ALM2}$, WP, $\overline{CD1}$, $\overline{CD2}$) | $C_{OUT}$ | | | 50 | pF |

**Fig. 3 – AC TEST CONDITIONS**




- Input Pulse Levels: 0.6V to 2.6V
- Input Pulse Rise & Fall Times: $t_T$ = 5ns (Transient between 0.8V and 2.4V)
- Timing Reference Levels
  Input: $V_{IL}$ = 0.8V, $V_{IH}$ = 2.4V
  Output $V_{OL}$ = 0.8V, $V_{OH}$ = 2.0V
- Output Load: 1TTL gate + $C_L$ (100pF)

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# AC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted.)**

## READ CYCLE

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Address Access Time *1 | $t_{ACC}$ | | 250 | ns |
| Chip Select Access Time | $t_{CS}$ | | 250 | ns |
| Output Enable to Output Valid *1 | $t_{OE}$ | | 120 | ns |
| Output Disable Time *2 | $t_{DF}$ | | 100 | ns |
| Output Hold Time | $t_{OH}$ | 0 | | ns |

**Note:** *1 $t_{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CSL}$, $\overline{CSH}$ without impact on $t_{ACC}$.

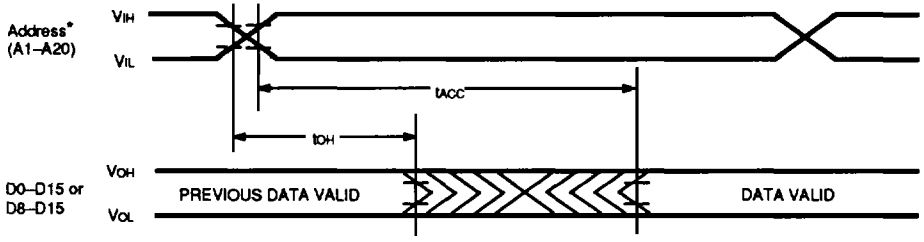
*2 $t_{DF}$ is specified from the rising edge of $\overline{OE}$, $\overline{CSL}$ or $\overline{CSH}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

# AC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted.)**

**READ CYCLE TIMING DIAGRAM ($\overline{PGM}$ = VIH)**

READ CYCLE 1: $\overline{CSL}$ = VIH, $\overline{CSH}$ = $\overline{OE}$ = VIL: x 8-bit Bus Organization
$\overline{CSL}$ = $\overline{CSH}$ = $\overline{OE}$ = VIL: x 16-bit Bus Organization

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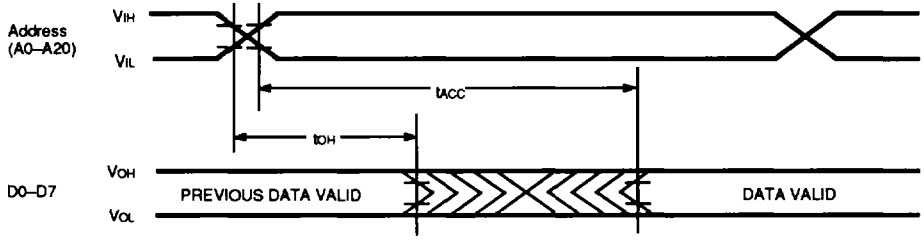
**Note:** * A0 = Either VIL or VIH.

READ CYCLE 2: $\overline{CSH}$ = VIH, $\overline{CSL}$ = $\overline{OE}$ = VIL: x 8-bit Bus Organization

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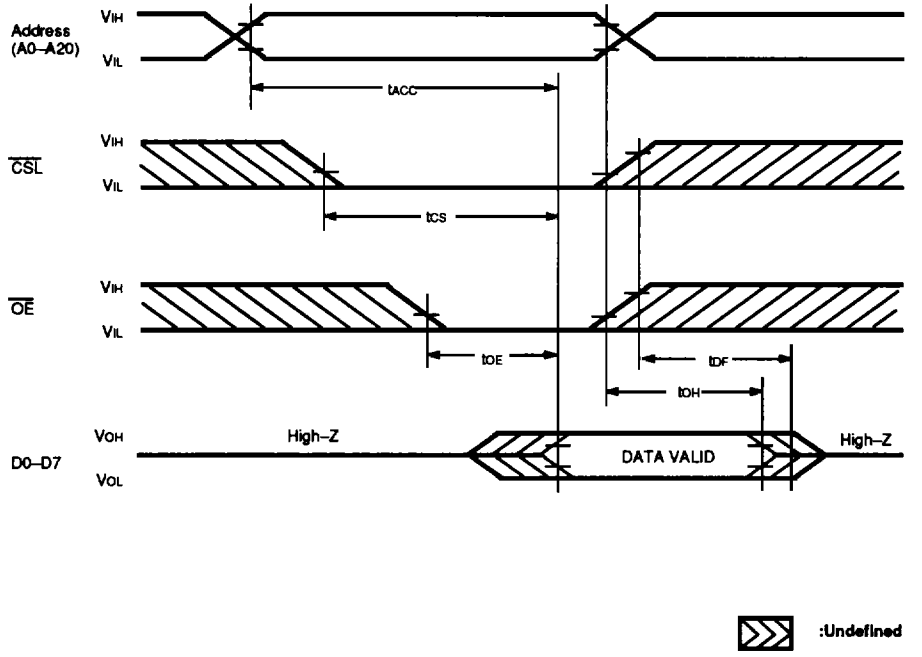
# AC CHARACTERISTICS (Continued)

**(Recommended operating conditions unless otherwise noted.)**

**READ CYCLE TIMING DIAGRAM ($\overline{PGM}$ = VIH)**

READ CYCLE 3: $\overline{CSH}$ = VIH: x 8-bit Bus Organization

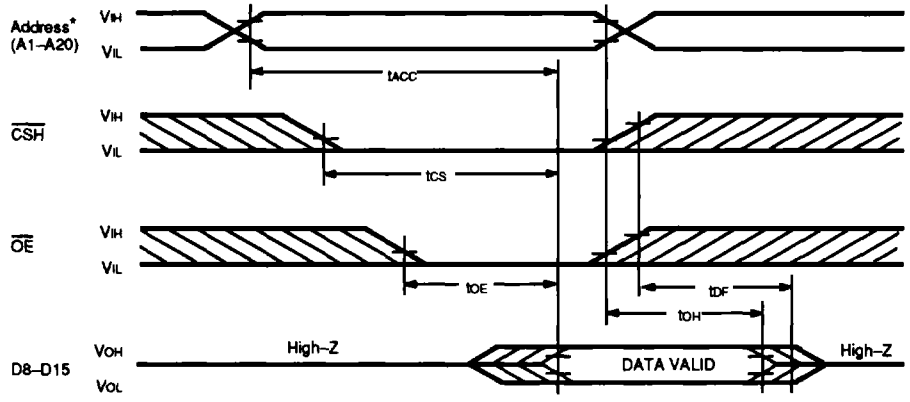


# AC CHARACTERISTICS (Continued)

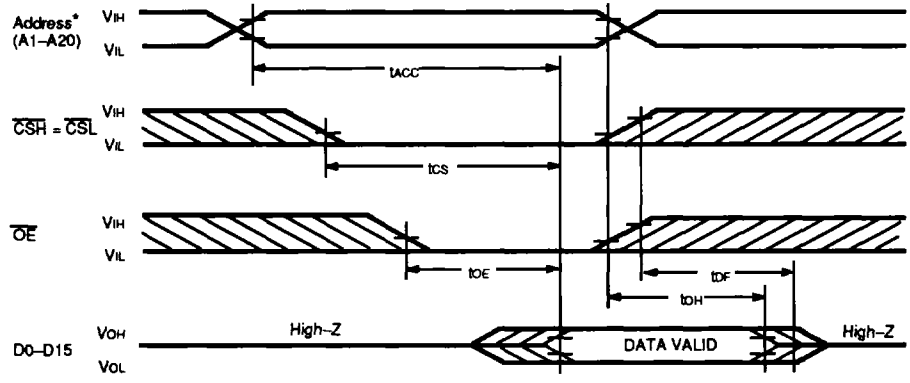
**(Recommended operating conditions unless otherwise noted.)**

**READ CYCLE TIMING DIAGRAM ($\overline{PGM}$ = VIH)**

READ CYCLE 4: $\overline{CSL}$ = VIH: x 8-bit Bus Organization




READ CYCLE 5: $\overline{CSL}$ = $\overline{CSH}$ = VIL: x 16-bit Bus Organization

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**Note:** * A0 = Either VIL or VIH.

# PROGRAMMING/ERASING INFORMATION

## PROGRAMMING

When the MB98A608A/609A/610A is shipped from the factory, all memory cells are set to the high state (logic 1). During the programming procedure, affected bit cells are set to the low state (logic 0).

When +12.5(±0.3) volts is applied to $V_{PP}$, +6(±0.25) volts is applied to $V_{CC}$, CSL (CSH)=$V_{IL}$, $\overline{OE}$ and $\overline{PGM}$=$V_{IH}$, the programming mode is initiated. Next, the proper address is input and the data pattern is applied to the input buffer. After both the address and data are stable, a 0.5–millisecond negative pulse is applied to the $\overline{PGM}$ pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulse used to accomplish a write) should be applied to $\overline{OE}$ complete word. Refer to the PROGRAMMING FLOWCHART that follows for step–by–step programming procedures.

## CAUTION

A TTL low–level voltage should not be applied to the $\overline{PGM}$ pin during the programming mode ($V_{PP}$=+12.5 volts). Also, the $V_{PP}$ voltage must not be switched from $V_{CC}$ to +12.5 volts or vice–versa. Neglecting either of these precautions may cause device failure.

## ELECTRONIC SIGNATURE

The MB98A608A/609A/610A has no electronic signature code. Therefore, more than +6 volts should not be applied to A9 pin.

## ERASING

In order to clear all memory cells of programmed contents, the MB98A608A/609A/610A must be exposed to an ultraviolet light source after taking off the cover of this card. To completely erase the memory (restore all cells to a logic 1 state), a dosage of 10Wsec/cm$^2$ is required. The required exposure can be obtained by using a UV–lamp with a wavelength of 2537 Angstroms and with an intensity of 12mW/cm$^2$. Remove all filters from the lamp and clean the transparent lid of the MB98A6xxA approximately one inch from the light source for 20–to–25 minutes.

# PROGRAMMING INFORMATION (Continued)

## DC CHARACTERISTICS ($T_A$=25°C, $V_{CC}$ *1=6V±0.25V, $V_{PP}$ *2=12.5V±0.5V)

| Parameter | Test Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Leakage Current | | $I_{LI}$ | | 10 | μA |
| $V_{PP}$ Supply Current during Programing | $\overline{CSL}$=$\overline{CSH}$=$V_{IL}$<br>$\overline{OE}$=$V_{IH}$, $\overline{PGM}$=$V_{IL}$<br>$\overline{OE}$/$V_{PP1}$=$\overline{OE}$/$V_{PP2}$=$V_{PP}$ | $I_{PP2}$ | | 100 | mA |
| $V_{PP}$ Supply Current during Programing Inhibit and Verify | $\overline{CSL}$=$\overline{CSH}$=$V_{IH}$ | $I_{PP3}$ | | 10 | mA |
| $V_{CC}$ Supply Current during Programing and Verify | | $I_{CC1}$ | | 100 | mA |
| Input High Voltage | | $V_{IH}$ | 2.4 | $V_{CC}$+0.3 | V |
| Input Low Voltage | | $V_{IL}$ | –0.1 | 0.6 | V |
| Output High Voltage | $V_{OH}$=–1.0mA | $V_{OH}$ | 2.4 | | V |
| Output Low Voltage | $V_{OL}$=2.1mA | $V_{OL}$ | | 0.45 | V |

**Note:** *1 $V_{CC}$ must be applied either coincidentally or before $V_{PP}$, and removed either coincidentally or after $V_{PP}$.

*2 $V_{PP}$ must not be greater than 13.5 volts including overshoot. Permanent device damage may occur if the card is taken out or put into programmer remaining $V_{PP}$=12.5 volts.

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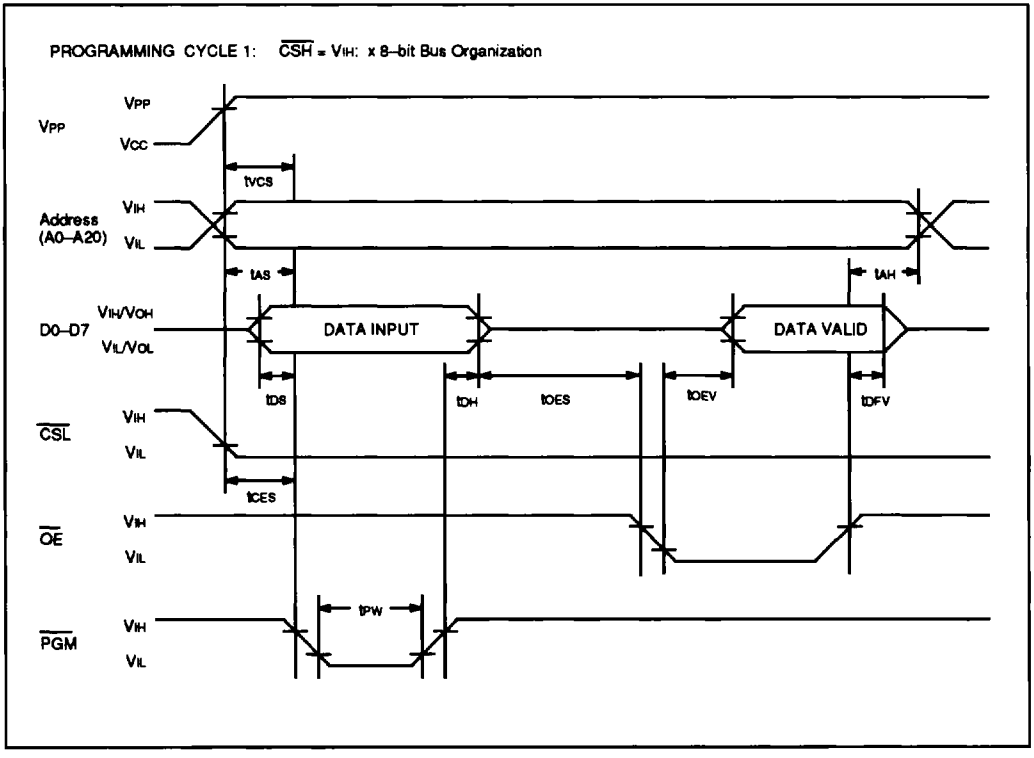
# PROGRAMMING INFORMATION (Continued)

## AC CHARACTERISTICS ($T_A$=25°C, $V_{CC}$=6V±0.25V, $V_{PP}$=12.5V±0.5V)

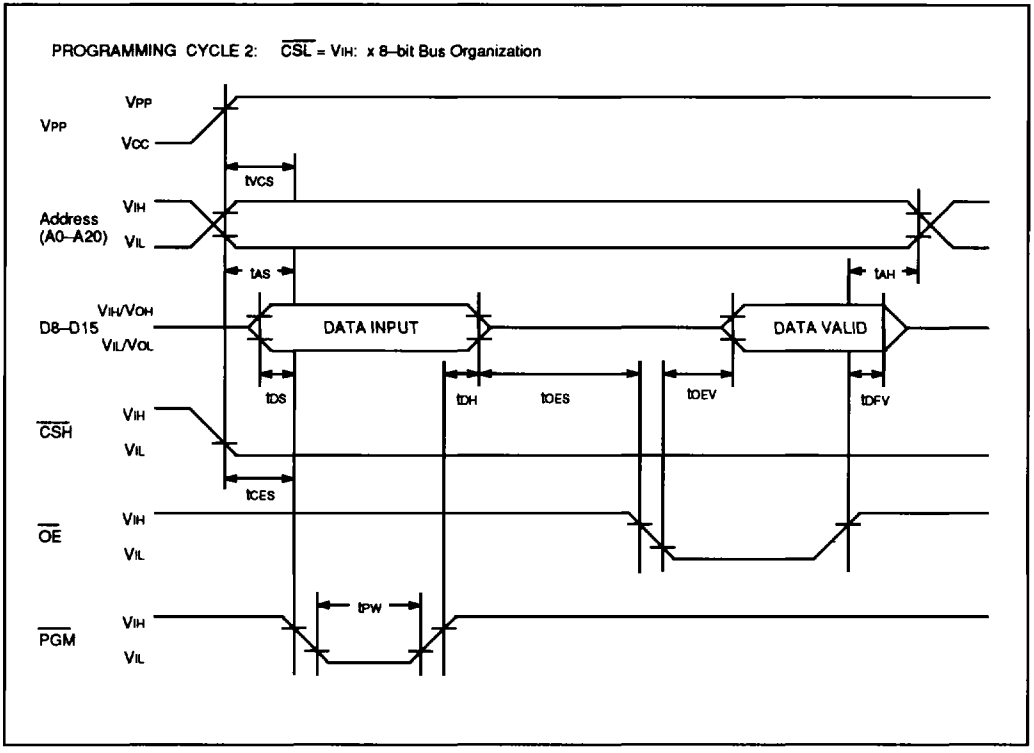
| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Address Setup Time | $t_{AS}$ | 2 | | | µs |
| Data Setup Time | $t_{DS}$ | 2 | | | µs |
| Chip Enable Setup Time | $t_{CES}$ | 2 | | | µs |
| Output Enable Setup Time | $t_{OES}$ | 2 | | | µs |
| Vcc Setup Time | $t_{VCS}$ | 2 | | | µs |
| Programming Pulse Width | $t_{PW}$ | 0.475 | 0.5 | 0.525 | ms |
| Additional Programming Pulse Width | $t_{APW}$ | 1.4 | | 39.4 | ms |
| Programming Pulse Number | N | 1 | | 25 | Times |
| Data Hold Time | $t_{DH}$ | 2 | | | µs |
| Address Hold Time | $t_{AH}$ | 2 | | | µs |
| Output Enable to Data Valid | $t_{OEV}$ | | | 500 | ns |
| Output Disable to Output Float Delay | $t_{DFV}$ | | | 150 | ns |

# PROGRAMMING INFORMATION (Continued)



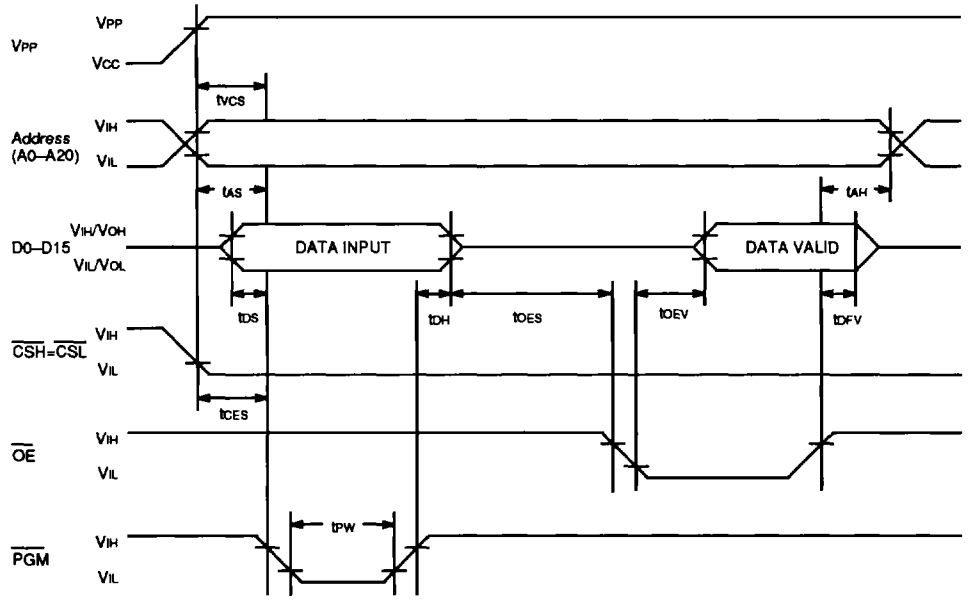

1

# PROGRAMMING INFORMATION (Continued)



# PROGRAMMING INFORMATION (Continued)

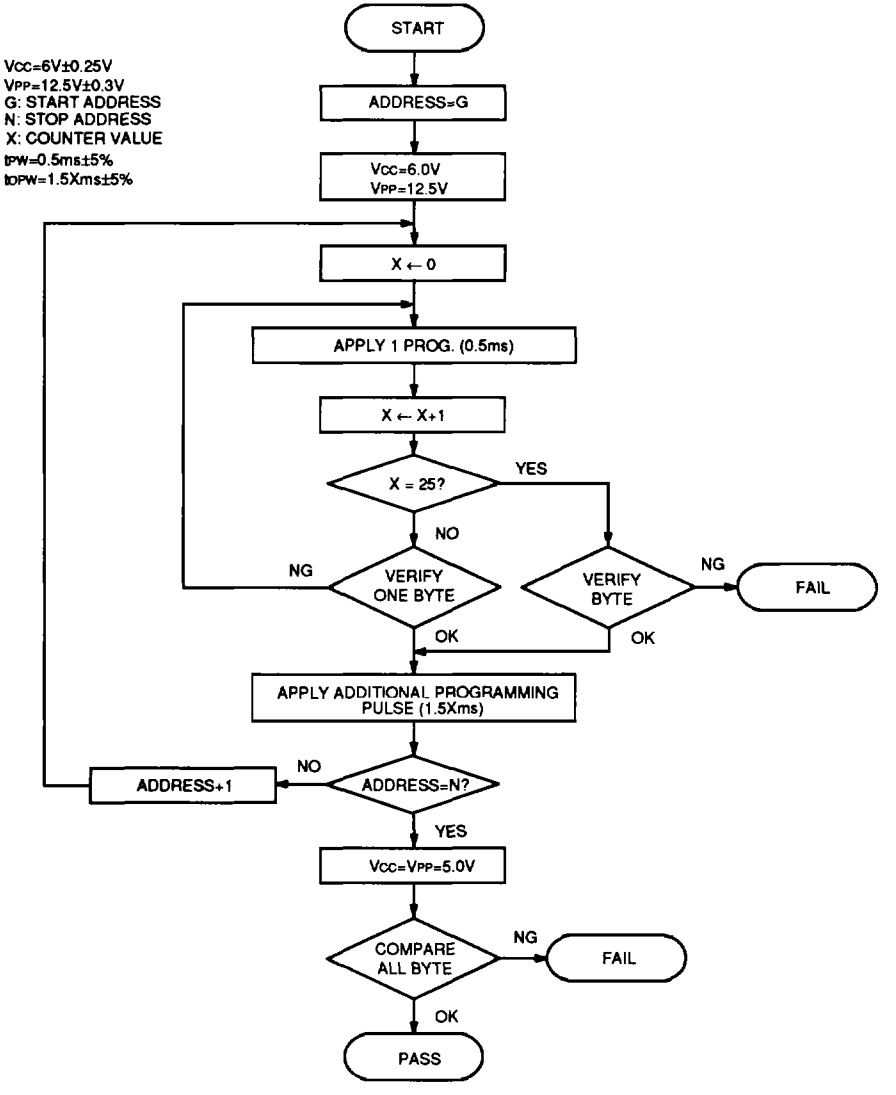
PROGRAMMING CYCLE 3: $\overline{CSL}$ = $\overline{CSH}$: x 16–bit Bus Organization




1

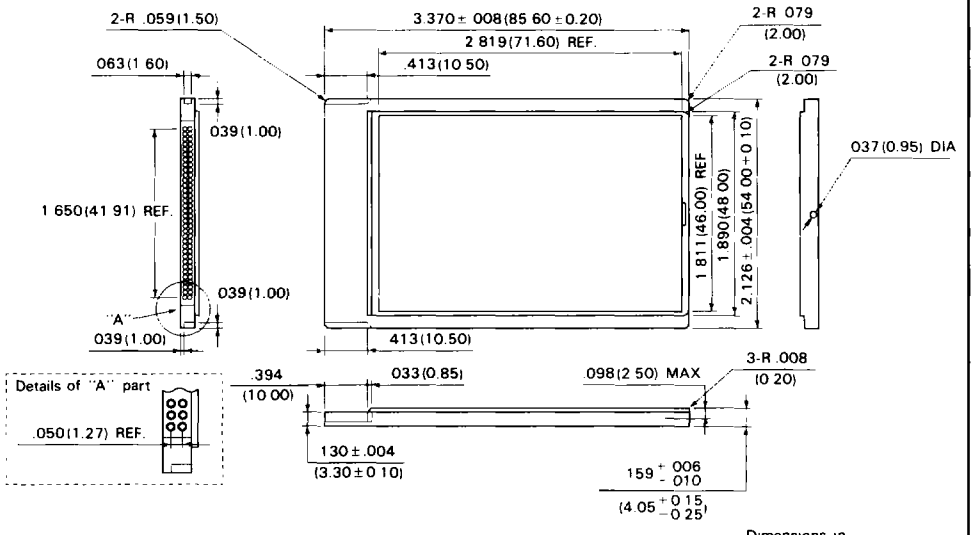
# PROGRAMMING INFORMATION (Continued)

PROGRAMMING FLOWCHART



# PACKAGE DIMENSIONS

**68-PIN MEMORY CARD**
**(CASE No.: CRD-68P-M03)**






Dimensions in
inches (millimeters)

1