OKI Semiconductor

MSM514280/SL

262,144-Word × 18-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM514280/SL is a new generation Dynamic RAM organized as 262,144-word × 18-bit configuration.
The technology used to fabricate the MSM514280/SL is OKI's CMOS silicon gate process technology.
The device operates at a single 5V power supply. Its I/O pins are TTL compatible.

FEATURES

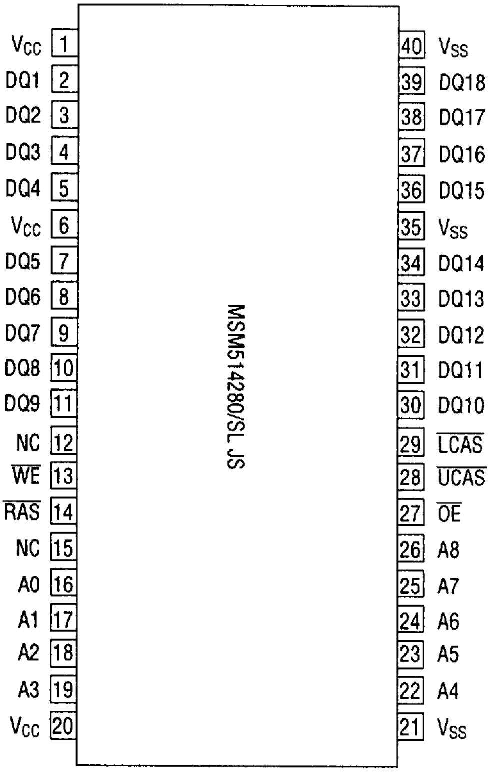
- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 262,144-word × 18-bit organization
- Single 5V power supply, ±10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate
- Refresh: 512 cycles/8ms, 512 cycles/128ms (SL version)
- Fast page mode, read modify write capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh, $\overline{\text{RAS}}$ only refresh capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh capability (SL version)
- Package :

40-Pin 400mil	Plastic SOJ	(SOJ40-P-400)
40-Pin 475mil	Plastic ZIP	(ZIP40-P-475)

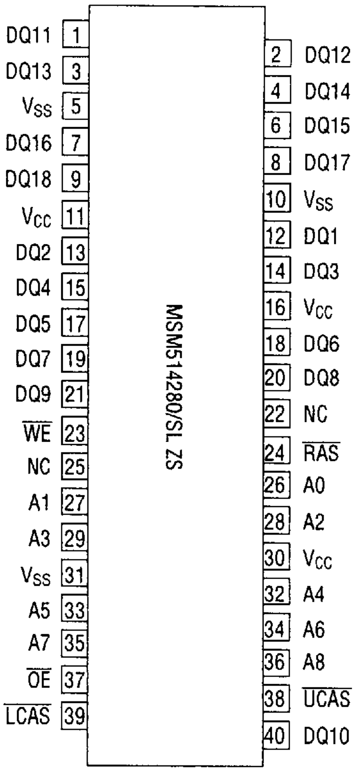
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM514280/SL-70	70ns	35ns	20ns	20ns	130ns	935mW	5.5mW/ 1.1mW(SL version)
MSM514280/SL-80	80ns	40ns	20ns	20ns	150ns	825mW	
MSM514280/SL-10	100ns	50ns	25ns	25ns	180ns	715mW	

PIN CONFIGURATION (TOP VIEW)



40-PIN SOJ

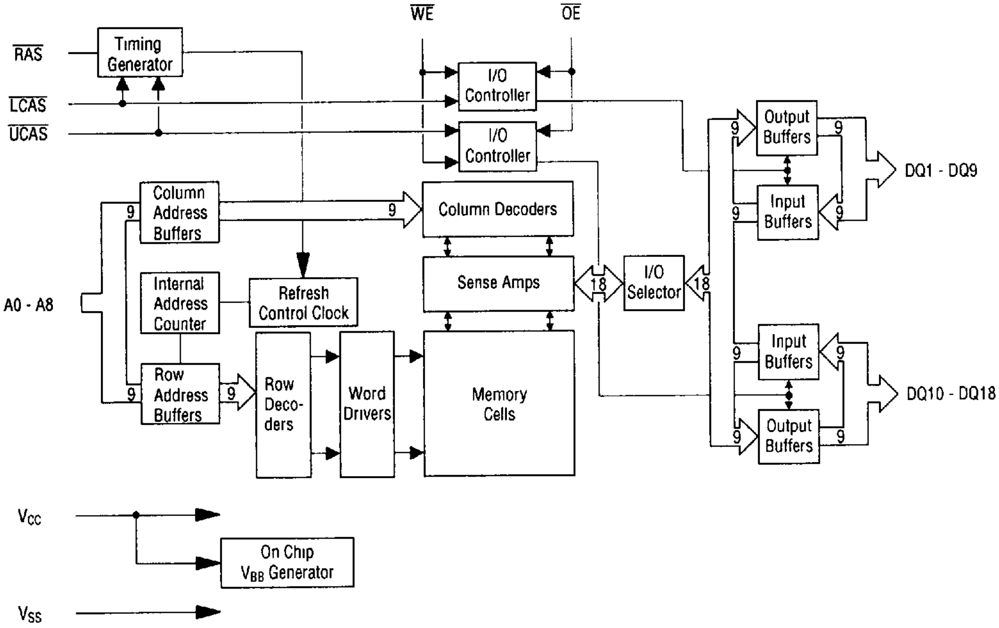


40-PIN ZIP

Pin Name	Function
A0 - A8	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{LCAS}}$	Lower Byte Column Address Strobe
$\overline{\text{UCAS}}$	Upper Byte Column Address Strobe
DQ1 - DQ18	Data - Input / Data - Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
V_{CC}	Power Supply (5V)
V_{SS}	Ground (0V)
NC	No Connection

Note: Same power supply voltage must be provided to every V_{CC} pin, and same GND voltage level must be provided to every V_{SS} pin.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL TABLE

Input Pin					DQ Pin		Functional Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ1 - DQ9	DQ10 - DQ18	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	H	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	–1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	–1.0	—	0.8	V

Capacitance

(V_{CC} = 5V ± 10%, Ta = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A8)	C_{IN1}	—	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ18)	$C_{I/O}$	—	10	pF

DC Characteristics

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MSM514280/SL-70		MSM514280/SL-80		MSM514280/SL-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = −5.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V ≤ V_I ≤ 6.5V; All other pins not under test = 0V	−10	10	−10	10	−10	10	µA	
Output Leakage Current	I_{LO}	DQi Disable 0V ≤ V_O ≤ 5.5V	−10	10	−10	10	−10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min.	—	170	—	150	—	130	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	2	—	2	—	2	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V	—	1	—	1	—	1		
			—	200	—	200	—	200	µA	1, 5
Average Power Supply Current ($\overline{RAS}$ Only Refresh)	I_{CC3}	$\overline{RAS}$ = cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min.	—	170	—	150	—	130	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = Enable	—	5	—	5	—	5	mA	1
Average power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ = cycling $\overline{CAS}$ before $\overline{RAS}$	—	170	—	150	—	130	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL} $\overline{CAS}$ cycling t_{PC} = Min.	—	140	—	130	—	120	mA	1, 3
Average Power Supply Current (Battery Backup)	I_{CC10}	t_{RC} = 125µs $\overline{CAS}$ before $\overline{RAS}$ t_{RAS} ≤ 1µs	—	300	—	300	—	300	µA	1, 2, 4, 5
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Self-refresh)	I_{CCS}	$\overline{RAS}$ ≤ 0.2V $\overline{CAS}$ ≤ 0.2V	—	200	—	200	—	200	µA	1, 5

Notes:
1. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V, −1.0V ≤ V_{IL} ≤ 0.2V.
5. SL version.

AC Characteristics (1/2)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM 514280/SL-70		MSM 514280/SL-80		MSM 514280/SL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or write Cycle Time	t_{RC}	130	—	150	—	180	—	ns	
Read Modify Write Cycle Time	t_{RMW}	180	—	200	—	240	—	ns	
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	60	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRMW}	95	—	100	—	120	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	4, 5
Access Time from Column Address	t_{AA}	—	35	—	40	—	50	ns	4, 6
Access Time from $\overline{OE}$	t_{OEA}	—	20	—	20	—	25	ns	4
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	40	—	45	—	55	ns	4, 12
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	ns	
Output Buffer Turn-off Delay Time	t_{OFF}	0	15	0	15	0	20	ns	7
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	15	0	15	0	20	ns	7
Transition Time	t_T	3	50	3	50	3	50	ns	
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	
Refresh Period (SL version)	t_{REF}	—	128	—	128	—	128	ms	15
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	t_{ROH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Precharge time (Fast Page Mode)	t_{CP}	10	—	10	—	10	—	ns	14
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	12
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	25	75	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	20	50	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	11
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	11
Column Address Hold Time from $\overline{RAS}$	t_{AR}	55	—	60	—	75	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	50	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	11
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	8, 11
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	8

AC Characteristics (2/2)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM 514280/SL-70		MSM 514280/SL-80		MSM 514280/SL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	9, 11
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	11
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t_{WCR}	55	—	60	—	75	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t_{OEH}	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	13
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	20	—	20	—	25	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	10, 11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	ns	10, 11
Data-in Hold Time from $\overline{\text{RAS}}$	t_{DHR}	55	—	60	—	75	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t_{OED}	15	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{CWD}	45	—	45	—	55	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t_{AWD}	60	—	65	—	80	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{RWD}	95	—	105	—	130	—	ns	9
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t_{RPC}	10	—	10	—	10	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$)	t_{CSR}	10	—	10	—	10	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$)	t_{CHR}	15	—	15	—	20	—	ns	12
$\overline{\text{CAS}}$ Precharge Time (Refresh Counter Test)	t_{CPT}	40	—	40	—	50	—	ns	14
$\overline{\text{CAS}}$ Precharge Time	t_{CPN}	10	—	10	—	10	—	ns	14
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self-refresh)	t_{RASS}	100	—	100	—	100	—	µs	15
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self-refresh)	t_{RPS}	130	—	150	—	180	—	ns	15
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self-refresh)	t_{CHS}	–50	—	–60	—	–70	—	ns	15

Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles (Example: $\overline{\text{RAS}}$ only refresh) before proper device operation is achieved.

2. The AC characteristics assume $t_T = 5\text{ns}$.

3. V_{IH}(Min.) and V_{IL}(Max.) are reference levels of input signals for timing measurement. Transition times(t_T) are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2 TLL loads and 100pF.

5. Operation within the t_{RCD}(Max.) limit insures that t_{RAC}(Max.) can be met. t_{RCD}(Max.) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD}(Max.) limit, then access time is controlled exclusively by t_{CAC}.

6. Operation within the t_{RAD}(Max.) limit insures that t_{RAC}(Max.) can be met. t_{RAD}(Max.) is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD}(Max.) limit, then access time is controlled exclusively by t_{AA}.

7. t_{OFF}(Max.) and t_{OEZ}(Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8. Either t_{RRH} and t_{RCH} must be satisfied for a read cycle.

9. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$(Min.), the cycle as an early write cycle and data out will remain open circuit (high impedance) throughout the entire cycle: if $t_{CWD} \geq t_{CWD}$(Min.), $t_{RWD} \geq t_{RWD}$(Min.) and $t_{AWD} \geq t_{AWD}$(Min.), the cycle is read modify write cycle and data out will contain data read from the selected cell: if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

10. These parameters are referenced to $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a $\overline{\text{OE}}$ control write cycle or a read modify write cycle.

11. t_{ASC}, t_{CAH}, t_{RCS}, t_{RCH}, t_{WCS}, t_{DS}, t_{DH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.

12. t_{CRP}, t_{CHR} and t_{CPA} are determined by the later rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.

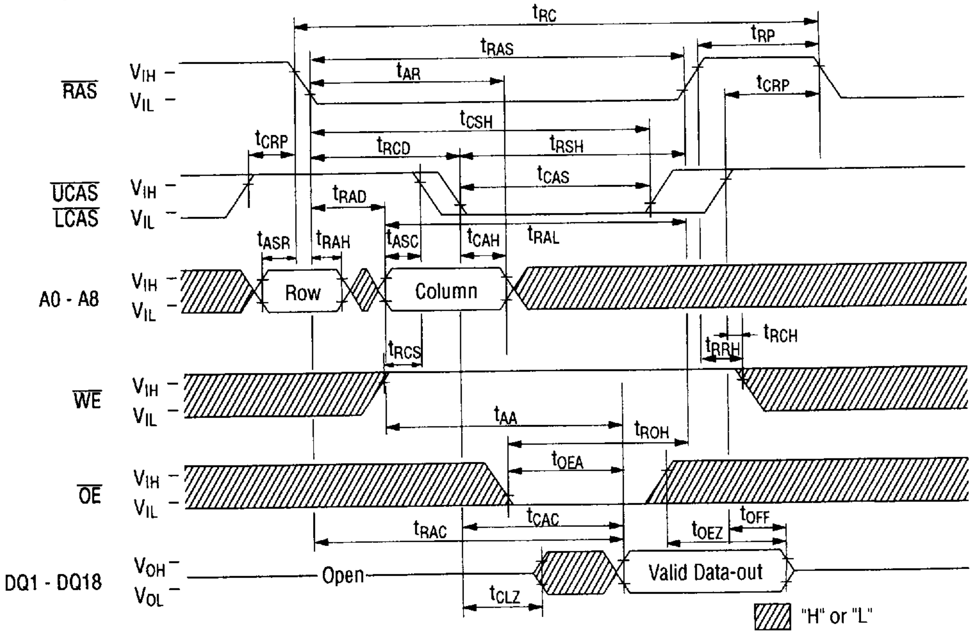
13. t_{CWL} should be satisfied by both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.

14. t_{CPN}, t_{CP} and t_{CPT} are determined by the time that both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are high.

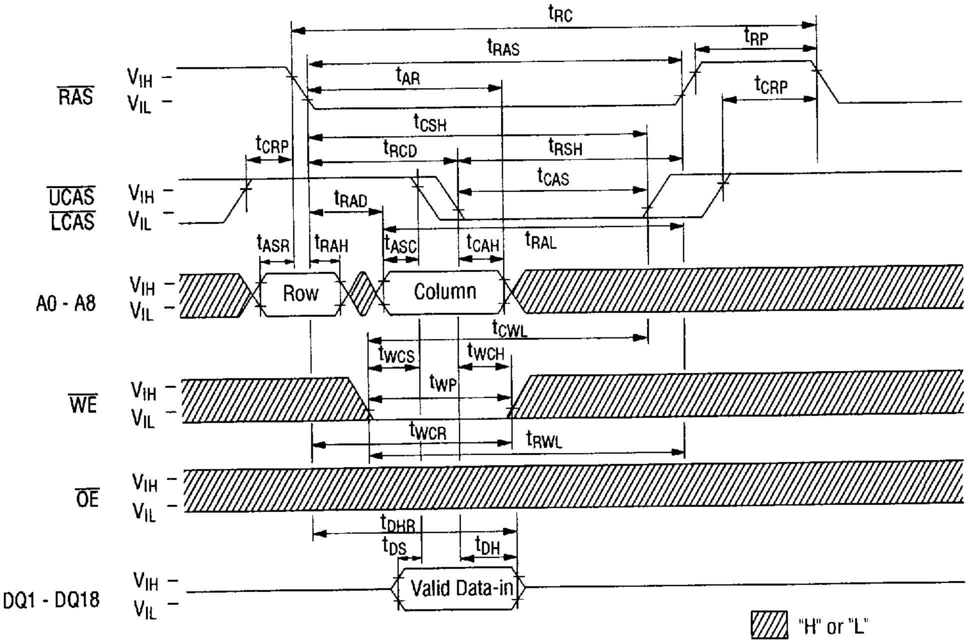
15. SL version.

TIMING WAVEFORM

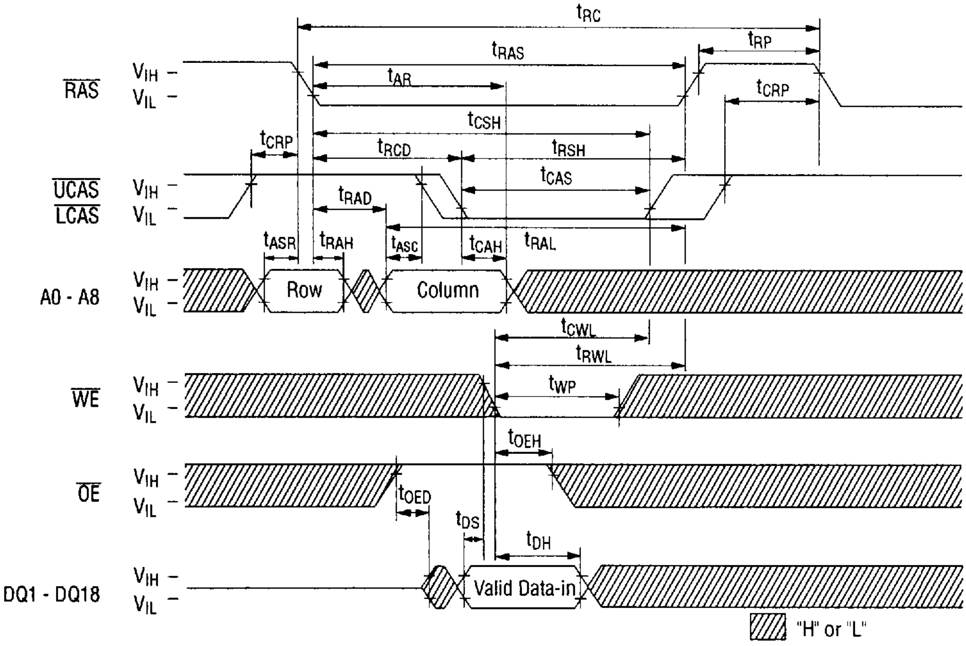
Read Cycle



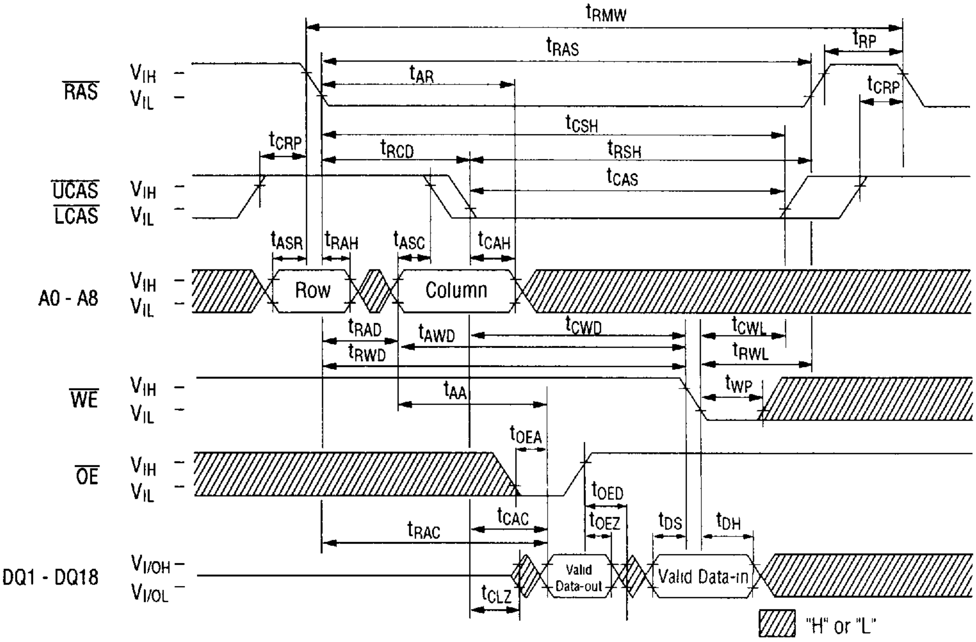
Write Cycle (Early Write)



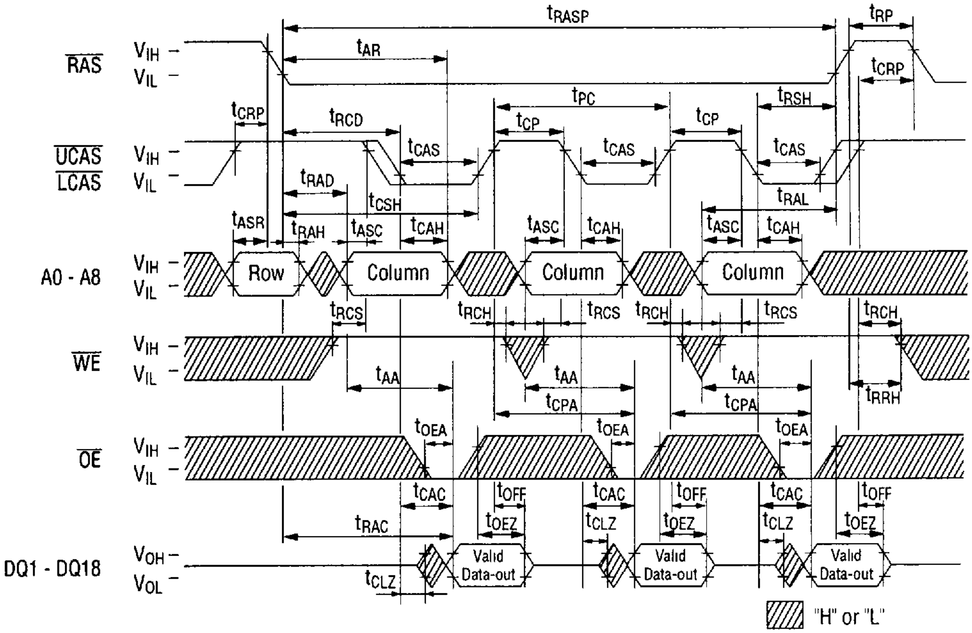
Write Cycle (OE Control Write)



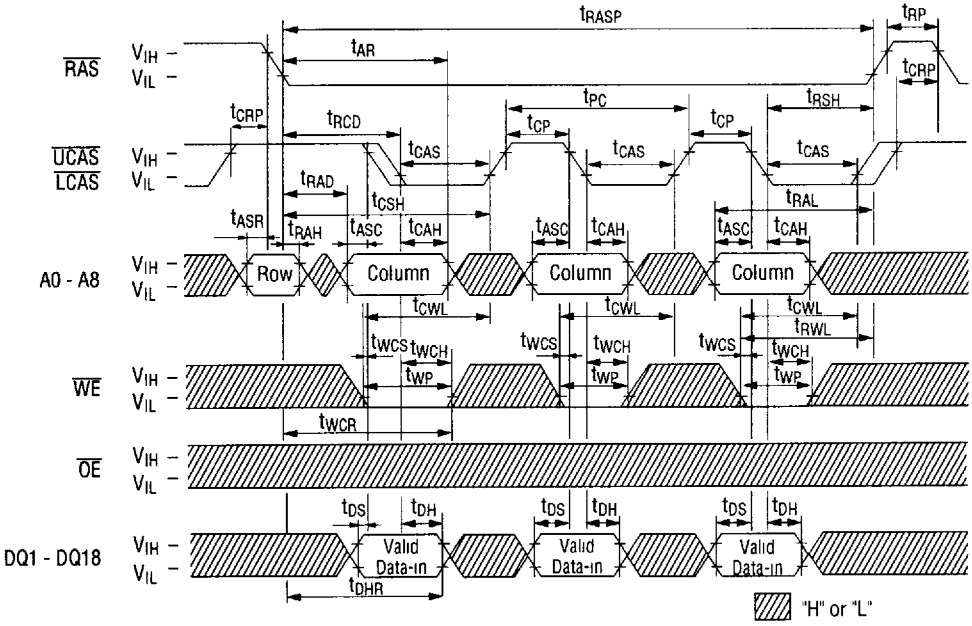
Read Modify Write Cycle



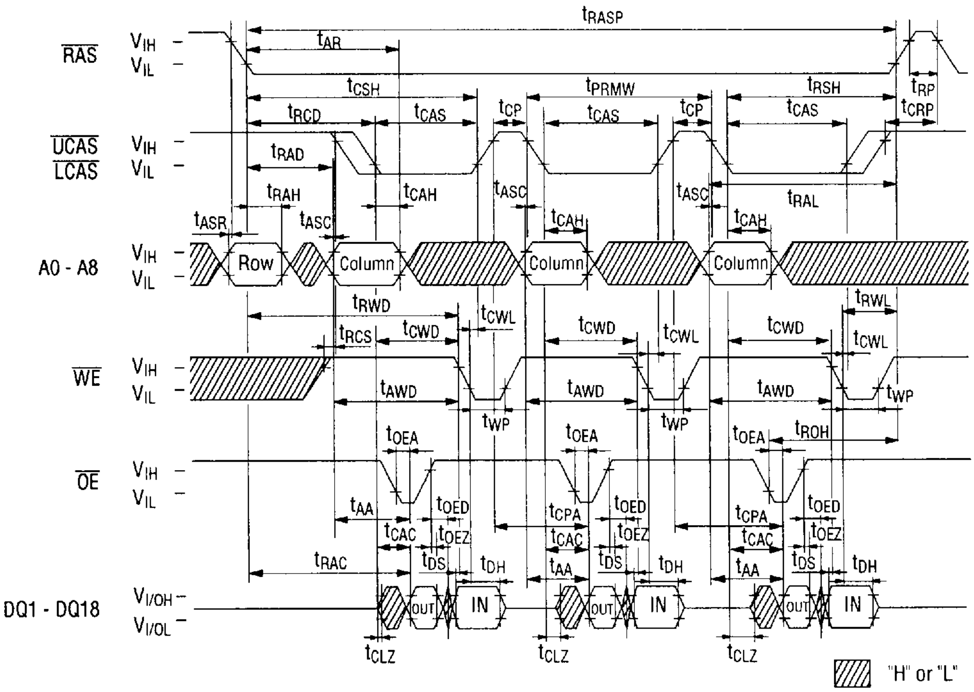
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)

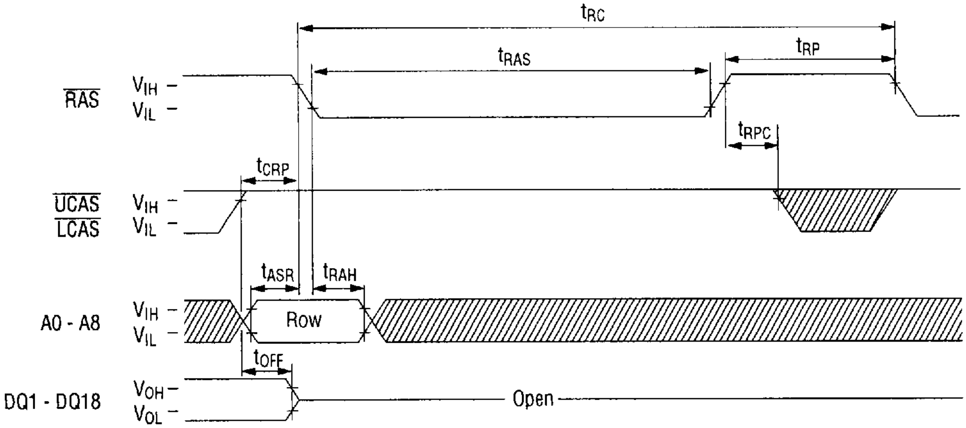


Fast Page Mode Read Modify Write Cycle



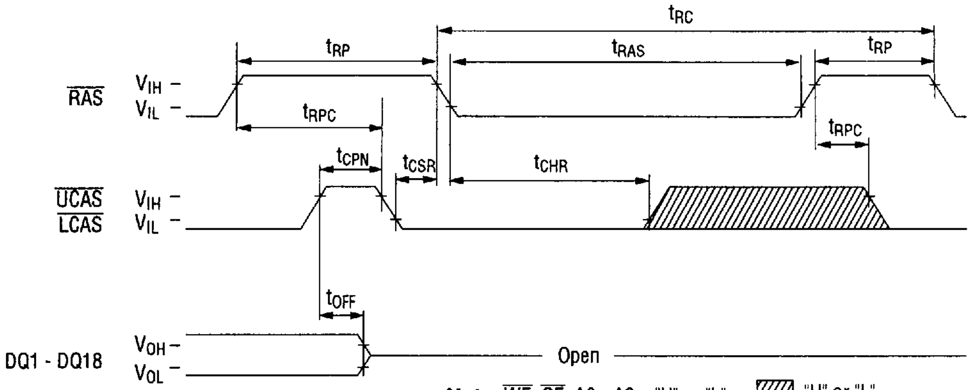
▨ "H" or "L"

RAS-only Refresh Cycle



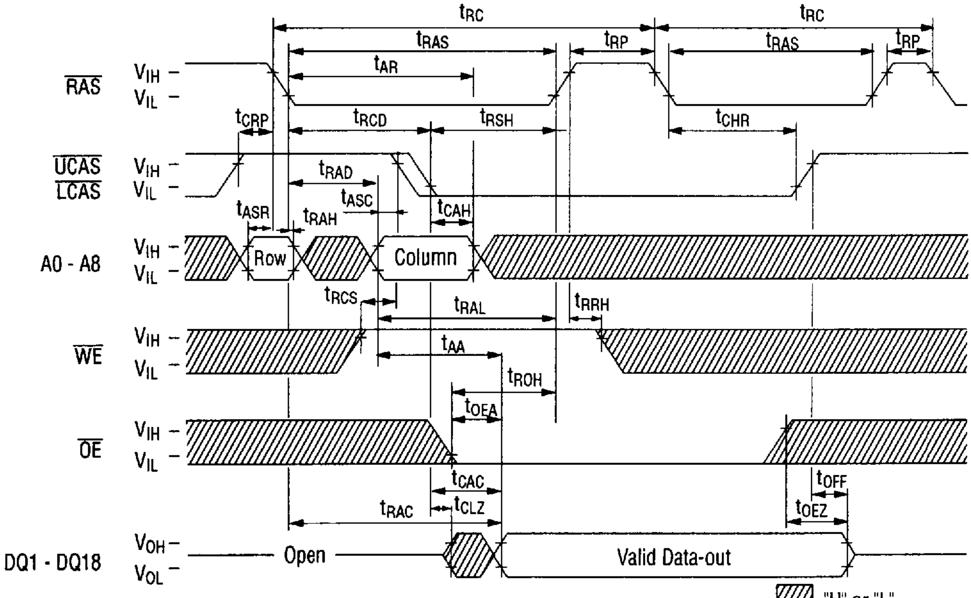
Note: WE, OE = "H" or "L" ▨ "H" or "L"

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Auto Refresh Cycle



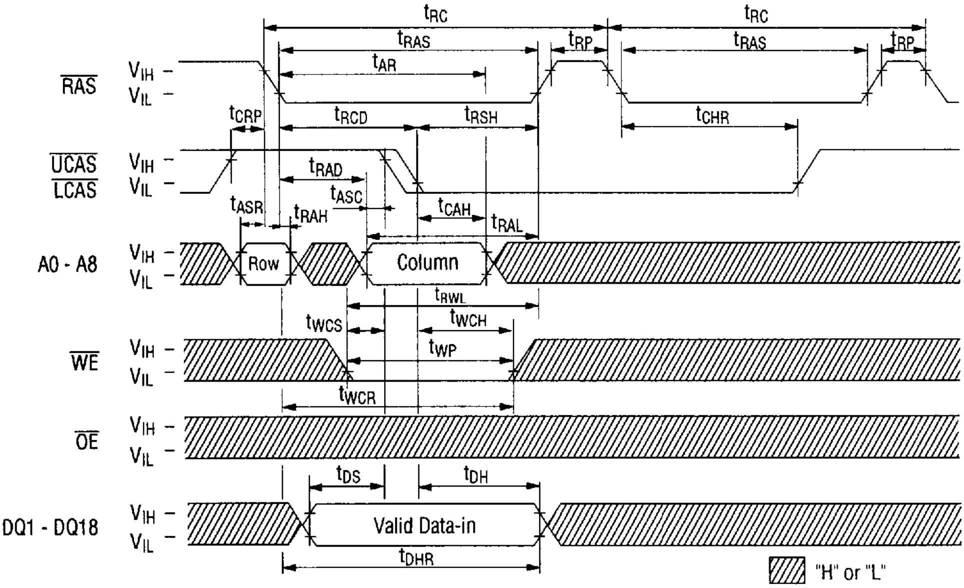
Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 - A8 = "H" or "L" ▨ "H" or "L"

Hidden Refresh Read Cycle

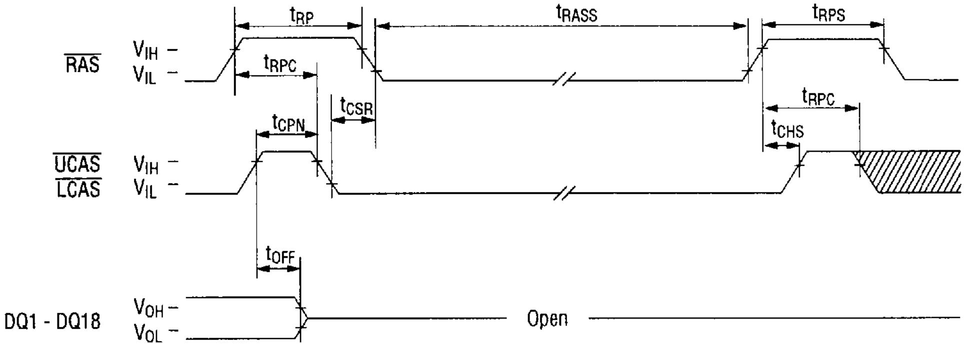


▨ "H" or "L"

Hidden Refresh Write Cycle



$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self-refresh Cycle



Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 - A8 = "H" or "L"
SL version

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test Cycle