GEC PLESSEY

SEMICONDUCTORS

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MA28137

Radiation Hard Programmable DMA Controller

Features

- Radiation hard to 1 MRad (Si)
- High SEU immunity, latch-up free
- CMOS Silicon-on-Sapphire Technology
- MAS281 MIL-STD-1750A compatible
- Four independent DMA channels
- Independent autoinitialisation of all channels
- Enable/Disable control of individual DMA requests
- Memory-to-memory, I/0-to-memory and memory-to-I/0
- Memory block initialisation

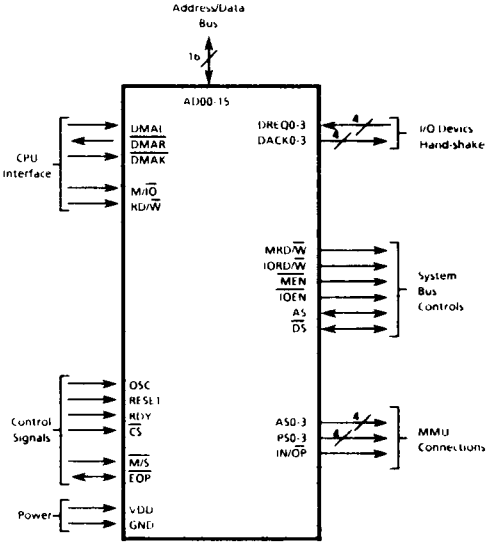


Figure 1: DMA Controller Connections

1 General Description

The MA28137 Direct Memory Access (DMA) controller is a peripheral interface circuit designed for MAS281 based microprocessor systems. It enhances system performance by allowing two way data transfer between external devices and the system memory, and between two memories. The MA28137 offers a wide variety of programmable control features to enhance system optimisation and to allow dynamic reconfiguration under program control.

The four independent channels may be expanded by cascading additional controller chips. Each channel can be individually programmed to autoinitialise to its original condition following an End of Process (EOP).

Three basic transfer modes are offered; read, write and verify.

A Memory Management Unit (MMU) can be used in conjunction with the MA28137 to extend addressing capability to 1M word.

2 Block Diagram

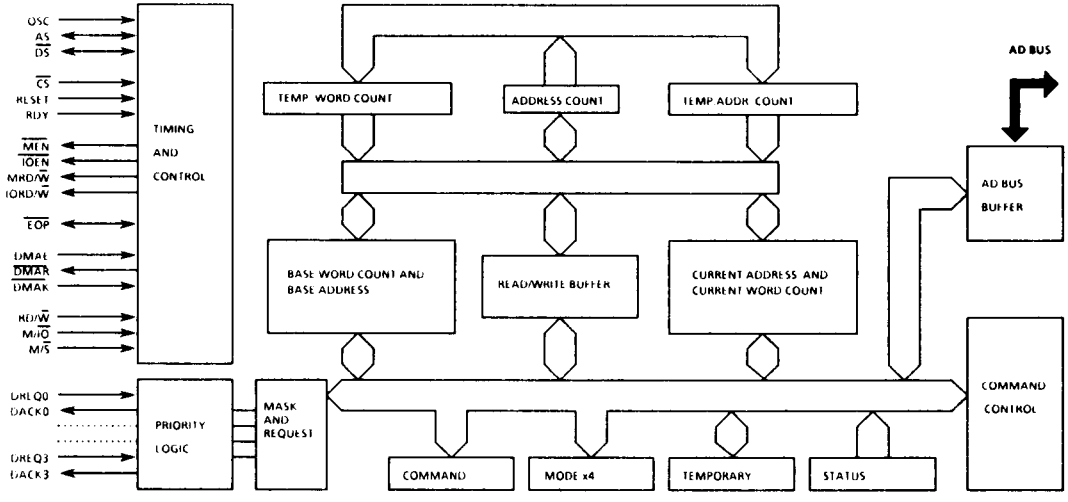


Figure 2: DMA Controller Principal Functional Blocks

3 Functional Description

The MA28137 provides four independent DMA channels, configurable under software control. Further DMA channels can be added by cascading two or more DMA controllers (see 4.2.4). Separate memory and I/O control signals are provided to allow direct I/O to memory and memory to I/O transfers. For memory to memory transfers, data passes through a 16-bit temporary register. Each channel has an associated MMU status register. Data held in these registers is output during DMA transfers to provide address status, instruction or operand status, and process status information to the memory management unit.

The major functional blocks and the principlal data paths of the DMA controller are shown in figure 2. The device contains three important blocks of control logic; the timing control block which generates internal timing and external control signals, the priority encoder block which resolves priority contention between DMA channels requesting service simultaneously, and the program command control block which decodes commands given to the MA28137 by the microprocessor and, while servicing a DMA request, decodes mode control words . The function and CPU access to each register in the set, is detailed in section 5.

4 DMA Operation

The MA28137 has two cycles of operation called the idle and active cycles. Each cycle comprises a number of states, each of which is one full OSC/2 internal clock period in length. For more detail see section 7.

When there is no DMA request pending the MA28137 enters the idle cycle. Although in the idle cycle, and thus inactive, the DMA controller may still be programmed by the processor. The control signals MENN, IOENN, MRD/WN and IORD/WN are generated by decoding the signals M/ION and RD/WN received from the MAS281. Whilst in the idle cycle the DMA controller repeats Si states until it enters the active cycle and the S0 state.

The MA28137 issues a DMA request to the processor and waits for a DMA acknowledge to be returned. When the acknowledge is received, the DMA transfer begins, however, until the acknowledge is received, the MA28137 remains programmable, and the M/ION and RD/WN signals continue to be decoded.

States S1, S2, S3 and S4 are the normal working states of a DMA transfer. If more time is needed to complete a transfer, wait states can be inserted by the MA28137 ready signal, between states S3 and S4.

During movements of data from memory to memory, each transfer word is temporarily stored in the DMA controller's temporary register. States S1, S2, S3 and S4 read the data word into the temporary register and and then transfer it from the temporary register to its new location. During the transfer all necessary bus control signals are driven by the DMA controller. For more detail see section 5.

When transferring data between memory and I/O, the temporary register is not used and data is passed directly from the source to the destination. The DMA controller passes through states S1, S2, S3 and S4 to complete a transfer (see figure 5).

4.1 Idle Cycle

When none of the channels are requesting service, the MA28137 will enter the idle cycle and perform Si states. In this cycle the MA28137 will sample the DREQ lines every clock cycle, to determine if any of the channels are requesting a DMA service. The device will also sample CSN, looking for an attempt by the microprocessor to write or read the MA28137's internal registers. When CSN is low and DMAK is high, the MA28137 enters the program condition and the CPU can establish, change, or inspect the internal definition of the device by reading from, or writing to, the internal registers. The four low-order address/data lines AD15-AD12, select which register is to be accessed. The RD/WN and DSN lines are used to select and time reads or writes.

There are two special software commands which can be executed by the MA28137 when in the program condition. These commands are decoded as sets of address with CSN and RD/WN. The commands Master Clear and Clear Mask do not make use of the data bus.

4.2 Active Cycle

When the MA28137 is in the idle cycle and a non-masked channel requests a DMA service, the device will output a DMAR to the microprocessor and enter the active cycle. In this cycle a DMA service will take place, in one of the four modes below.

4.2.1 Single Transfer Mode

In single transfer mode the device is programmed to make one transfer only. The word count will be decremented, and the address decremented or incremented following each transfer. The channel can be programmed to enable a Terminal Count (TC) to cause an autoinitialise when the word count 'rolls over' from zero to $FFFF_H$.

DREQ will not be recognised if it is allowed to go inactive before DACK becomes active. If DREQ is held active throughout the single transfer, DMARN will go inactive and release the bus to the system. Upon receipt of a new DMAK after the single tarnsfer, DMARN will once again go active, allowing another transfer to take place.

4.2.2 Block Transfer Mode

In block transfer mode the device is instructed by DREQ to continue making transfers during the service until a terminal count, caused by the word count going to $FFFF_H$, or an external end of process is encountered. DREQ need only be held active until DACK becomes active. Again, if the channel has been programmed, an autoinitialisation will occur at the end of the service.

4.2.3 Demand Transfer Mode

In demand transfer mode the device is programmed to continue making transfers until a terminal count or external EOP is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity.

After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the MA28137 current address and current word count registers. Only an EOP can cause an autoinitialise at the end of the service: EOP is generated either by TC or by an external signal.

4.2.4 Cascade Mode

This mode is used to cascade more than one MA28137 together for simple system expansion. The DMAR and DMAK signals from the additional controller are connected to the DREQ and DACK signals of a channel on the initial MA28137. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the processing device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests.

In a system with only one DMA controller, the controller generates the system control signals MENN, IOENN, MRD/WN and IORD/WN from the incoming signals M/ION and RD/WN during periods when DMAKN is high (i.e. no transfers occurring). This allows the same control signals to be used during both DMA and non-DMA modes.

In a multi-level DMA system during non-DMA periods only one controller must generate the four system control lines, to prevent contention. The master/slave (M/SN) pin enables (master) or disables (slave). The generation of these control lines during non-DMA mode and allows one level 1 controller to be designated a master (with all other controllers as slaves).

The cascade channel of the master MA28137 is used only to prioritise the slave device, it does not produce any address or control signals of its own. These could conflict with the address and control signals of the slave device. The master MA28137 will respond to DREQ and DACK but all other outputs except DMARN will be disabled.

Figure 3 shows two slave devices cascaded into the master device using two of its channels. This forms a two level DMA system. More MA28137s could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

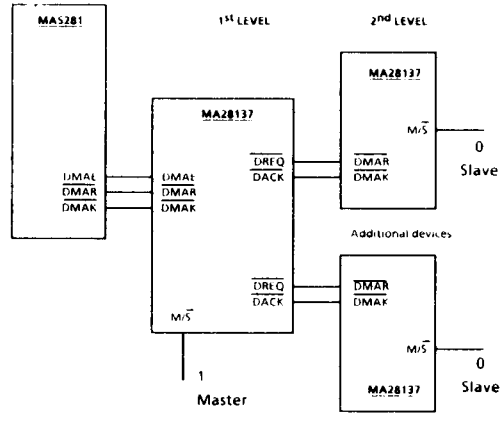


Figure 3: Connections of Cascaded DMA Controllers

4.3 Transfer Types

Each of the active transfer modes can perform three different types of transfer. These are read, write and verify.

Write transfers move data from an I/O device to memory by making MRD/WN low, IORD/WN high and toggling DSN. Similarly read transfers move data from memory to an I/O device by making MRD/WN high, IORD/WN low and toggling DSN.

Verify transfers are pseudo transfers. The MA28137 operates as in read or write transfers generating addresses and responding to EOPN, etc. However, the memory and I/O control lines all remain inactive. Verify mode is not permitted during memory to memory operation.

4.4 Memory-to-Memory

To perform block moves of data from one area of memory to another, with a minimum of program effort and time, the MA28137 includes a memory-to-memory transfer feature. Programming bit 15 in the command register selects channels 0 and 1 to operate as memory-to-memory transfer channels.

The transfer is initiated by setting the software DREQ for channel 0. The MA28137 requests a DMA service in the normal manner. After DMAKN is true, the device using eight-state transfers in block transfer mode, reads data from the memory. The channel 0 current address register is the source for the address used and is decremented or incremented in the normal manner. The data word read from the memory is stored in the MA28137 internal temporary register.

Channel 1 then writes the data from the temporary register to memory using the address in its current address register and incrementing or decrementing it in the normal manner. The channel 1 current word count is decremented. When the word count of channel 1 becomes equal to $FFFF_H$, a terminal count is generated causing an EOP output terminating the service.

Channel 0 may be programmed to retain the same address for all transfers allowing a single word to be written to a block of memory.The MA28137 will respond to external EOP signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. DMAKN signals are not active during memory to memory transfers.

4.5 Auto-initialisation

By programming bit 11 in the mode register a channel may be set up as an auto-initialise channel. During auto-initialise, the original values of the current address and current word count registers are automatically restored from the base address and base word count registers of that channel following EOP. The base registers are loaded when the current registers are loaded by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in auto-initialise. Following auto-initialise the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected.

4.6 Priority

The MA28137 has two types of priority encoding available as software selectable options. The first is fixed priority, which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3, followed by 2, 1 and 0. After the recognition of any one channel for service, the other channels are prevented from interfering with that service until it is completed.

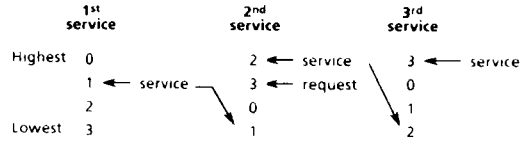


Figure 4: DMA Servicing Sequence with Rotating Priority

The second scheme is rotating priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. With rotating priority in a single chip DMA system any device requesting service is guaranteed to be recognised after no more than three higher priority services have occurred. This prevents any one channel from monopolising the system.

5 Register Descriptions

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current address registers	16 bits	4
Current word count registers	16 bits	4
Temporary address register	16 bits	1
Temporary word count register	16 bits	1
MMU status register	11 bits	4
Status register	8 bits	1
Temporary register	16 bits	1
Mode registers	8 bits	4
Command register	6 bits	1
Mask register	4 bits	1
Request register	3 bits	1

Table 1: Register Summary

5.1 Base Address and Base Word Count Registers

Each channel has a pair of base address and base word count registers. These 16-bit registers store the original value of their associated current registers, and are used to restore the original values to the current register after an autoinitialisation. The base registers are written simultaneously with their corresponding current register. These registers cannot be read by the microprocessor.

5.2 Current Address Register

Each channel has a 16-bit current address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the current address register during the transfer. This register is restored to its original value by an autoinitialise. Autoinitialise takes place only after an EOP.

5.3 Current Word Count Register

Each channel has a 16-bit current word count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the current word count register (i.e. programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes from zero to $FFFF_H$, a terminal count will be generated. Following the end of a DMA service it may also be reinitialised to its original value by an autoinitialisation, however, this may only occur when an EOP occurs. If it is not autoinitialised this register will hold a count of $FFFF_H$ after TC.

5.4 MMU Status Register

Each channel has an 11-bit register associated with it which holds process and address status information for use by an MMU. During DMA transfer, the contents of this register are placed on lines AS0-3 and PS0-3 to allow the correct memory page to be selected and accessed. In addition, the signal IN/OPN is produced to select the instruction or operand page register set. The entire register is cleared by a reset.

During memory to I/O, or I/O to memory transfers, the AS and PS fields associated with the selected channel are placed on the appropriate output lines. During memory-to-memory transfer the AS and PS fields alternate between those programmed into channels 0 and 1 to allow transfers between different address states.

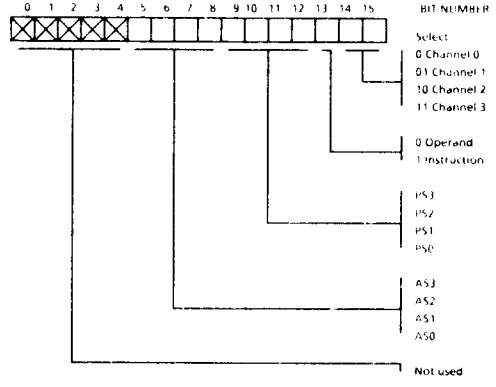


Figure 5: MMU Status Register

5.5 Status Register

The MA28137 contains a status register which can be read by the microprocessor. It contains information about the status of the device indicating which channels have reached a terminal count and which channels have pending DMA requests. Bits 15-12 are set every time a terminal count is reached by the corresponding channel or an external EOP is applied. These bits are cleared upon reset and on each status read. Bits 11-8 are set whenever their corresponding channel is requesting service.

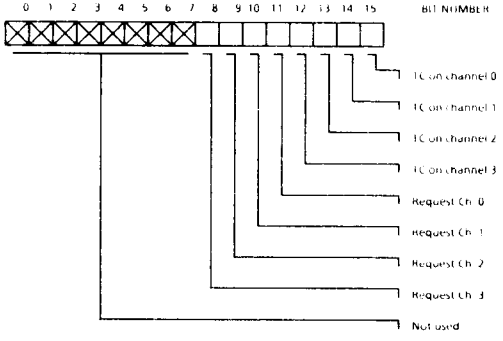


Figure 6: Status register

5.6 Temporary Register

The temporary register is used to hold data during memory-to-memory transfers. When in the program condition following the completion of a transfer, the last word transferred can be read by the microprocessor. The temporary register always contains the last word transferred in the previous memory-to-memory operation, unless cleared by a reset.

5.7 Mode Register

Each channel has an associated 8-bit mode register. When the register is being written to by the microprocessor in the program condition, bits 14 and 15, determine which channel is being addressed.

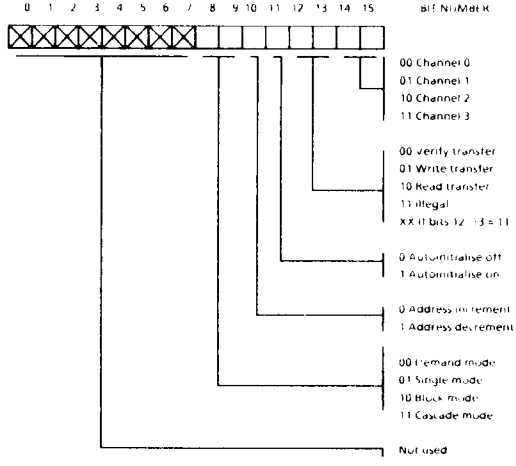


Figure 7: Mode Register

5.8 Command Register

This 6-bit register controls the operation of the MA28137. It is programmed by the microprocessor in the program condition and is cleared by Preset or a Master Clear instruction. Table 2 lists the function of the command bits (see section 6).

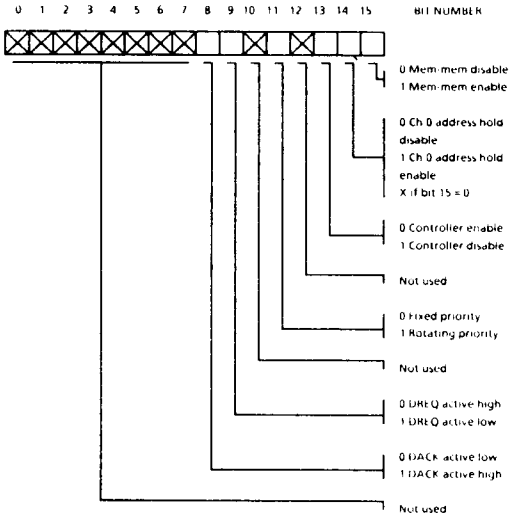


Figure 8: Command Register

5.9 Mask Register

Each channel has a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP unless the channel has been programmed for autoinitialise. Each bit of the 4-bit mask register may also be set or cleared separately under software control. The entire register is also set by a Preset. Reset also disables all DMA requests until a clear mask register instruction. The instruction to separately set or clear the mask bits is similar in form to that used with the request register. All four bits of the mask register may also be written to with a single command.

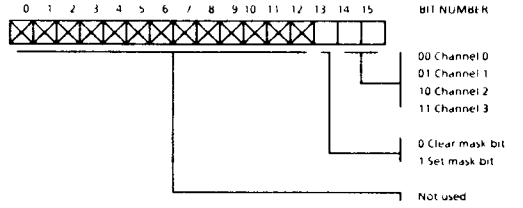


Figure 9: Mask register

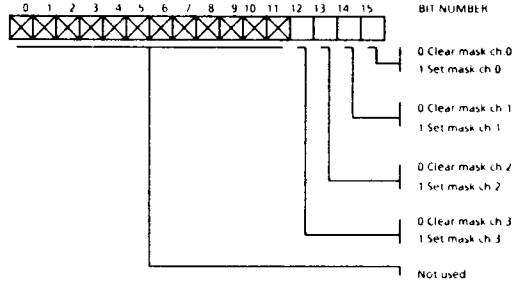


Figure 10: Mask register 4-bit write

5.10 Request Register

The MA28137 can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the request register. These are non-maskable and subject to prioritisation by the priority encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a reset. To set or reset a bit, the software loads the proper form of the data word. In order to make a software request, the channel must be in block mode.

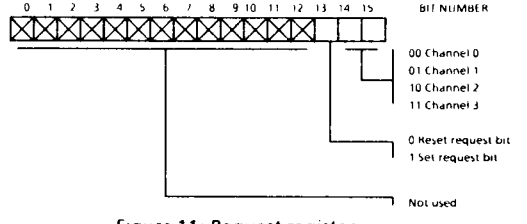


Figure 11: Request register

6 Programming

The MA28137 will accept programming from the host processor when DMAKN is inactive; this is true even if DMAR is active. The responsibility of the host is to assure that programming and DMAKN are mutually exclusive. Note that a problem can occur if a DMA request occurs on an unmasked channel while the MA28137 is being programmed. For instance, the CPU may be starting to reprogam the address register and word count of channel 1 when channel 1 receives a DMA request. If the MA28137 is enabled ie bit 13 in the command register is 0, and channel 1 is unmasked, a DMA service can occur when the address register only, has been reprogrammed. This can be avoided by disabling the controller by setting bit 13 in the command register, or masking the channel before programming any other registers. Once this is complete, the controller can be enabled or un-masked.

After power-up it is suggested that all internal locations, especially the mode registers, be loaded with some valid value. This should be done even if some channels are unused.

6.1 Software Commands

Master Clear and Clear Mash are two special software commands which can be executed in the program condition. They do not depend on any specific data bus bit pattern.

Master Clear: Has the same effect as the hardware reset. The command status, request and temporary registers are cleared and the mask register is set. The MA28137 will enter the idle cycle.

Clear Mask: Clears the mask bits of all four channels, enabling them to accept DMA requests.

Signals					Operation
A12	A13	A14	A15	RD/W	
0	0	0	0	1	Read current address register chan 0
0	0	0	0	0	Write current address register chan 0
0	0	0	1	1	Read current word count register chan 0
0	0	0	1	0	Write current word count register chan 0
0	0	1	0	1	Read current address register chan 1
0	0	1	0	0	Write current address register chan 1
0	0	1	1	1	Read current word count register chan 1
0	0	1	1	0	Write current word count register chan 1
0	1	0	0	1	Read current address register chan 2
0	1	0	0	0	Write current address register chan 2
0	1	0	1	1	Read current word count register chan 2
0	1	0	1	0	Write current word count register chan 2
0	1	1	0	1	Read current address register chan 3
0	1	1	0	0	Write current address register chan 3
0	1	1	1	1	Read current word count register chan 3
0	1	1	1	0	Write current word count register chan 3
1	0	0	0	1	Read status register
1	0	0	0	0	Write command register
1	0	0	1	1	Illegal
1	0	0	1	0	Write request register
1	0	1	0	1	Illegal
1	0	1	0	0	Write single mask register bit
1	0	1	1	1	Illegal
1	0	1	1	0	Write mode register
1	1	0	0	1	Illegal
1	1	0	0	0	Write MMU status
1	1	0	1	1	Read temporary register
1	1	0	1	0	Master Clear
1	1	1	0	1	Illegal
1	1	1	0	0	Clear mask register
1	1	1	1	1	Illegal
1	1	1	1	0	Write mask register lists

Table 2: Register Addressing

7 Pin Descriptions

7.1VDD & GND (Power & Ground)

7.2 OSC (Clock Input)
This input signal is used to generate the timing for the MA28137 internal operations and rate of data transfer. The maximum clock input is 20MHz. The internal clock OSC/2 is derived from this signal.

7.3 RDY (Ready)
A logic high on this input signal allows the MA28137 to complete the machine cycle. A low is used to extend the data strobe signal from the MA28137 to accommodate slow memories or I/O peripheral devices.

7.4 DMAE (DMA Enable)
The active high input signal DMA enable from the Central Processing Unit (CPU) indicates that DMA requests from the controller will be acknowledged.

7.5 DMAKN (DMA Acknowledge)
The CPU sets DMAKN low to indicate it has relinquished control of the system busses.

7.6 DMARN (DMA Request)
The DMA Controller requests control of the system bus from the CPU by setting DMARN low. If the corresponding mask bit is clear, the presence of a valid request causes the MA28137 to issue the DMARN to the processor. After DMARN goes active at least one clock cycle must occur before DMAKN goes active.

7.7 AD00 - AD15 (Address / Data Bus)
These connections carry multiplexed addresses and data when the MA28137 has bus control.

7.8 DSN (Data Strobe)
This is a 3-state active low signal. When DMAKN is high, the DSN signal is generated by the system processor. When the DMAKN line is low, the DMA controller produces this signal. In both cases the rising edge of DSN indicates that valid data is present on the AD bus.

7.9 AS (Address Strobe)
This 3-state active high signal functions in a similar way to DSN, except its falling edge indicates the presence of a valid address on the AD bus.

7.10 CSN (Chip Select)
Chip select is an active low input used to select the MA28137 as an I/O device during the idle cycle. This allows the CPU to communicate with the DMA Controller across the data bus.

7.11 RESET (Reset)
Reset is an active high input which clears the command, status, request and temporary registers, and sets the mask register. Following a reset the device is in the idle cycle.

7.12 DREQ 0-3 (DMA Request)
The DMA request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. The polarity of DREQ lines is programmable. Reset initialises them to active high. In fixed priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of the DREQ signal. Polarity of DREQ must be maintained until the corresponding DACK goes active.

7.13 DACK 0-3 (DMA Acknowledge)
DMA Acknowledge outputs are used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. They are initialised to active low by Reset.

7.14 EOPN (End of Process)
End of process is an active low bidirectional signal

The MA28137 allows an external EOP signal to terminate an active DMA service. This is accomplished by pulling the EOPN line low. The MA28137 also generates a pulse when the terminal count (TC) for an channel is reached. This generates an EOP signal which is output through the EOPN line.

The reception of EOP, either internal or external, will cause the MA28137 to terminate the service, reset the request, and, if autoinitialise is enabled, to write the base registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by EOP, unless the channel is programmed for autoinitialise. In that case, the mask bit remains clear. During memory-to-memory transfers, EOP will be output when the TC for channel 1 occurs. EOPN should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.

7.15 RD/WN (Read/Write)
This input signal indicates the direction of data flow to and from the CPU. A logic '1' signifies a read by the processor.

7.16 M/ION (Memory or I/O)
This is an input from the CPU and indicates the type of instruction currently being executed by the processor.

7.17MENN (Memory Enable)
When low, this output signal enables access to the system memory.

7.18 IOENN (Input/Output Enable)
When low, this output signal enables access to the system I/O.

7.19 MRD/WN (Memory Read/Write)
This output signal defines the direction of data transfer to and from the system memory. A logic 1 implies a read from memory, logic 0 a write to memory.

7.20 IORD/WN (Input/Output Read/Write)
This output signal defines the direction of data transfer to and from the system I/O. A logic 1 implies a read from I/O, logic 0 a write to I/O.

7.21M/SN (Master/Slave Mode)
When this output is set to a logical 1 and no DMAK has been issued the controller is in master mode and will generate the system control signals MENN, IOENN, MRD/WN and IORD/W from the incoming signals M/ION and RD/WN. A logical 0 places these outputs in a high impedance state, allowing another controller to drive these lines. See the section on cascade mode for further information.

7.22 AS0-AS3 (Address Status)
These 3-state outputs are used by an MMU during expanded memory access to define the page register set used during DMA transfers.

7.23 PS0-PS3 (Process Status)
These 3-state outputs are used by an MMU during expanded memory access to provide page access protection during DMA transfers.

7.24 IN/OPN (Instruction/Operation)
This is a 3-state output used by an MMU to select the correct page register set.

8 Application Information

Figure 12 shows an example of a DMA system configned with a MA28137 controller and a MAS281 microprocessor. The multimode DMA controller issues a DMAR to the processor whenever there is at least one valid DMA request from a peripheral device. When the processor replies with a DMAK signal, the MA28137 takes control of the address/data bus and the control bus.

The system control signals MENN, IOENN, MRD/WN and IORD/WN are produced by the DMA controller during DMA access. During normal processor action these signals are decoded from M/ION and RD/WN (MAS281 signals) by the MA28137 to reduce the requirement for extra logic.

In this example only one DMAC is shown and this is designated the master DMAC (M/SN pin is tied to logic 1). In a multi-DMAC system only one DMAC would be the master controller, generating the control signals outlined above.

Figure 13 shows the use of the MA28137 in the MAS281 system in combination with a MA17504 MMU/BPU.

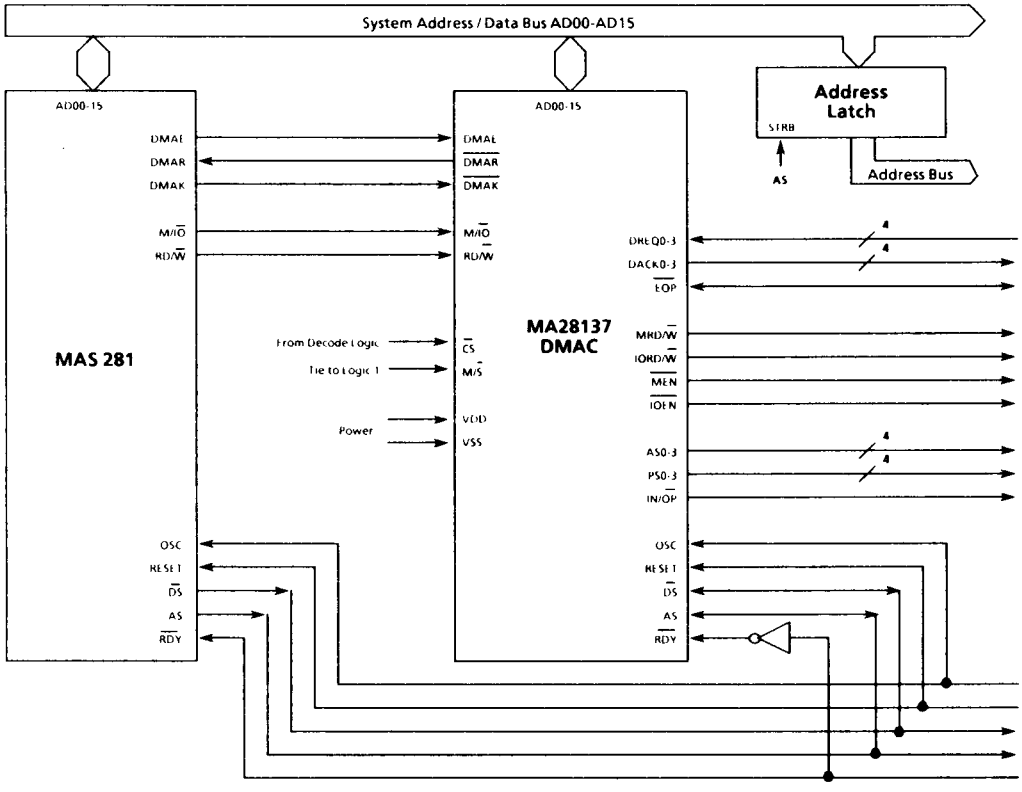


Figure 12: MA28137 - MAS281 System interfacing

MA28137
Radiation Hard Programmable DMA Controller

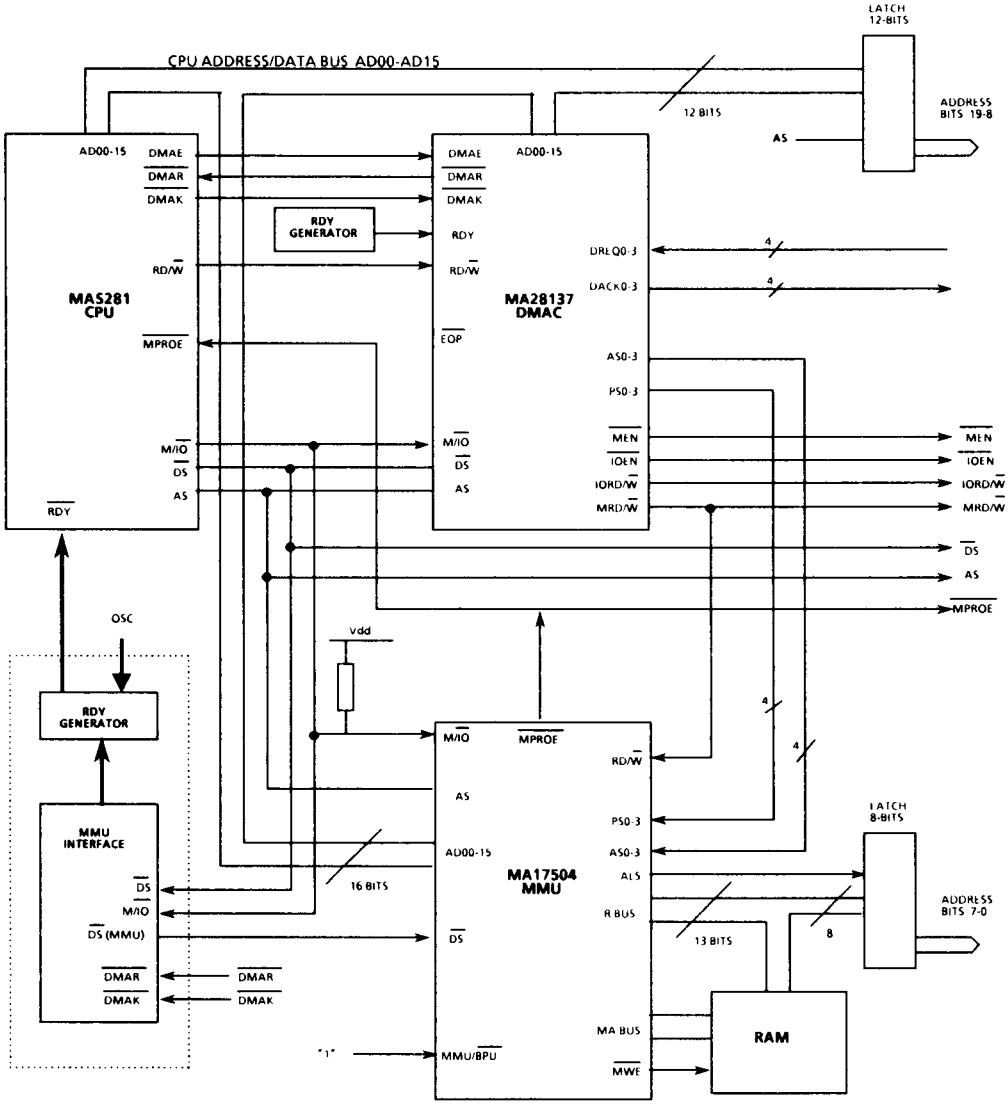


Figure 13: MA28137 - MAS281 with MMU System interfacing

9 Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply voltage	-0 5	10	V
Input voltage	-0 3	V_{DD} + 0 3	V
Current through any pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Table 3: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

10 DC Electrical Characteristics

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^3$ Rad (Si)			Total dose $>3x10^5$ Rad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage	-	4 5	5 0	5 5	4 5	5 5	V
V_{IH}	Input high voltage	-	2 0	-	-	2 0	-	V
V_{IL}	Input low voltage	-	-	-	0 8	-	0 3	V
V_{OH}	Output high voltage	I_{OH} = -0 8mA	2 4	-	-	2 4	-	V
V_{OL}	Output low voltage	I_{OL} = 2 0mA	-	-	0 4	-	0 4	V
I_{IL}	Input leakage current	$V_{IN} = V_{SS}$ or V_{DD}	-	-	± 10	-	± 100	uA
I_{OL}	Output leakage current	$V_{O(H)} = V_{SS}$ or V_{DD}	-	-	± 50	-	± 100	uA
I_{DD}	Power supply current	Static	-	-	1 0	-	10 0	mA

V_{DD} = 5V ± 10%, over full operating temperature range

Table 4: Operating DC Electrical Characteristics

11 AC Electrical Characteristics

Number	Parameter	Min.	Max.	Units
t_1	V_{DD} applied to RESET falling	100	-	us
t_2	RESET pulse width	100	-	ns
t_3	RESET to first Program	100	-	ns
t_4	Address strobe width	70	-	ns
t_5	Data strobe width	70	-	ns
t_6	Address setup to AS lo (write)	20	-	ns
t_7	Address hold after AS lo (write)	0	-	ns
t_8	Data setup to DS hi (write)	20	-	ns
t_9	Data hold after DS hi (write)	0	-	ns
t_{10}	Chip Select lo to AS lo setup time	50	-	ns
t_{11}	Address setup to AS lo (read)	20	-	ns
t_{12}	Address hold after AS lo (read)	0	-	ns
t_{13}	NOT USED	-	-	-
t_{14}	Data valid after DS lo (read)	38	90	ns
t_{15}	Data valid after DS hi (read)	12	32	ns
t_{16}	RD/W lo to MRD/W, IORD/W lo (Non-DMA)	-	42	ns
t_{17}	M/IO lo to MEN, IOEN lo (Non-DMA)	-	37	ns
t_{18}	DREQ active to OSC hi	-	45	ns
t_{19}	Osc hi to DMAR lo	-	50	ns
t_{20}	Osc hi to DMAR hi	-	50	ns
t_{21}	Osc hi to DACK active	-	52	ns
t_{22}	Osc hi to DACK inactive	-	52	ns
t_{23}	Dmakn lo to Osc hi	-	40	ns
t_{24}	AS hi-Z to AS hi after Osc hi	-	55	ns
t_{25}	Osc hi to AS lo	-	55	ns
t_{26}	Osc hi to AS hi	-	55	ns
t_{27}	DS hi-Z to DS lo after Osc hi	-	55	ns
t_{28}	Osc hi to DS lo	-	55	ns
t_{29}	Osc hi to DS hi	-	55	ns
t_{30}	Osc hi to MEN lo	-	48	ns
t_{31}	Osc hi to MEN hi	-	48	ns
t_{32}	Osc hi to IOEN lo	-	40	ns

Table 5: AC Electrical Characteristics

Number	Parameter	Min.	Max.	Units
t_{33}	Osc hi to IOEN hi	-	40	us
t_{34}	Osc hi to MRD/W lo	-	48	ns
t_{35}	Osc hi to MRD/W hi	-	48	ns
t_{36}	Osc hi to IORD/W hi	-	48	ns
t_{37}	Osc hi to IORD/W lo	-	48	ns
t_{38}	Osc hi to Address valid (first AS)	-	110	ns
t_{39}	Osc hi to Address valid (thereafter)	-	60	ns
t_{40}	Osc hi to Address hi-Z	-	75	ns
t_{41}	Osc hi to EOPB lo	-	60	ns
t_{42}	Osc hi to EOPB hi-Z	-	60	ns
t_{43}	Osc hi to EOPB lo	-	90	ns
t_{44}	Osc hi to Address valid (first AS)	-	110	ns
t_{45}	Osc hi to Address hi-Z	-	60	ns
t_{46}	Data-in valid to Osc hi	0	-	ns
t_{47}	Osc hi to Data-in hi-Z	10	-	ns
t_{48}	Osc hi to MRD/W lo	-	50	ns
t_{49}	Osc hi to DS hi	-	55	ns
t_{50}	Osc hi to DS hi	-	55	ns
t_{51}	Osc hi to Address valid	-	110	ns
t_{52}	Osc hi to Address hi-Z	-	75	ns
t_{53}	Osc hi to Data-out valid	-	65	ns
t_{54}	Osc hi to Data-out hi-Z	-	80	ns
t_{55}	READY lo to Osc hi	8	-	ns
t_{56}	READY hi to Osc hi	8	-	ns

Table 5: AC Electrical Characteristics cont.

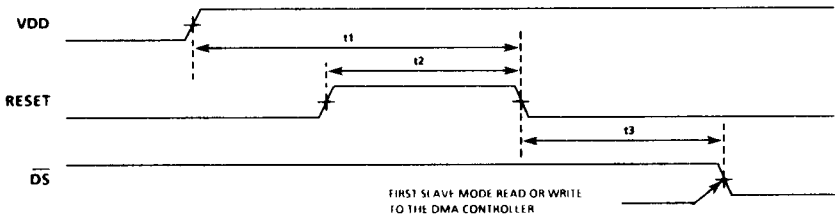


Figure 14: RESET timing

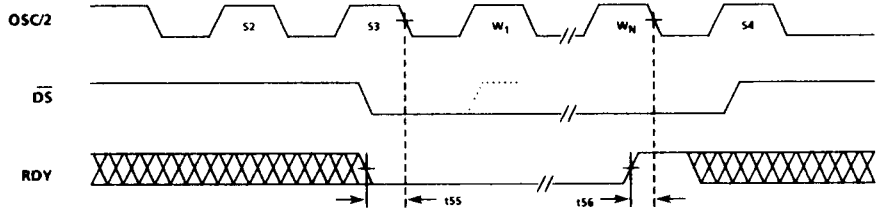


Figure15: READY Timing

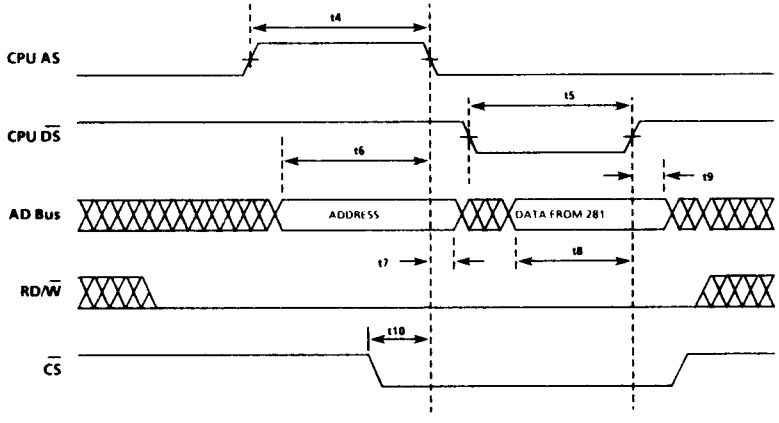


Figure 16: Programme mode CPU write timing

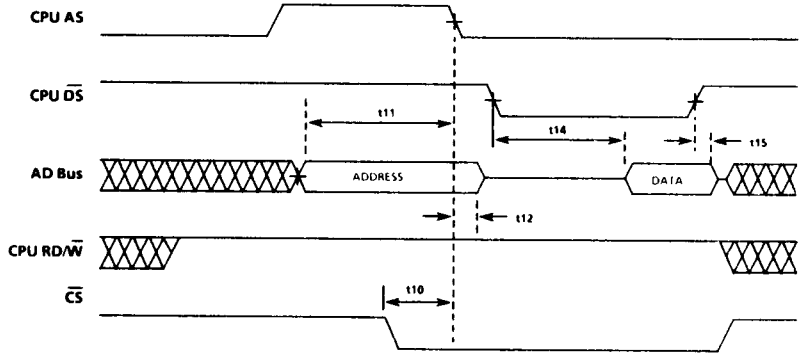


Figure 17: Programme mode CPU read timing

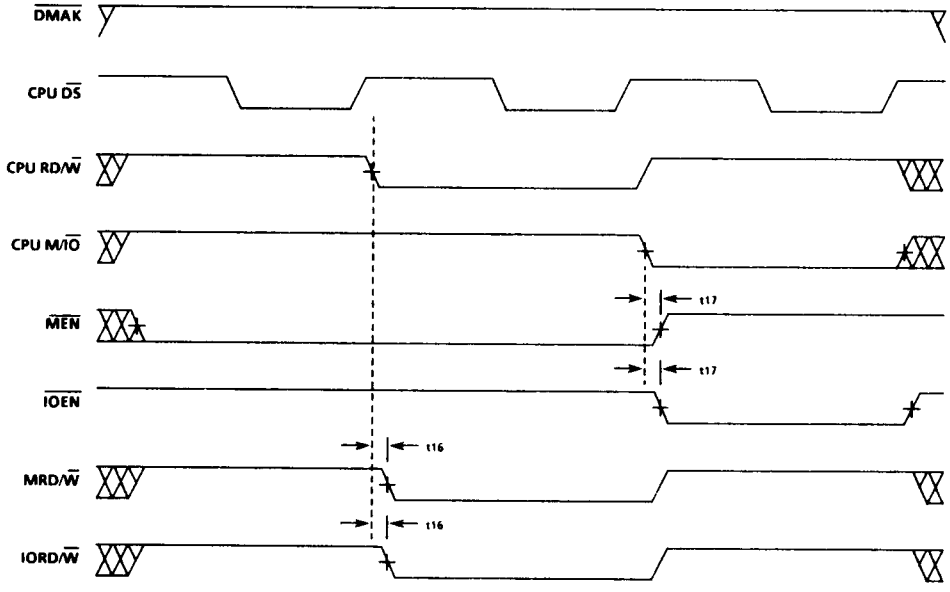
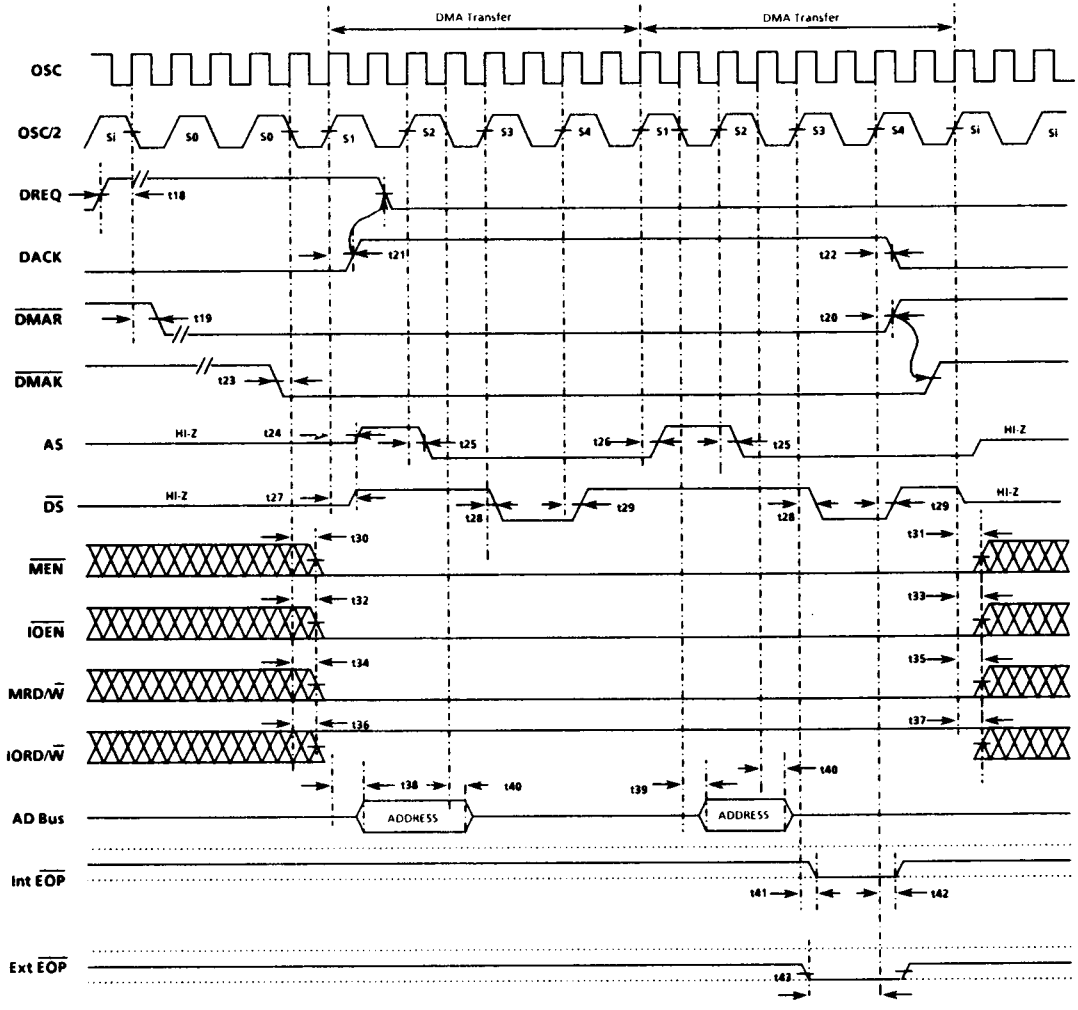


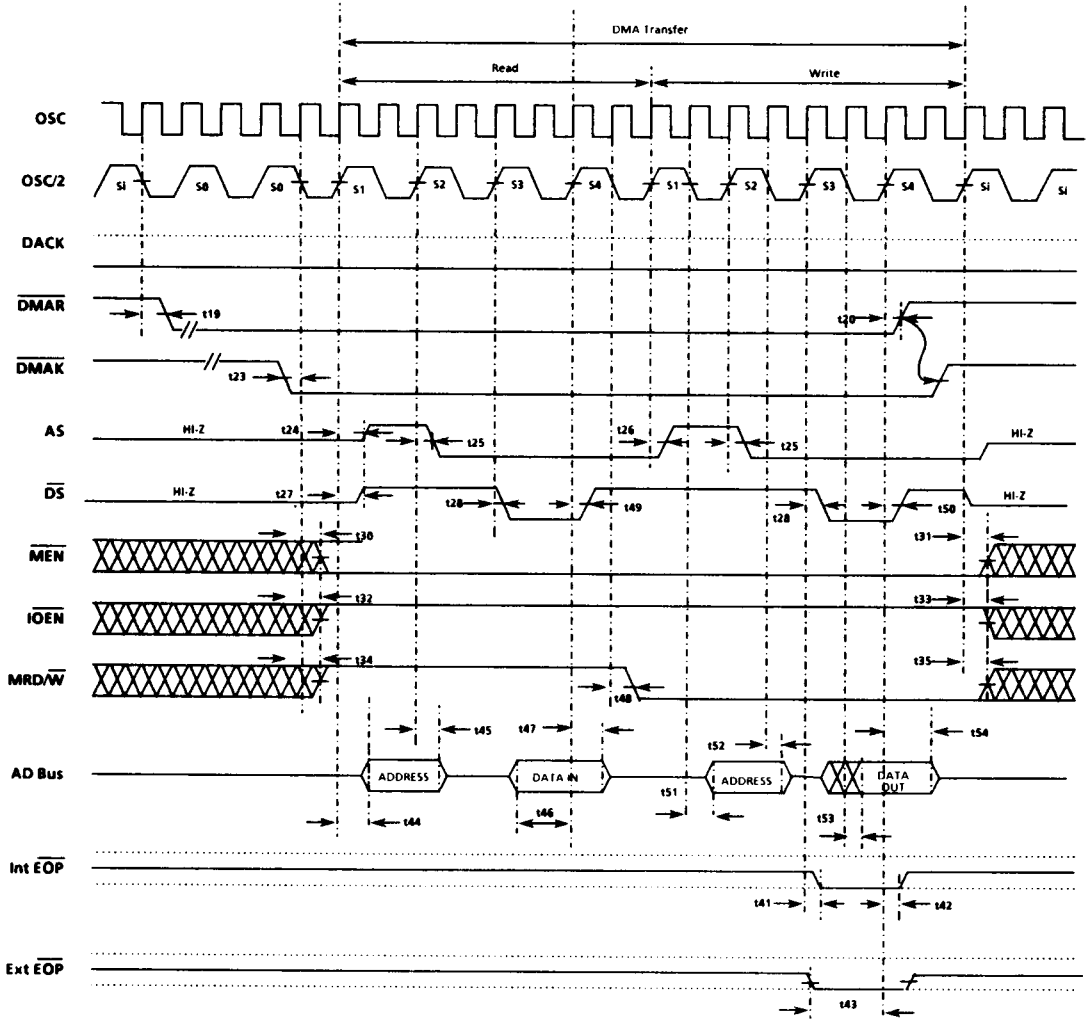
Figure 18: Memory and IO control signal timing (Non-DMA)



NOTES:

1. OSC/2 is internally generated from the input signal OSC.
2. This diagram shows a peripheral to memory transfer. The control signals MRD/W and IORD/W are in the opposite state for a memory to peripheral transfer.

Figure 19: DMA transfer timing, IO to memory.

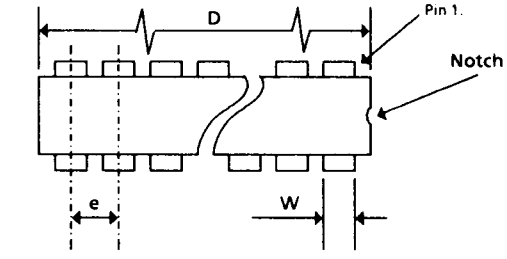


NOTES:

1. A memory to memory transfer is initiated by setting a software DREQ for channel 0
2. OSC/2 is internally generated from the input signal OSC

Figure 20: DMA transfer timing, memory to memory.

12 Packaging Information



Ref.	Min.	Nom.	Max.
A			5.60 (0.220)
A_1	0.38 (0.015)		1.53 (0.060)
b	0.35 (0.014)		0.59 (0.023)
c	0.20 (0.008)		0.36 (0.014)
D			82.10 (3.232)
e		2.54 (0.100) typ	
e_1		23.52 (0.900) typ	
H	4.71 (0.185)		5.38 (0.212)
M_E			23.52 (0.900)
Dimensions in mm (inches)			

MEDL XG413

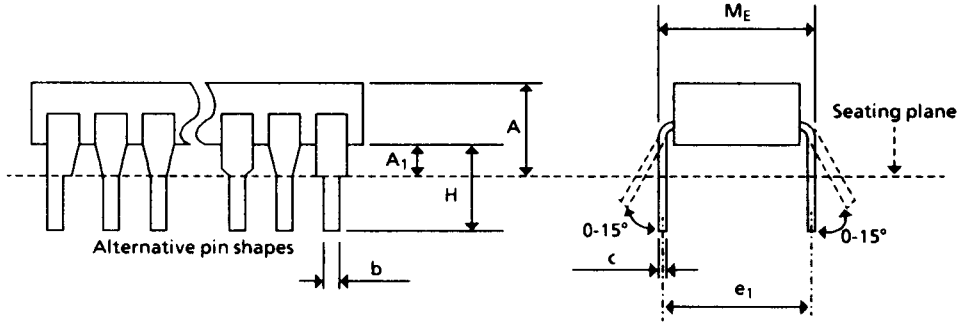


Figure 21a: 64-Lead Ceramic DIL (solder seal) - package style C

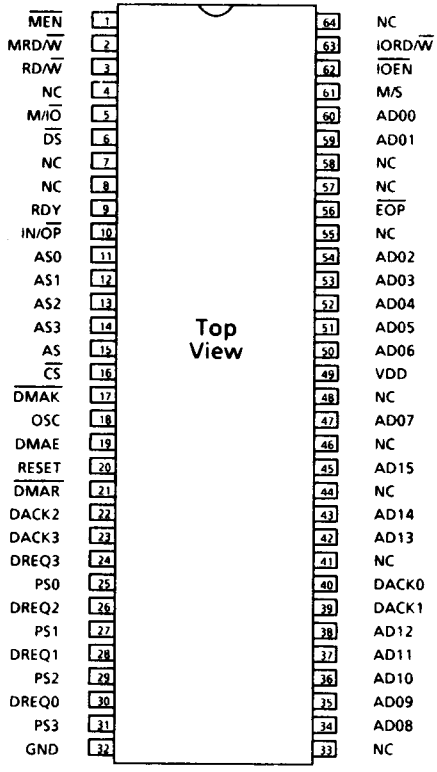
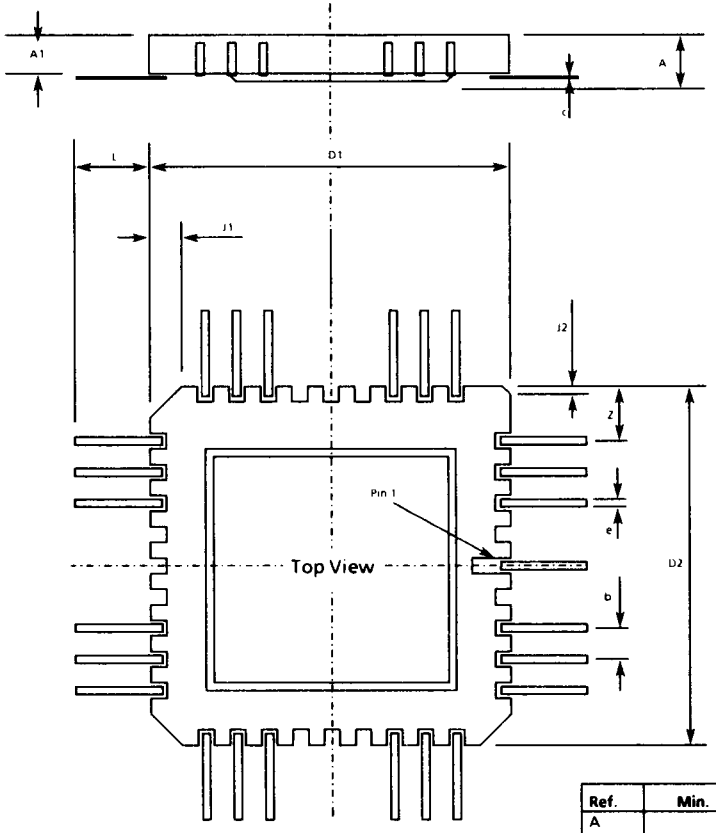


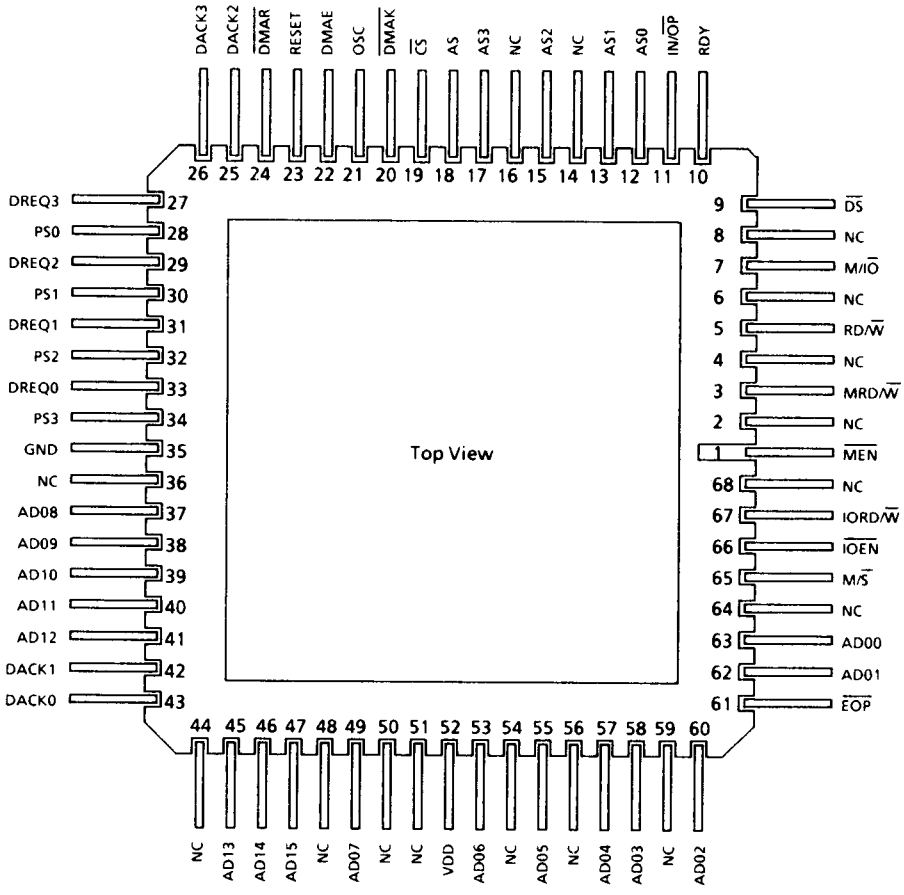
Figure 21b: 64-Lead Ceramic DIL (solder seal) - package style C



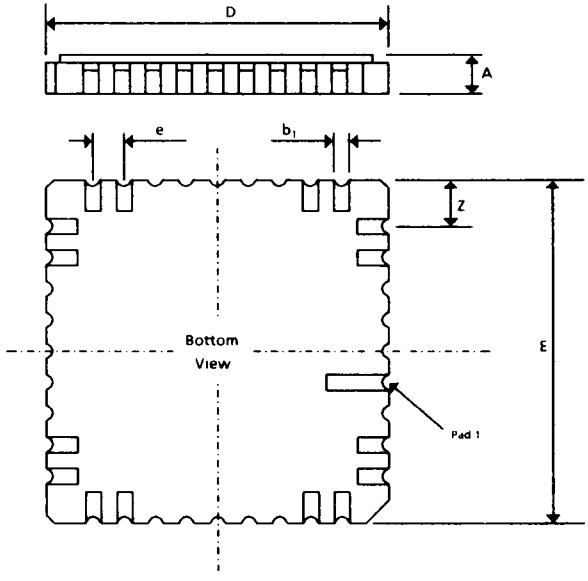
Ref.	Min.	Nom.	Max.
A			2.59 (0.102)
A_1	1.83 (0.072)		2.24 (0.088)
b	0.25 (0.010)		0.36 (0.014)
c	0.10 (0.004)		0.20 (0.008)
D1 D2	23.88 (0.940)		24.51 (0.965)
e		2.54 (0.050)	
j1		1.02 (0.040)	
j2		0.51 (0.020)	
L	8.89 (0.350)		25.85 (0.445)
Z	1.65 (0.065)		2.16 (0.085)
Dimensions in mm (inches)			

MEDL XG491

Figures 22a: 68-Lead Topbraze Flatpack (Package style F)



Figures 22b: 68-Lead Topbraze Flatpack (Package style F)



Ref.	Min.	Nom.	Max.
A	1.78 (0.070)	-	2.08 (0.082)
b_1	-	0.51 (0.020)	-
D	18.08 (0.712)	-	18.62 (0.733)
E	18.08 (0.712)	-	18.62 (0.733)
e	-	1.02 (0.040)	-
Z	1.40 (0.055)	-	1.78 (0.070)

Dimensions in mm (inches)

MEDL XG493

Figure 23a. 64-pad Leadless Chip Carrier (Package style L)

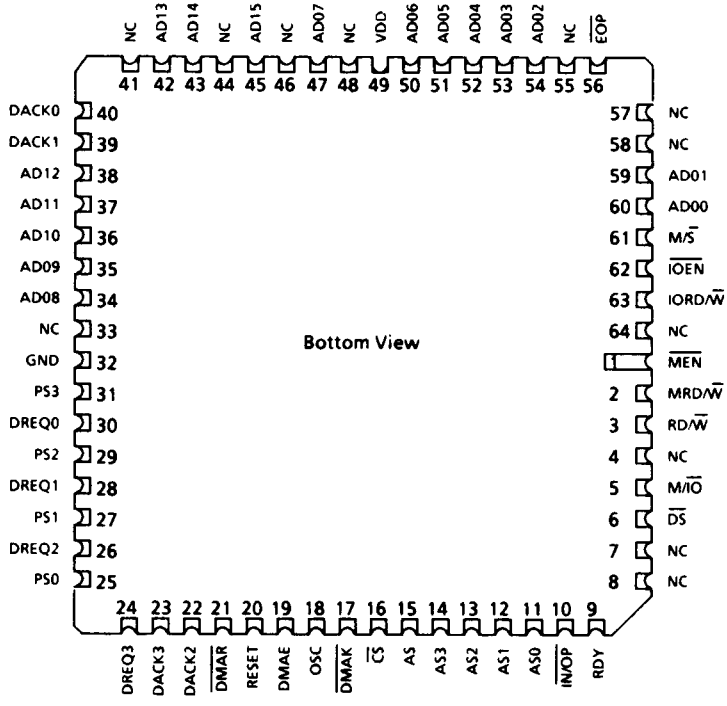


Figure 23b. 64-pad Leadless Chip Carrier (Package style L)

MA28137

Radiation Hard Programmable DMA Controller

13 Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification, note 1)	$1x10^6$ Rad(Si)
Total Dose (Function to specification, note 2)	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	3×10^{10} Rad(Si)/sec
Transient Upset (Survivability)	$>1 \times 10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	1×10^{15} neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

Notes: 1. Circuits with all inputs 'CMOS' types
2. Circuits with 'TTL' type inputs

3

14 Ordering Information

Unique circuit designator.

MAx28137xxxxx

Radiation Tolerance

- S Radiation hard processing
- R 100 kRads (Si) guaranteed
- Q 300 kRads (Si) guaranteed
- H 1000 kRads (Si) guaranteed

Package Type

- C Ceramic DIL (solder seal)
- F Flatpack (solder seal)
- L Leadless Chip Carrier
- N Naked Die

QA/QCI Process (see section 9, part 4)

Test Process (see section 9, part 3)

Assembly Process (see section 9, part 2)

Reliability Level

- L Rel 0
- C Rel 1
- D Rel 2
- E Rel 3/4/5/STACK
- B Class B
- S Class S

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.