TC54H1000AP/AF-85, -100
TC54H1001AP/AF-85, -100

SILICON STACKED GATE CMOS

131,072 WORD x 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

Description

The TC54H1000AP/AF and the TC54H1001AP/AF are 131,072 word x 8 bit CMOS one time programmable read only memories molded in 32-pin plastic packages.

The TC54H1000AP/AF and TC54H1001AP/AF access times are 85ns/100ns. They have a low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as for the TC57H1000AD/TC57H1001AD UV EPROMs. Once programmed, the TC54H1000AP/AF and TC54H1001AP/AF cannot be erased because of the use of a plastic package without a transparent window.

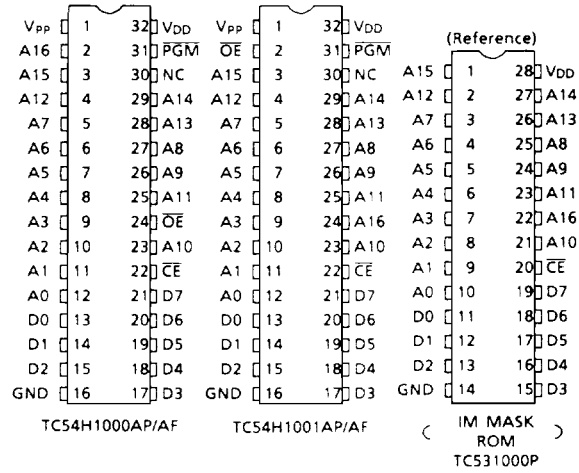
Features

- Peripheral circuit : CMOS
  Memory cell : NMOS
- Access time

	-85	-10
t_{ACC}	85ns	100ns
Temp	0 ~ 70°C	

- Low power dissipation
  - Active : 40mA/11.8MHz
  - Standby : 100μA
- Single 5V power supply
- Fully static operation
- High speed programming mode : t_{PW} = 0.1ms
- Inputs and outputs TTL compatible
- JEDEC standard 32-pin : TC54H1000AP/AF
- 1M MROM compatible : TC54H1001AP/AF
- Package
  - TC54H1000AP/TC54H1001AP : DIP32-P-600
  - TC54H1000AF/TC54H1001AF : SOP32-P-525

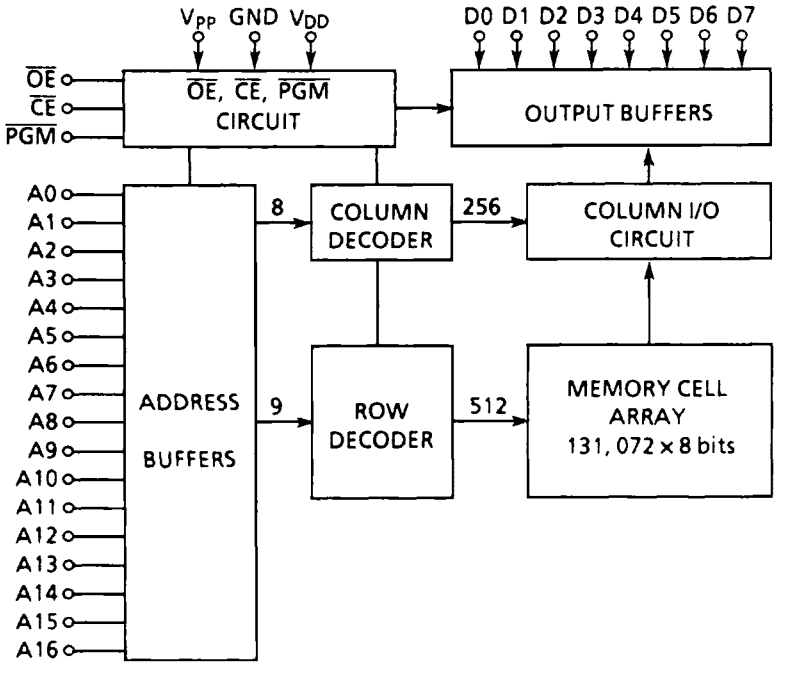
Pin Connection (Top View)



Pin Names

A0 ~ A16	Address Inputs
D0 ~ D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{DD}	Power Supply Voltage (+5V)
V_{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

Block Diagram



Operating Mode

MODE \ PIN	PGM	CE	OE	V_{PP}	V_{DD}	D0 ~ D7	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ~ 14.0	
V_{IN}	Input Voltage	-0.6 ~ 7.0	
$V_{I/O}$	Input/Output Voltage	-0.6 ~ V_{DD} + 0.5	
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 125	°C
T_{OPR}	Operating Temperature	0 ~ 70	

Read Mode

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	
V_{DD}	Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	Program Supply Voltage	V_{DD} - 0.6	V_{DD}	V_{DD} + 0.6	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±10	µA
I_{DDO1}	Operating Current	$\overline{CE}$ = 0V, I_{OUT} = 0mA	f = 11.8MHz	–	–	40	mA
I_{DDO2}			f = 1MHz	–	–	15	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	1	
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V		–	–	100	µA
V_{OH}	Output High Voltage	I_{OH} = -400µA		2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		–	–	0.4	
I_{PP1}	V_{PP} Current	V_{PP} = V_{DD}±0.6V		–	–	±10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V ~ V_{DD}		–	–	±10	

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±5%, V_{PP} = V_{DD}±0.6V)

SYMBOL	PARAMETER	TC54H1000AP-85/TC54H1001AP-85 TC54H1000AF-85/TC54H1001AF-85		TC54H1000AP-10/TC54H1001AP-10 TC54H1000AF-10/TC54H1001AF-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	–	85	–	100	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	85	–	100	
t_{OE}	$\overline{OE}$ to Output Valid	–	45	–	50	
t_{PGM}	$\overline{PGM}$ to Output Valid	–	45	–	50	
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	30	0	40	
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	30	0	40	
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	30	0	40	
t_{OH}	Output Data Hold Time	0	–	0	–	

AC Test Conditions

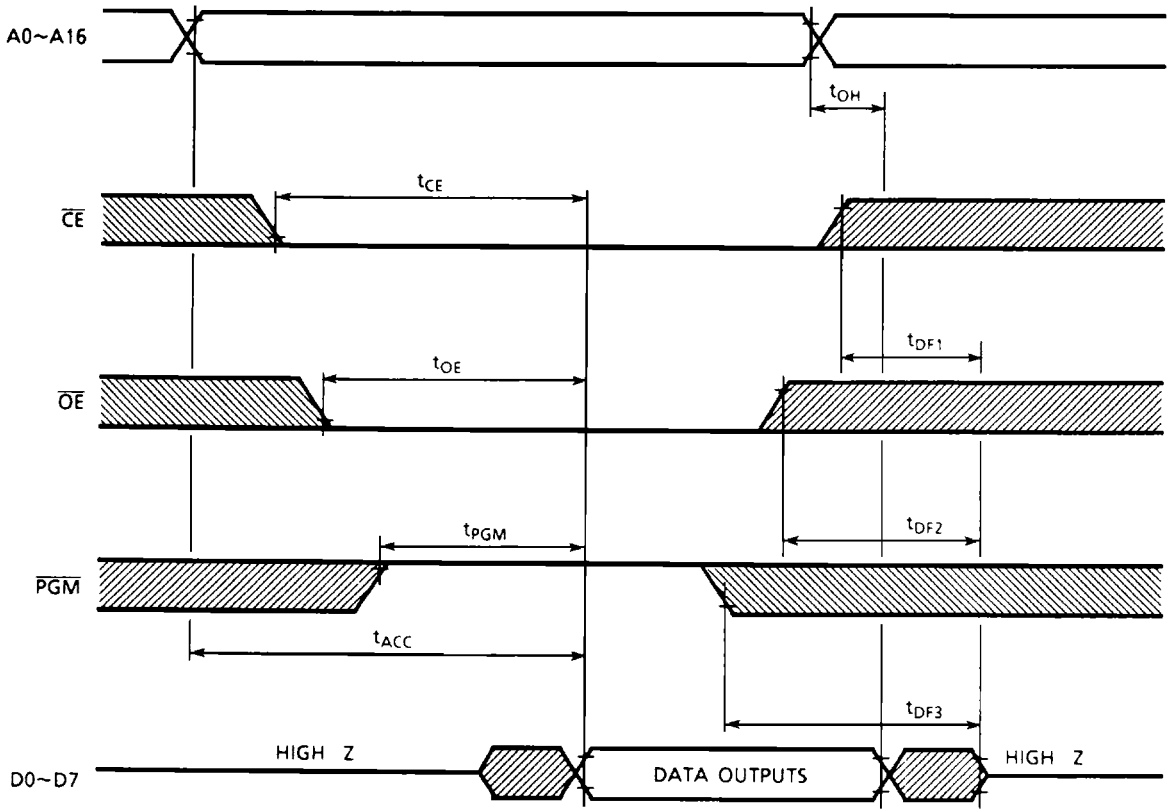
Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	16	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	16	

*This parameter is periodically sampled and is not 100% tested.

Timing Waveforms (Read)



High Speed Programming Mode

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 1.0	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	
V_{DD}	Power Supply Voltage	6.00	6.25	6.50	
V_{PP}	Program Supply Voltage	12.50	12.75	13.00	

DC Characteristics (Ta = 25±5°C, V_{DD} = 6.25V±0.25V, V_{PP} = 12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	–	±10	μA
V_{OH}	Output High Voltage	I_{OH} = -400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	
I_{DD}	V_{DD} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 13.0V	–	–	50	

AC Programming Characteristics (Ta = 25±5°C, V_{DD} = 6.25V±0.25V, V_{PP} = 12.75V±0.25V)

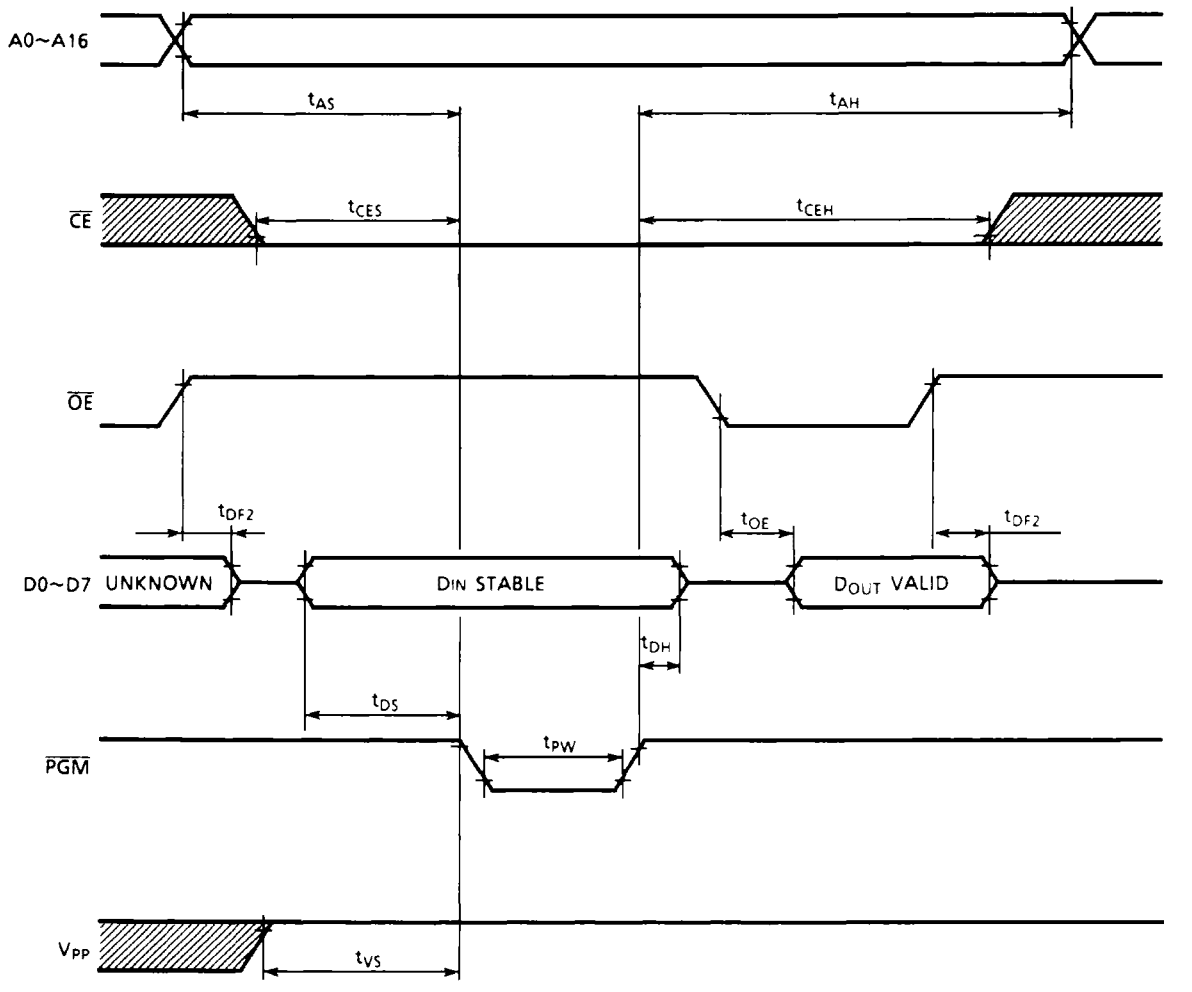
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	
t_{DS}	Data Setup Time	–	2	–	–	
t_{DH}	Data Hold Time	–	2	–	–	
t_{VS}	V_{PP} Setup Time	–	2	–	–	
t_{PW}	Program Pulse Width	–	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IL}	–	–	90	

AC Test Conditions

Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

Timing Waveforms (Program)

High Speed Programming Mode



Notes:

1. V_{DD} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from a programming socket and replacing the device in the socket while V_{PP} = 12.75V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted to be up to 14V for programming. Voltages over 14V should not be applied to the V_{PP} terminal. When the programming voltage is applied to the V_{PP} terminal, the overshoot voltage should not exceed 14V.

Operation Information

The TC54H1000AP/AF/TC54H1001AP/AF's six operating modes are listed in the following table.
Mode selection is achieved by applying TTL level signals to appropriate inputs.

MODE \ PIN		$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	D0 ~ D7	POWER
Read Operation (Ta = 0 ~ 70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
Program Operation (Ta = 25±5°C)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Notes: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

Read Mode

The TC54H1000AP/AF/TC54H1001AP/AF has three control inputs. The chip enable ($\overline{CE}$) input controls the operating power and should be used for device selection. The output enable ($\overline{OE}$) and program control ($\overline{PGM}$) inputs control the output buffers.

Assuming that $\overline{CE}$ = $\overline{OE}$ = V_{IL} and $\overline{PGM}$ = V_{IH}, once the address has stabilized, output data will be valid after the address access time has elapsed. The $\overline{CE}$ to output valid time (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH} and that the address has been stable for at least t_{ACC}, then output data will be valid after t_{OE} from the falling edge of $\overline{OE}$. And assuming that $\overline{CE}$ = $\overline{OE}$ = V_{IL} and that all address lines have been stable, then output data is valid after t_{PGM} from the rising edge of $\overline{PGM}$.

Output Deselect Mode

If $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, the outputs will be in a high impedance state.

Therefore, two or more devices can be connected together on a common bus if the output of only one device is enabled. When $\overline{CE}$ is used for device selection, all deselected devices are in the low power standby mode.

Standby Mode

The TC54H1000AP/AF/TC54H1001AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a MOS high level voltage (V_{DD}) to the $\overline{CE}$ input, the TC54H1000AP/AF/TC54H1001AP/AF is placed in the standby mode which reduces the operating current to 100μA and puts the outputs in a high impedance state, independent of the $\overline{OE}$ input.

Program Mode

When the TC54H1000AP/AF/TC54H1001AP/AF is initially received by customers, all bits of the device are in the "1" state, which is the erased state. Therefore, the object of the program operation is to introduce "0" data into the desired bit locations.

The TC54H1000AP/AF/TC54H1001AP/AF is in the programming mode when V_{PP} = 12.75V, $\overline{PGM}$ = $\overline{CE}$ = V_{IL}, and $\overline{OE}$ = V_{IH}.

The TC54H1000AP/AF/TC54H1001AP/AF can be programmed at any address location at any time - either individually, sequentially, or at random.

Program Verify Mode

The verify mode is used to check that the desired data has been correctly programmed. The verify mode is activated when $\overline{OE}$ = $\overline{CE}$ = V_{IL} and $\overline{PGM}$ = V_{IH}.

Program Inhibit Mode

When the programming voltage (+12.75V) is applied to the V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC54H1000AP/AF/TC54H1001AP/AF from being programmed.

The programming of two or more EPROMs in parallel with different data is easily accomplished. All inputs except for $\overline{CE}$ and $\overline{PGM}$ may be commonly connected, then a TTL low level program pulse is applied to $\overline{CE}$ and $\overline{PGM}$ of the desired device only while a TTL high level signal is applied to the $\overline{CE}$ of the other devices.

High Speed Programming Mode

The device is set up in high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{DD} = 6.25V and $\overline{PGM}$ = V_{IH}.

Programming is achieved by applying a single 0.1ms TTL low level pulse to the $\overline{PGM}$ input after addresses and data are

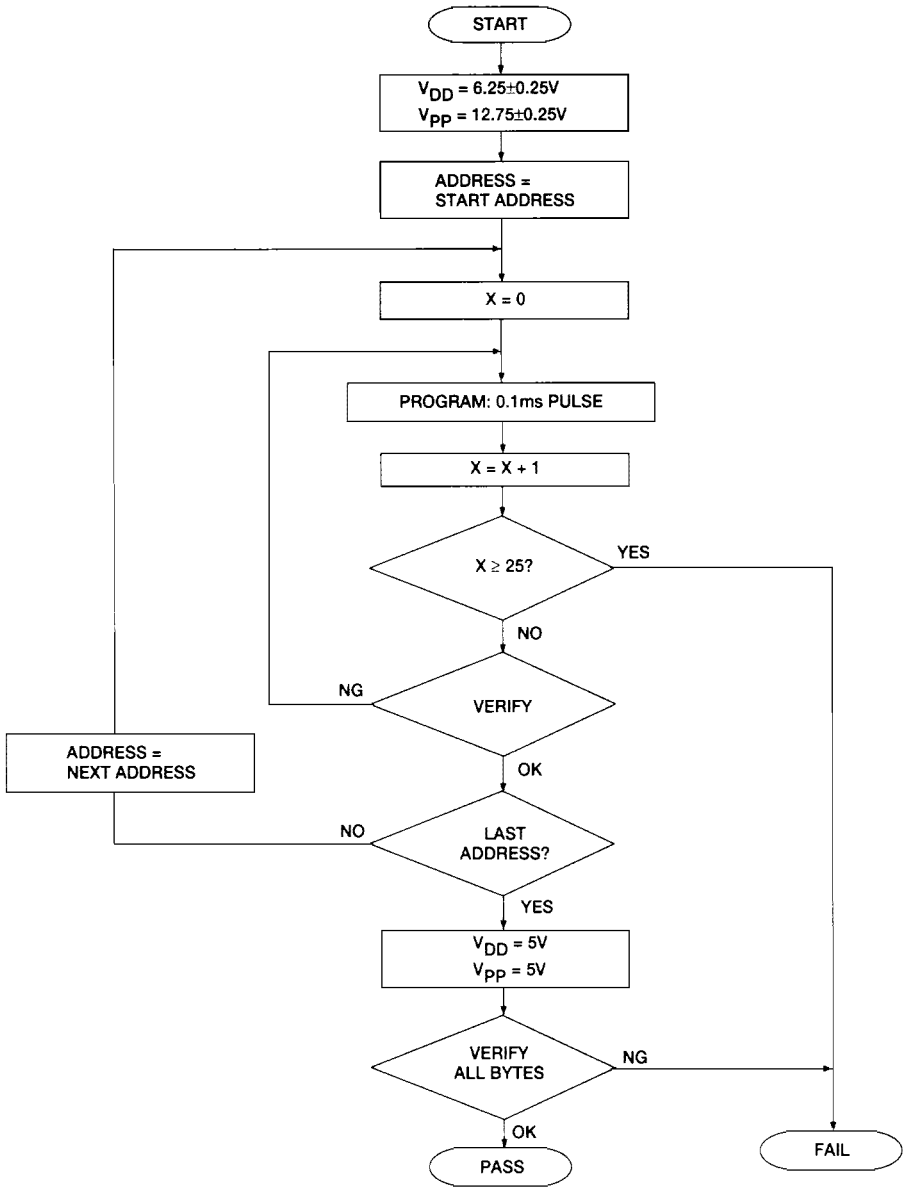
stable. Then the programmed data is verified by using the program verify mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then the programmed data is verified. This should be repeated until the data has programmed correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{DD} = V_{PP} = 5V$.

High Speed Programming Mode

Flow Chart



Electric Signature Mode

The electric signature mode allows one to read out a code from the TC54H1000AP/AF/TC54H1001AP/AF which identifies its manufacturer and device type.

The programming equipment may read out the manufacturer code and device code from the TC54H1000AP/AF/TC54H1001AP/AF by using this mode before programming and automatically set the programming voltage (V_{PP}) and algorithm.

The electric signature mode is set up when 12V is applied to address line A9 and the rest of the address lines are set to V_{IL} during a read operation. Data output under these conditions is the manufacturer code. The device code is output when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit being the MSB (D7). The following table shows the electric signature of the TC54H1000AP/AF/TC54H1001AP/AF.

SIGNATURE / PINS		A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacturer Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC54H1000AP/AF	V_{IH}	1	0	0	0	0	1	1	0	86
	TC54H1001AP/AF		0	0	0	0	0	1	1	1	07

Notes: A9 = 12V±0.5V
A1 ~ A8, A10 ~ A16, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}