MSM514410B/BL

1,048,576-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE (WRITE PER BIT)

DESCRIPTION

The MSM514410B/BL is a new generation dynamic RAM organized as 1,048,576-word × 4-bit. The technology used to fabricate the MSM514410B/BL is OKI's CMOS silicon gate process technology. The device operates at a single 5V power supply. Its I/O pins are TTL compatible.

FEATURES

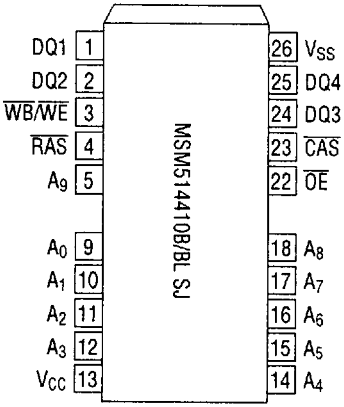
- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 1,048,576-word × 4-bit organization
- Single 5V power supply, ±10% tolerance
- Input :TTL compatible
- Output :TTL compatible, tristate
- Refresh :1024 cycles/16ms, 1024 cycles/128ms (L-version)
- Fast page, write per bit mode capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh, $\overline{\text{RAS}}$-only refresh capability
- Multibit test mode capability
- Package:

26-Pin 300mil	Plastic SOJ	(SOJ26-P-300)
20-Pin 400mil	Plastic ZIP	(ZIP20-P-400)
26-Pin 300mil	Plastic TSOP	(TSOP26-P-300-K) (TSOP26-P-300-L)

PRODUCT FAMILY

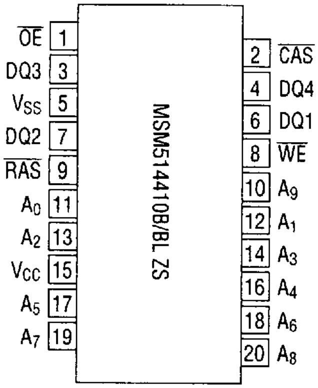
Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM514410B/BL-60	60ns	30ns	15ns	15ns	110ns	550mW	5.5mW/ 1.1mW (L-version)
MSM514410B/BL-70	70ns	35ns	20ns	20ns	130ns	495mW	
MSM514410B/BL-80	80ns	40ns	20ns	20ns	150ns	440mW	
MSM514410B/BL-10	100ns	50ns	25ns	25ns	180ns	385mW	

PIN CONFIGURATION (TOP VIEW)

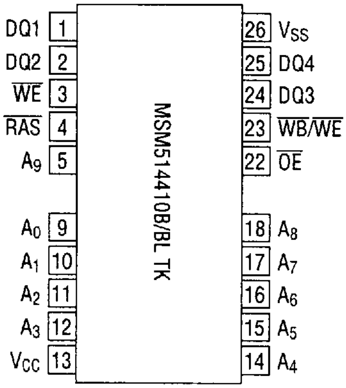


26-PIN SOJ

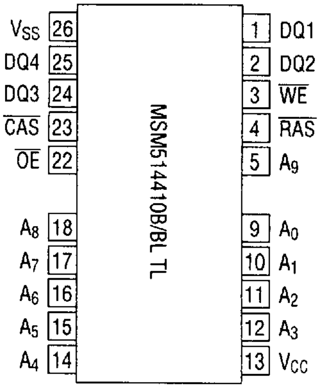
SJ=300mil



20-PIN ZIP



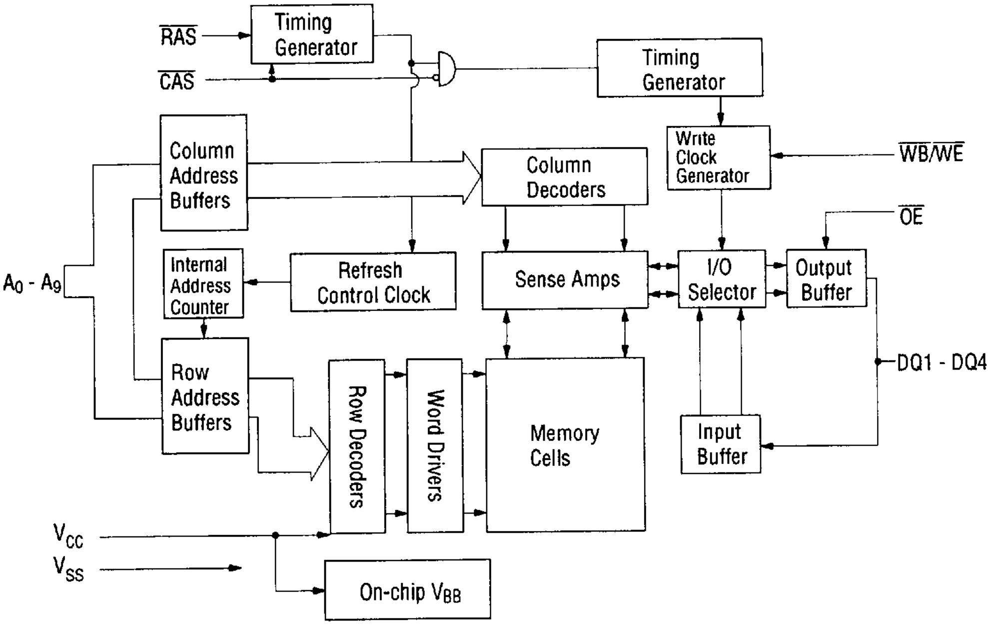
26-PIN TSOP
(K TYPE)



26-PIN TSOP
(L TYPE)

Pin Name	Function
A_0 - A_9	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
DQ1 - DQ4	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WB}}/\overline{\text{WE}}$	Write Enable
V_{CC}	Power Supply (5V)
V_{SS}	Ground (0V)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	–1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	–1.0	—	0.8	V

Capacitance

(V_{CC} = 5V ± 10%, Ta = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 - A_9, D_{IN})	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ4)	$C_{I/O}$	—	7	pF

DC Characteristics

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MSM514410 B/BL-60		MSM514410 B/BL-70		MSM514410 B/BL-80		MSM514410 B/BL-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V ≤ V_I ≤ 6.5V; All Other Pins Not Under Test = 0V	−10	10	−10	10	−10	10	−10	10	µA	
Output Leakage Current	I_{LO}	DQ_i Disable 0V ≤ V_O ≤ 5.5V	−10	10	−10	10	−10	10	−10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ Cycling, t_{RC} = Min.	—	100	—	90	—	80	—	70	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = V_{IH}	—	2	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ ≥ V_{CC} −0.2V	—	1	—	1	—	1	—	1		
			—	200	—	200	—	200	—	200	µA	5
Average Power Supply Current ($\overline{\text{RAS}}$-only Refresh)	I_{CC3}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}}$ = V_{IH} t_{RC} = Min.	—	100	—	90	—	80	—	70	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{\text{RAS}}$ = V_{IH} $\overline{\text{CAS}}$ = V_{IL} DQ_i = Enable	—	5	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	I_{CC6}	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$	—	100	—	90	—	80	—	70	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{\text{RAS}}$ = V_{IL}, $\overline{\text{CAS}}$ Cycling t_{PC} = Min.	—	80	—	80	—	70	—	60	mA	1, 3
Average Power Supply Current (Battery Backup)	I_{CC10}	t_{RC} = 125µs $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ $\overline{\text{RAS}}$ Cycling t_{RAS} = 125µs	—	300	—	300	—	300	—	300	µA	1, 2, 4, 5

Notes :
1. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{\text{RAS}}$ = V_{IL}.
3. Address can be changed once or less while $\overline{\text{CAS}}$ = V_{IH}.
4. V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V, −1.0V ≤ V_{IL} ≤ 0.2V.
5. L-version.

AC Characteristics (1/2)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 11, 12

Parameter	Symbol	MSM514410 B/BL-60		MSM514410 B/BL-70		MSM514410 B/BL-80		MSM514410 B/BL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
Read Modify Write Cycle Time	t_{RMW}	150	—	180	—	200	—	240	—	ns	
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	60	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRMW}	80	—	95	—	100	—	120	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	35	—	40	—	50	ns	4, 6
Access Time from $\overline{OE}$	t_{OEA}	—	15	—	20	—	20	—	25	ns	4
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	—	45	—	55	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	0	—	ns	
Output Buffer Turn-off Delay Time	t_{OFF}	0	15	0	20	0	20	0	25	ns	7
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	20	0	20	0	20	0	25	ns	7
Transition Time	t_T	3	50	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	
Refresh Period (L-version)	t_{REF}	—	128	—	128	—	128	—	128	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	t_{ROH}	15	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	50	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	50	—	55	—	60	—	75	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	50	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 11, 12

Parameter	Symbol	MSM514410 B/BL-60		MSM514410 B/BL-70		MSM514410 B/BL-80		MSM514410 B/BL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	0	—	ns	8
Read Command Hold Time Reference to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	10	—	10	—	10	—	15	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	15	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t_{WCR}	45	—	50	—	60	—	75	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t_{OEH}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	ns	10
Data-in Hold Time from $\overline{\text{RAS}}$	t_{DHR}	50	—	55	—	60	—	75	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t_{OED}	15	—	20	—	20	—	25	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{CWD}	35	—	45	—	45	—	55	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t_{AWD}	50	—	60	—	65	—	80	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{RWD}	80	—	95	—	105	—	130	—	ns	9
$\overline{\text{CAS}}$ Active Delay from $\overline{\text{RAS}}$ Precharge	t_{RPC}	5	—	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$)	t_{CSR}	5	—	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Refresh Counter Test)	t_{CPT}	30	—	35	—	40	—	50	—	ns	
Write-per Bit Set-up time	t_{WBS}	0	—	0	—	0	—	0	—	ns	13
Write-per Bit Hold time	t_{WBH}	10	—	10	—	10	—	10	—	ns	13
Write-per Bit Selection Set-up Time	t_{WDS}	0	—	0	—	0	—	0	—	ns	13
Write-per Bit Selection Hold Time	t_{WDS}	10	—	10	—	10	—	10	—	ns	13
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$)	t_{WRP}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$)	t_{WRH}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode)	t_{WSR}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode)	t_{WHR}	10	—	10	—	10	—	10	—	ns	

Notes:

1. An initial pause of 200μs is required after power-up followed by eight or more initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is achieved. In case of using internal refresh counter, eight or more $\overline{CAS}$ before $\overline{RAS}$ initialization cycles is required.

2. The AC characteristics assume t_T = 5ns.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels of input signals for timing measurement. Transition times are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2 TTL loads and 100pF.

5. Operating within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.

6. Operation within the t_{RAD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled exclusively by t_{AA}.

7. t_{OFF} (Max.) and t_{OEZ} (Max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8. Either t_{RRH} of t_{RCH} must be satisfied for a read cycle.

9. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (Min.) the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), $t_{CPWD} \geq t_{CPWD}$ (Min.), the cycle is read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

10. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a $\overline{OE}$ control write cycle or a read modify write cycle.

11. The test mode is initiated by performing a $\overline{WB}$, $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remain in effect until the exit cycle is generated. In a test mode CA0 is not used and each I/O pin now accesses 2 bit locations.
Since all 4 I/O pins are used, a total of 8 data bits can be written in parallel into the memory array. In a read cycle, if 2 data bits are equal, the I/O pin will indicate a high level.
If the 2 data bits are not equal, the I/O pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

12. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

13. Write-per-bit Feature:

The addition of a data write-mask register in this multibit wide memory device allows the capability of writing only to the needed data bits in a given address location while leaving the other data bits unaffected.

During execution of a write cycle, including Early Write, Delayed Write or Read-Modify-Write, if $\overline{\text{WB}}/\overline{\text{WE}}$ is at a low level (V_{IL}) during the falling edge of $\overline{\text{RAS}}$ the data present on the DQi pins is latched into the Write-mask register. At this time the DQi pins determine which data bits will be inhibited during the write cycle. A low level (V_{IL}) on a DQi pin indicates that the data bit will be masked or inhibited from being written into the cell during the write cycle. A high level (V_{IH}) on a DQi pin indicates that the data bit will be written into the cell during the write cycle. Refer to Table 1 and Figure 1.

Since the write-mask register is latched by the falling edge of $\overline{\text{RAS}}$, it cannot be changed during write cycles. All the write cycles use the same mask data latched at the begining of the $\overline{\text{RAS}}$ cycle.

Tabel 1 Example of Write-per-Bit Operation

Falling edge of $\overline{\text{RAS}}$					Function
$\overline{\text{WB}}/\overline{\text{WE}}$	DQ1	DQ2	DQ3	DQ4	
H	X	X	X	X	Normal Write mode: Write Enable
L	L	H	L	L	Write-per-bit mode: Write Enable for DQ2, DQ4 Write Enable for DQ1, DQ3

X: Don't Care

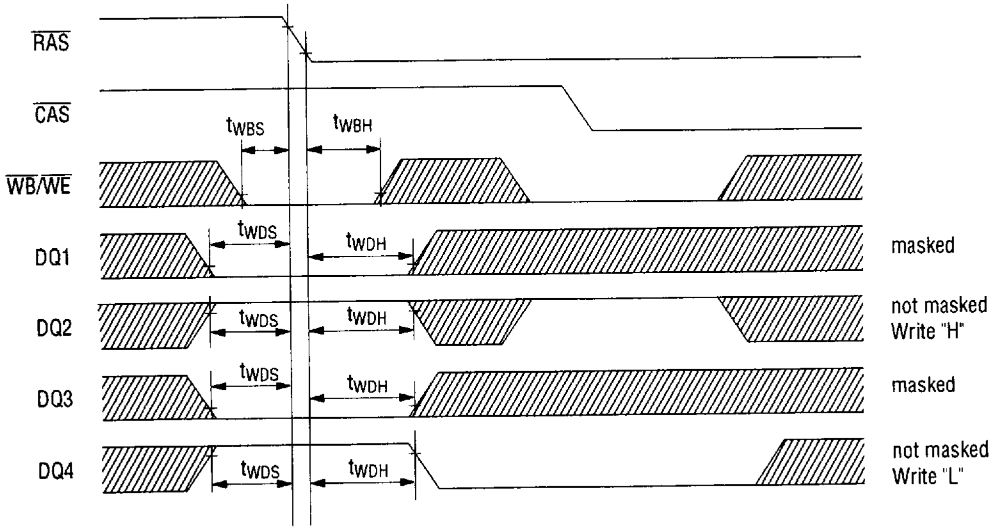
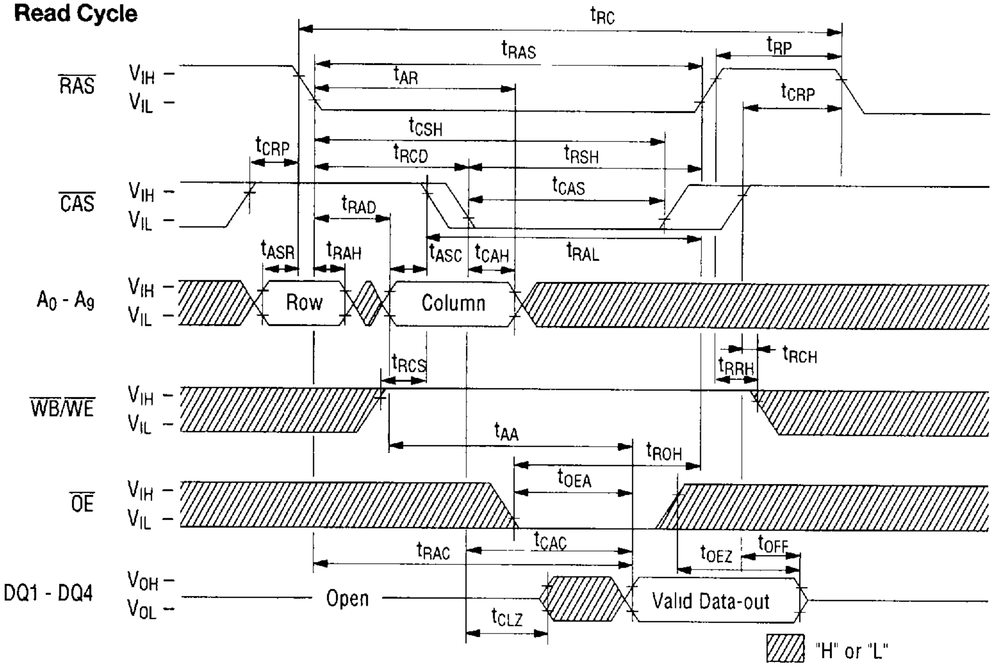


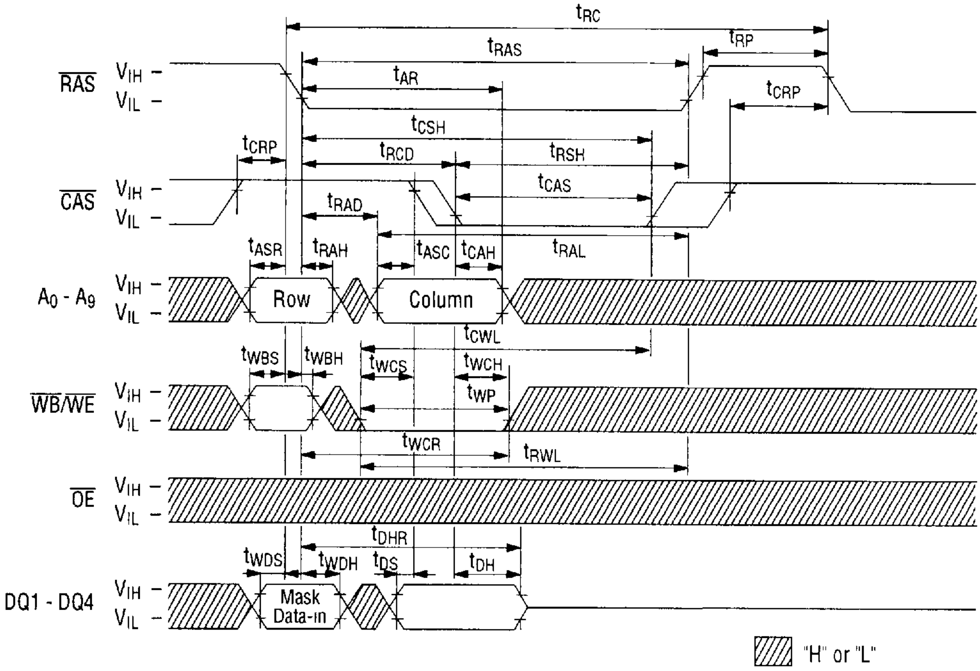
Fig. 1 Example or Write-per-Bit Operation

TIMING WAVEFORM

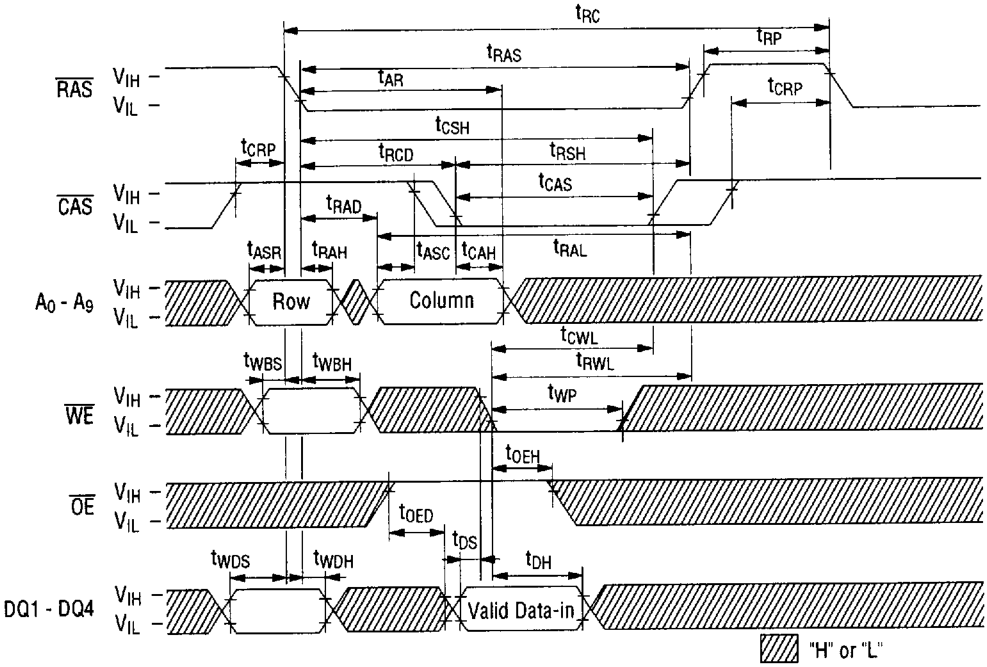
Read Cycle



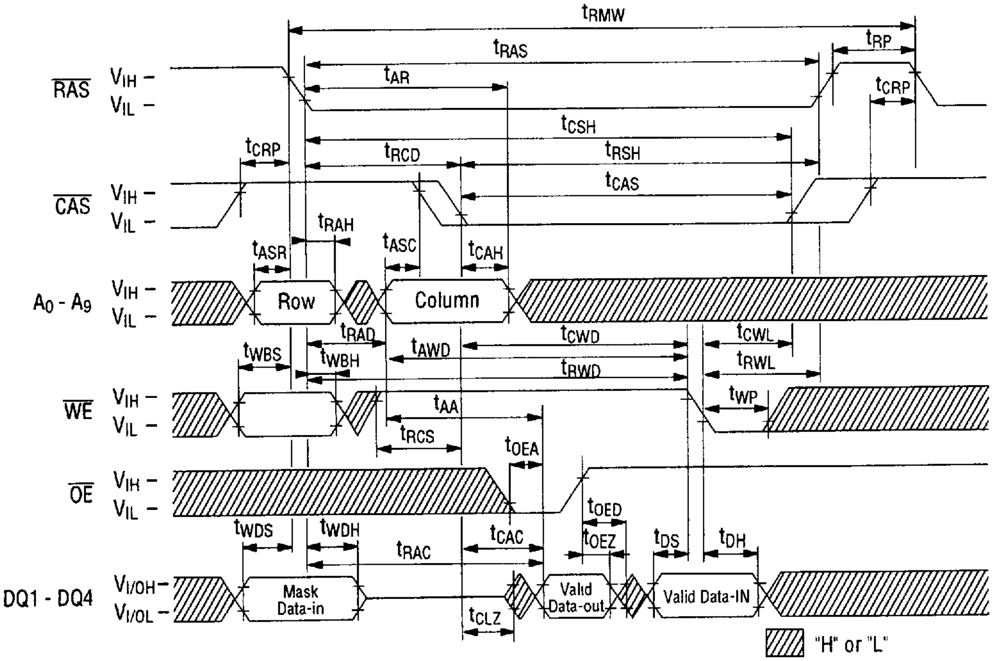
Write Cycle (Early Write)



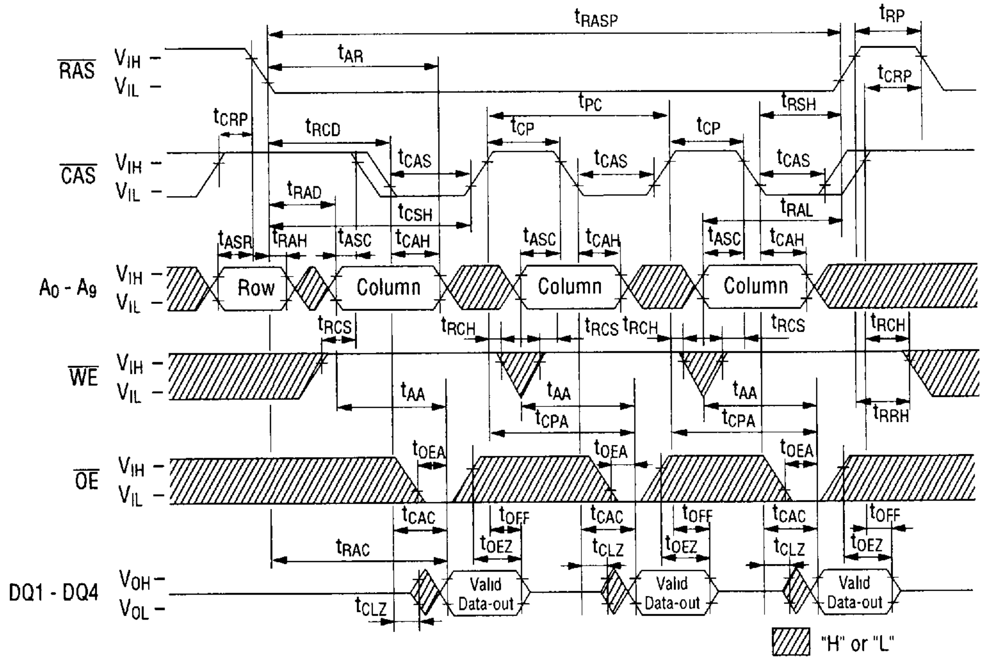
Write Cycle ($\overline{OE}$ Control Write)



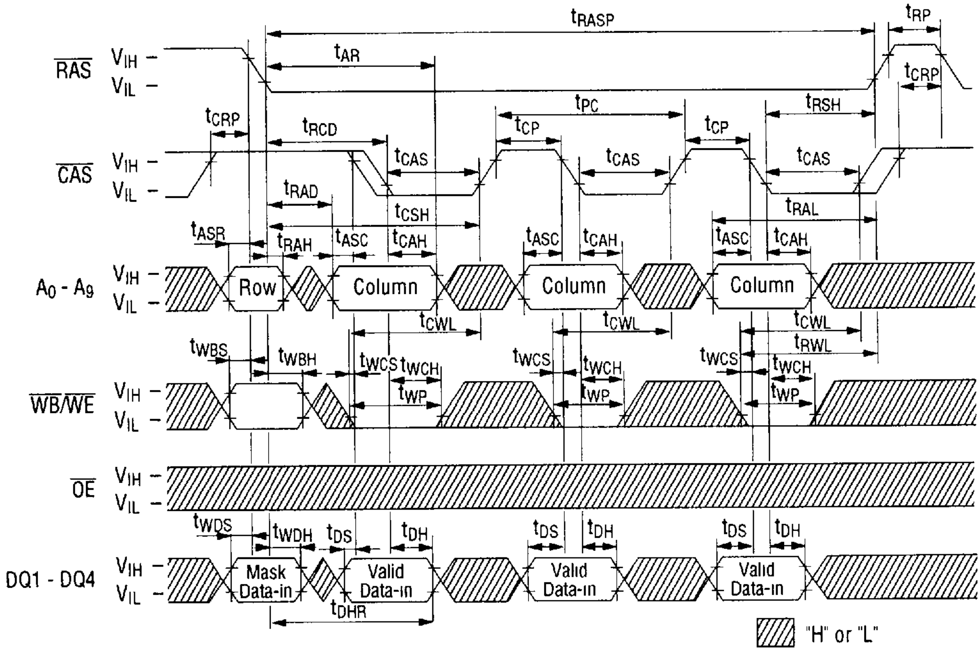
Read Modify Write Cycle



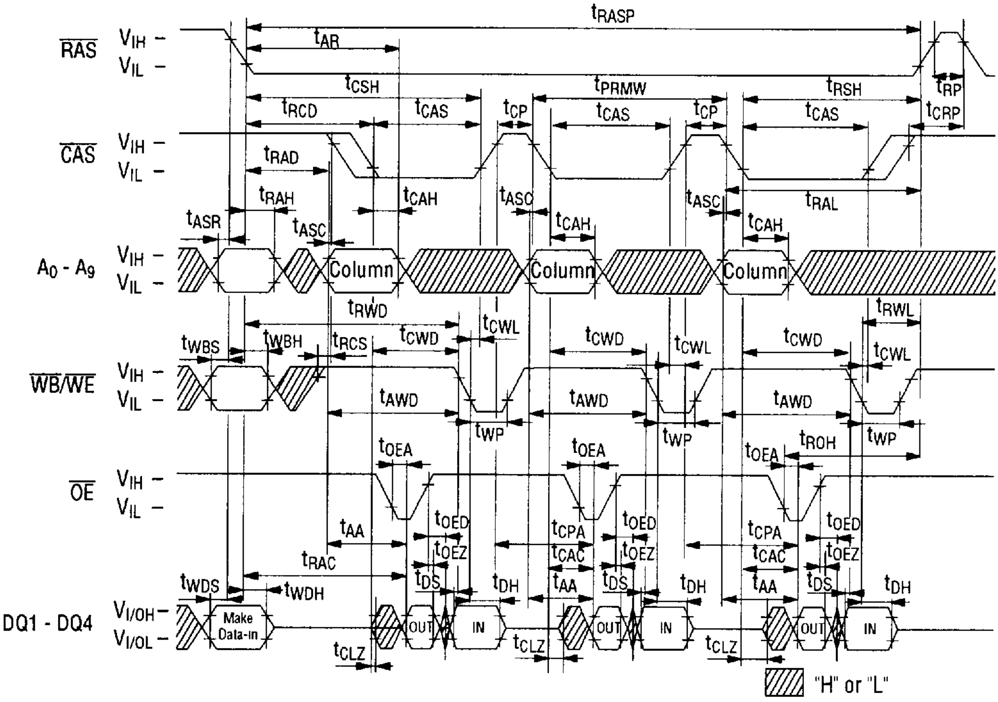
Fast Page Mode Read Cycle



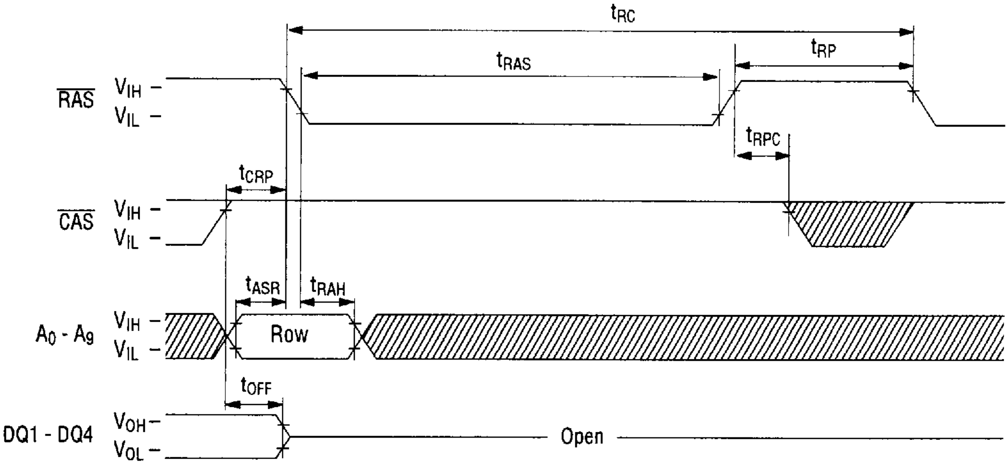
Fast Page Mode Write Cycle (Early Write)



Fast Page Mode Read Modify Write Cycle

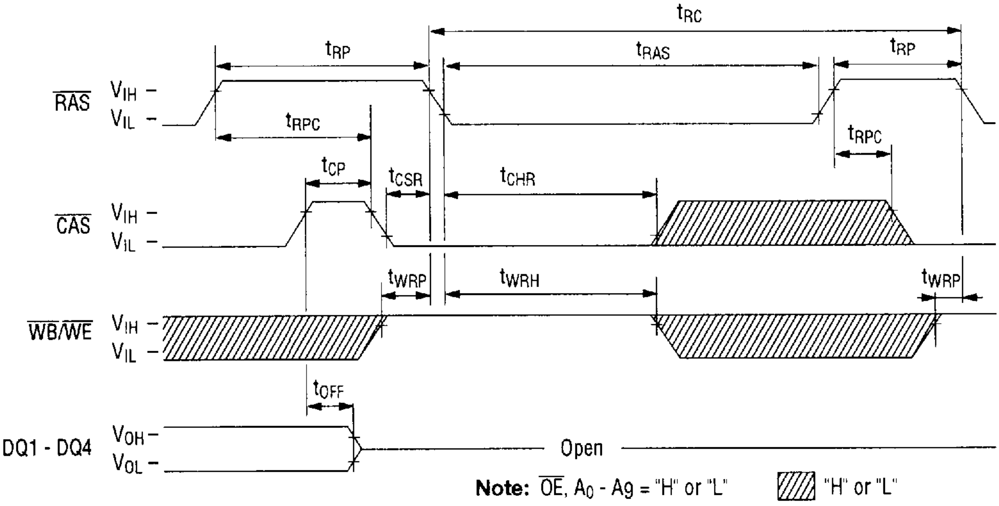


$\overline{\text{RAS}}$-only Refresh Cycle

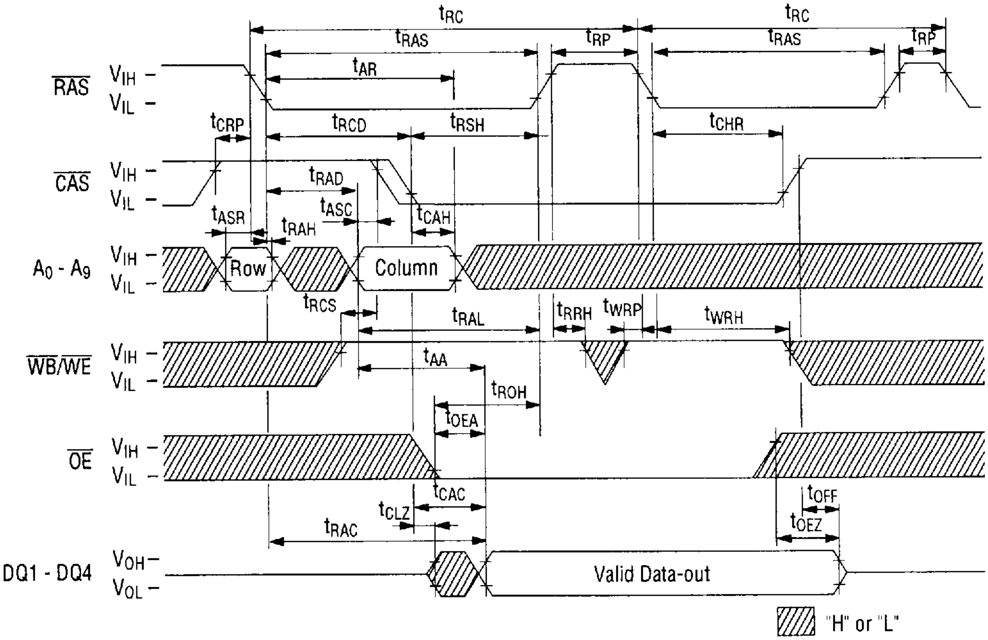


Note: $\overline{\text{WB}}/\overline{\text{WE}}$, $\overline{\text{OE}}$ = "H" or "L" ▨ "H" or "L"

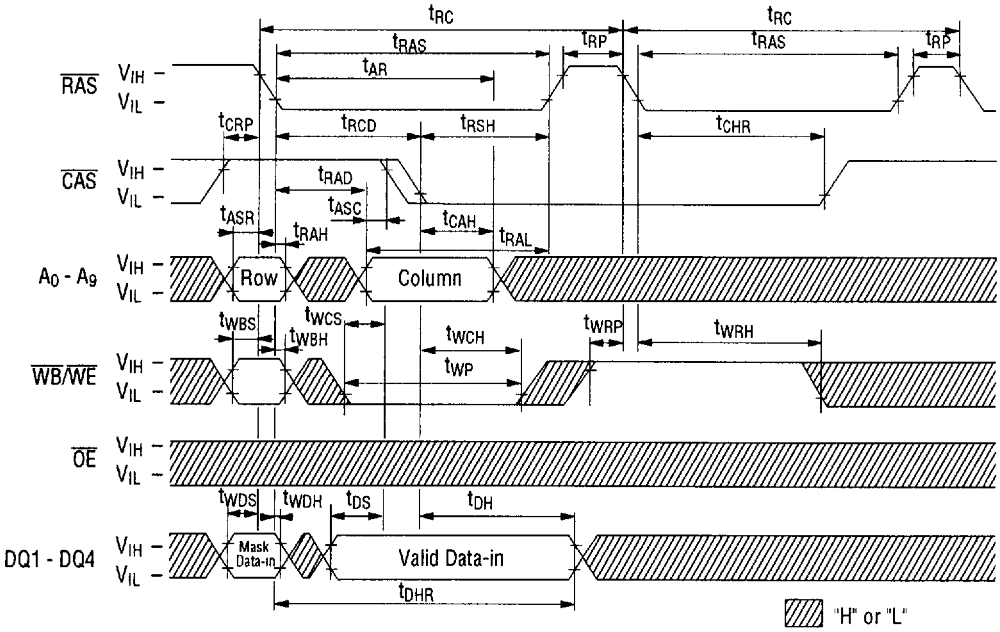
$\overline{CAS}$ Before $\overline{RAS}$ Auto-refresh Cycle



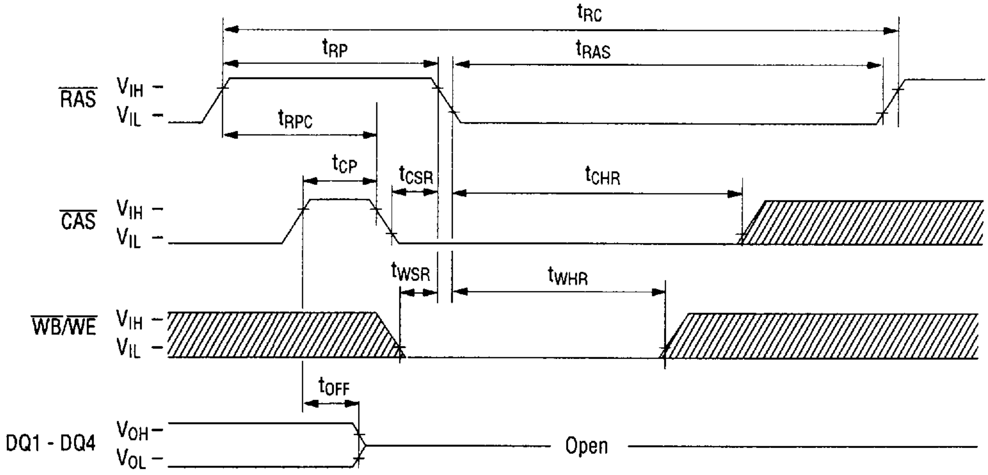
Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



Test Mode Intiate Cycle



Note: $\overline{OE}$, A_0 - A_9 = "H" or "L" ▨ "H" or "L"

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test Cycle