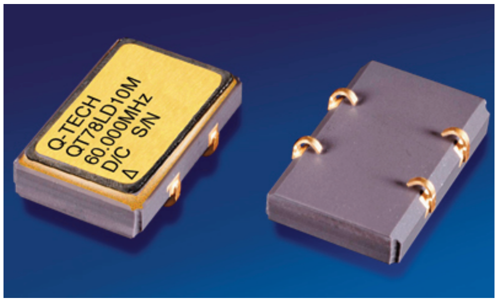
QT78 SERIES

HIGH RELIABILITY MINIATURE CRYSTAL CLOCK OSCILLATORS

1.8 to 5.0Vdc - 15kHz to 150MHz

Description

Q-Tech's surface-mount QT78 Series oscillators consist of an IC 5Vdc, 3.3Vdc, 2.5Vdc, 1.8Vdc clock square wave generator and an AT high-precision quartz crystal built in a rugged surface-mount ceramic J-lead miniature package.



Features

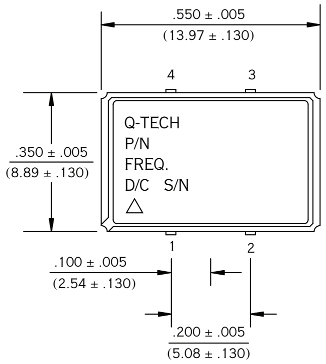
- Made in the USA
- ECCN: EAR99
- DFARS 252-225-7014 Compliant: Electronic Component Exemption
- Available as QPL MIL-PRF-55310/27, /28, and /30
- Broad frequency range from 15kHz to 150MHz
- ACMOS, HCMOS, TTL or LVHCMOS logic
- Tri-State Output Option (D)
- Hermetically sealed ceramic SMD package
- Fundamental and 3rd Overtone designs
- Low phase noise
- Custom designs available
- Q-Tech does not use pure lead or pure tin in its products
- RoHS compliant

Applications

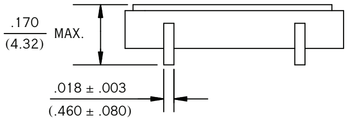
- Designed to meet today's requirements for low voltage applications
- Wide military clock applications
- Smart munitions
- Navigation
- Industrial controls
- Microcontroller driver

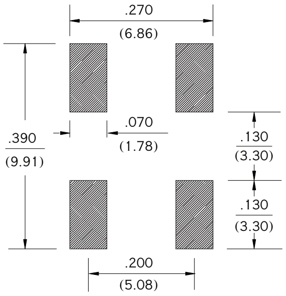
Package Outline and Pin Connections

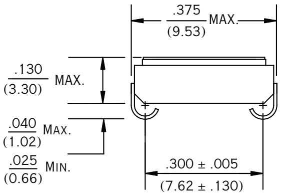
Dimensions are in inches (mm)



Pin No.	Function
1	TRISTATE or NC
2	GND/CASE
3	OUTPUT
4	VDD







Package Information

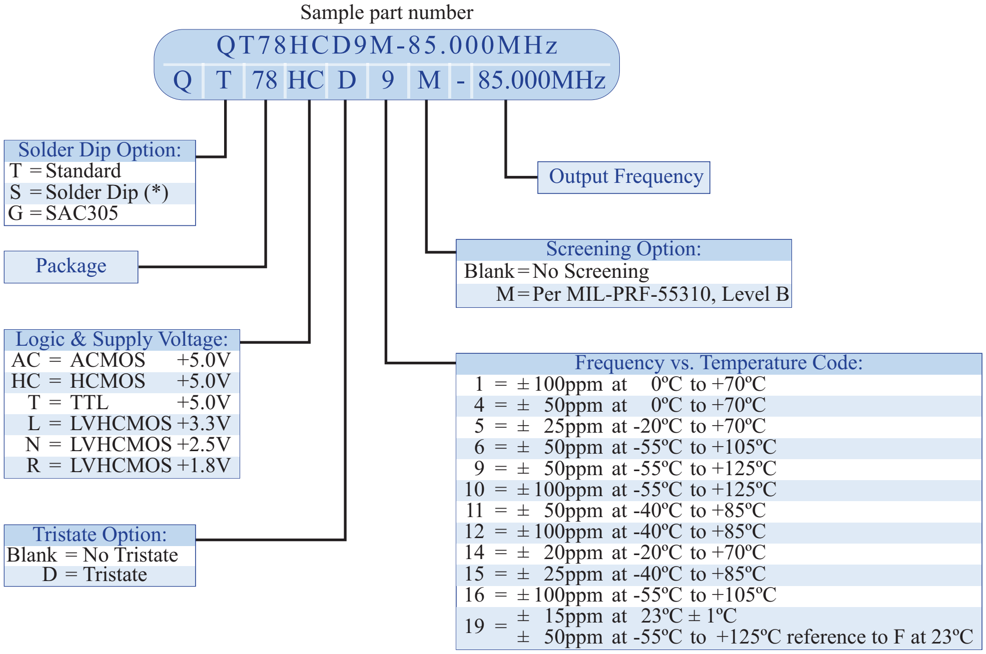
- Package material: 91% AL_2O_3
- Lead material: Kovar
- Lead finish: Gold Plated: 50µ ~ 80µ inches
  Nickel Underplate: 100µ ~ 250µ inches
- Weight: 1.1g typ., 3.0g max.

Electrical Characteristics

Parameters	QT78AC	QT78HC	QT78T	QT78L	QT78N	QT78R
Output frequency range (Fo)	**15kHz — 85.000MHz (*)**			**15kHz — 150.000MHz (*)**	**125.000kHz — 133.000MHz**	**125.000kHz — 100.000MHz**
Supply voltage (Vdd)	5.0Vdc ± 10%			3.3Vdc ± 10%	2.5Vdc ± 10%	1.8Vdc ± 10%
Maximum Applied Voltage (Vdd max.)	-0.5 to +7.0Vdc			-0.5 to +5.0Vdc		
Frequency stability (ΔF/ΔT)	See Option codes					
Operating temperature (Topr)	See Option codes					
Storage temperature (Tsto)	-62ºC to + 125ºC					
Operating supply current (Idd) (No Load)	20 mA max. - 15kHz ~ < 16MHz 25 mA max. - 16MHz ~ < 32MHz 35 mA max. - 32MHz ~ < 60MHz 45 mA max. - 60MHz ~ ≤ 85MHz			3 mA max. - 15kHz ~ < 500kHz 6 mA max. - 500kHz ~ < 16MHz 10 mA max. - 16MHz ~ < 32MHz 20 mA max. - 32MHz ~ < 60MHz 30 mA max. - 60MHz ~ < 100MHz 40 mA max. - 100MHz ~ < 130MHz 50 mA max. - 130MHz ~ ≤150MHz	3 mA max. - 125kHz ~ < 500kHz 6 mA max. - 500kHz ~ < 40MHz 15 mA max. - 40MHz ~ < 60MHz 25 mA max. - 60MHz ~ < 85MHz 35 mA max. - 85MHz ~ ≤ 133MHz	4 mA max. - 125kHz ~ < 40MHz 10 mA max. - 40MHz ~ < 50MHz 20 mA max. - 50MHz ~ < 85MHz 25 mA max. - 85MHz ~ ≤ 100MHz
Symmetry (50% of ouput waveform or 1.4Vdc for TTL)	45/55% max. - 15kHz ~ < 15MHz 40/60% max. - 15 ~ ≤ 85MHz (Tighter symmetry available)			45/55% max. - 15kHz ~ < 15MHz 40/60% max. - 15 ~ ≤ 150MHz (Tighter symmetry available)	45/55% max. - 125kHz ~ < 15MHz 40/60% max. - 15 ~ ≤ 133MHz (Tighter symmetry available)	45/55% max. - 125kHz~ < 15MHz 40/60% max. - 15 ~ ≤ 100MHz (Tighter symmetry available)
Rise and Fall times (with typical load)	200ns max. Fo ≤ 345.6kHz 8ns max. Fo 345.6kHz ~ ≤ 20MHz 5ns max. Fo 20MHz ~ ≤ 50MHz 7ns max. - 20MHz ~ ≤ 50MHz **(50pF Load)** 3ns max. Fo > 50MHz (Measured from 10% to 90% CMOS or from 0.8V to 2.0V TTL)			200ns max. Fo < 345.6kHz 6ns max. Fo 345.6kHz ~ ≤ 20MHz 4ns max. Fo 20MHz ~ ≤ 50MHz 3ns max. Fo > 50MHz 7ns max. - **50pF Load** (Measured from 10% to 90%)		
Output Load	**15pF // 10kohms** 50pF max. or 10TTL for (Fo ≤ 50MHz) 30pF max. or 6TTL for (Fo > 50MHz)	**15pF // 10kohms** (2LSTTL)	**10TTL (Fo < 60MHz)** 6TTL (Fo ≥ 60MHz)	**15pF // 10kohms** (30pF max. for Fo > 50MHz)	**15pF // 10kohms**	
Start-up time (Tstup)	10ms max.				5ms max.	
Output voltage (Voh/Vol)	0.9 x Vdd min.; 0.1 x Vdd max.		2.4V min.; 0.4V max.	0.9 x Vdd min.; 0.1 x Vdd max.		
Output Current (Ioh/Iol)	± 24mA max.	± 16mA max.	-1.6 mA/TTL +40 µA/TTL	± 8mA max.		
Enable/Disable Tristate function Pin 1	VIH ≥ 4.0V Oscillation; VIL ≤ 0.8V High Impedance		VIH ≥ 2.2V Oscillation; VIL ≤ 0.8V High Impedance	VIH ≥ 2.0V Oscillation; VIL ≤ 0.5V High Impedance	VIH ≥ 1.75V Oscillation; VIL ≤ 0.5V High Impedance	VIH ≥ 1.26V Oscillation; VIL ≤ 0.5V High Impedance
Jitter RMS 1σ (at 25ºC)	8ps typ. - < 40MHz 5ps typ. - ≥ 40MHz			15ps typ. - < 40MHz 8ps typ. - ≥ 40MHz		
Aging (at 70ºC)	± 5ppm max. first year / ± 2ppm max. per year thereafter					

(*) Frequency as low as 1kHz without tristate function available. Contact Q-Tech for details.

Ordering Information



Sample part number

QT78HCD9M-85.000MHz

Q | T | 78 | HC | D | 9 | M | - | 85.000MHz

Solder Dip Option:
T = Standard
S = Solder Dip (*)
G = SAC305

Package

Logic & Supply Voltage:

AC	=	ACMOS	+5.0V
HC	=	HCMOS	+5.0V
T	=	TTL	+5.0V
L	=	LVHCMOS	+3.3V
N	=	LVHCMOS	+2.5V
R	=	LVHCMOS	+1.8V

Tristate Option:
Blank = No Tristate
D = Tristate

Output Frequency

Screening Option:
Blank = No Screening
M = Per MIL-PRF-55310, Level B

Frequency vs. Temperature Code:

Code		Stability		Temperature Range
1	=	± 100ppm	at	0ºC to +70ºC
4	=	± 50ppm	at	0ºC to +70ºC
5	=	± 25ppm	at	-20ºC to +70ºC
6	=	± 50ppm	at	-55ºC to +105ºC
9	=	± 50ppm	at	-55ºC to +125ºC
10	=	± 100ppm	at	-55ºC to +125ºC
11	=	± 50ppm	at	-40ºC to +85ºC
12	=	± 100ppm	at	-40ºC to +85ºC
14	=	± 20ppm	at	-20ºC to +70ºC
15	=	± 25ppm	at	-40ºC to +85ºC
16	=	± 100ppm	at	-55ºC to +105ºC
19	=	± 15ppm ± 50ppm	at at	23ºC ± 1ºC -55ºC to +125ºC reference to F at 23ºC

(*) Hot Solder Dip Sn60/Pb40 per MIL-PRF 55310 is optional for an additional cost

Frequency stability vs. temperature codes may not be available in all frequencies.

For Non-Standard requirements,
contact Q-Tech Corporation at Sales@Q-Tech.com

Packaging Options

- Standard packaging in anti-static plastic tube (60 pcs/tube)
- Tape and Reel (1,000 pcs/reel) is available for an additional charge.

Other Options Available For An Additional Charge

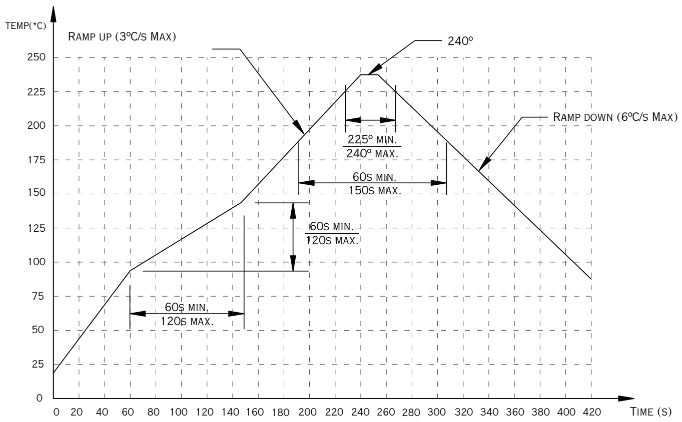
- P. I. N. D. test (MIL-STD 883, Method 2020)

Specifications subject to change without prior notice.

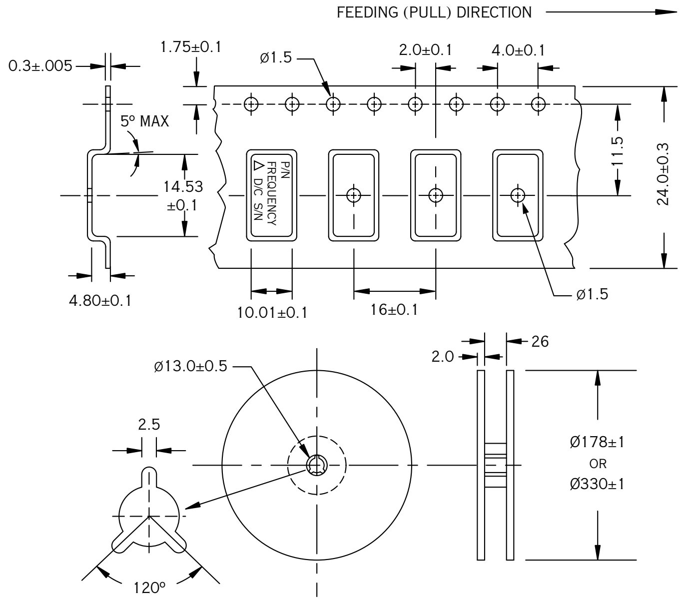
Reflow Profile

The five transition periods for the typical reflow process are:

- Preheat
- Flux activation
- Thermal equalization
- Reflow
- Cool down


TYPICAL REFLOW PROFILE FOR SN-PB ASSEMBLY

Embossed Tape and Reel Information For QT78



Dimensions are in mm. Tape is compliant to EIA-481-A.

Reel size vs. quantity:

Reel size (Diameter in mm)	Qty per reel (pcs)
178	250
330	1,000

Environmental Specifications

Q-Tech Standard Screening/QCI (MIL-PRF55310) is available for all of our QT78 Products. Q-Tech can also customize screening and test procedures to meet your specific requirements. The QT78 product is designed and processed to exceed the following test conditions:

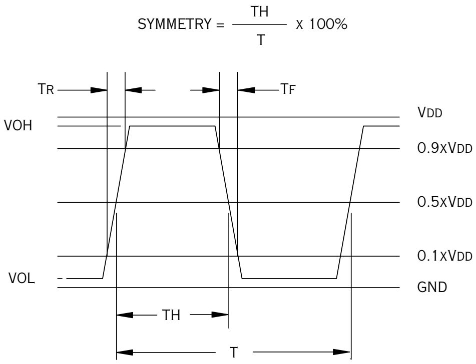
Environmental Test	Test Conditions
Temperature cycling	MIL-STD-883, Method 1010, Cond. B
Constant acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal: Fine and Gross Leak	MIL-STD-883, Method 1014, Cond. A and C
Burn-in	160 hours, 125°C with load
Aging	30 days, 70°C, ±1.5ppm max
Vibration sinusoidal	MIL-STD-202, Method 204, Cond. D
Shock, non operating	MIL-STD-202, Method 213, Cond. I (See Note 1)
Thermal shock, non operating	MIL-STD-202, Method 107, Cond. B
Ambient pressure, non operating	MIL-STD-202, 105, Cond. C, 5 minutes dwell time minimum
Resistance to solder heat	MIL-STD-202, Method 210, Cond. B
Moisture resistance	MIL-STD-202, Method 106
Terminal strength	MIL-STD-202, Method 211, Cond. C
Resistance to solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208
ESD Classification	MIL-STD-883, Method 3015, Class 1 HBM 0 to 1,999V
Moisture Sensitivity Level	J-STD-020, MSL=1

Note 1: Additional shock results successfully passed on 16MHz, 40MHz, and 80MHz

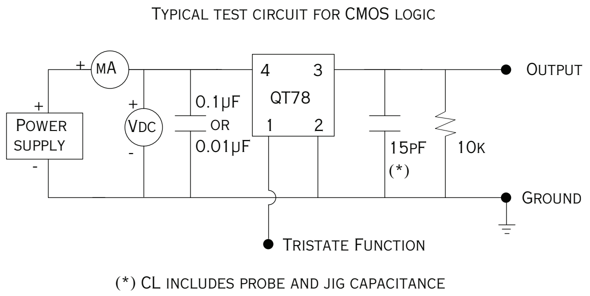
- Shock 850g peak, half-sine, 1 ms duration (MIL-STD-202, Method 213, Cond. D modified)
- Shock 1,500g peak, half-sine, 0.5ms duration (MIL-STD-883, Method 2002, Cond. B)

Please contact Q-Tech for higher shock requirements

Output Waveform (Typical)

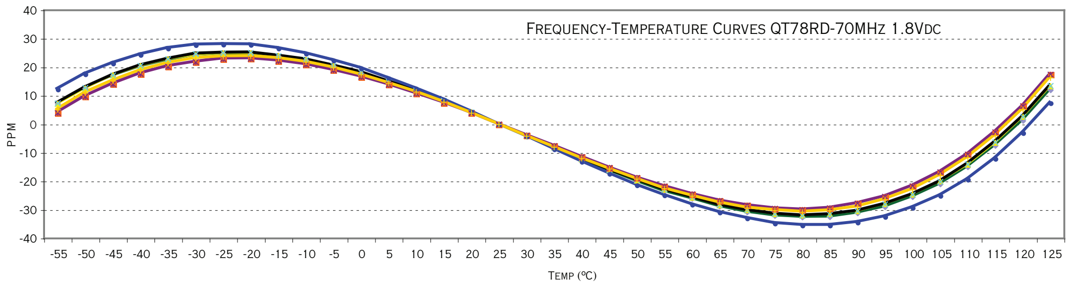


Test Circuit



The Tristate function on pin 1 has a built-in pull-up resistor typical 50kΩ, so it can be left floating or tied to Vdd without deteriorating the electrical performance.

Frequency vs. Temperature Curve



Thermal Characteristics

The heat transfer model in a hybrid package is described in figure 1.

Heat spreading occurs when heat flows into a material layer of increased cross-sectional area. It is adequate to assume that spreading occurs at a 45° angle.

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and hybrid case.

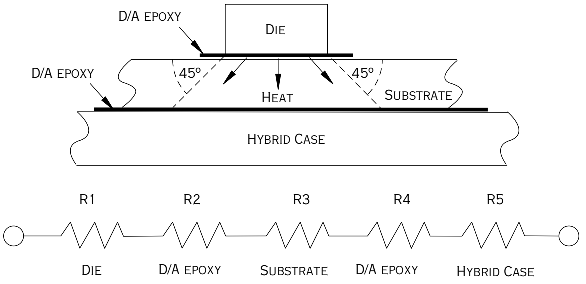
$$RT = R1 + R2 + R3 + R4 + R5$$

The total thermal resistance RT (see figure 2) between the heat source (die) to the hybrid case is the Theta Junction to Case (Theta JC) in°C/W.

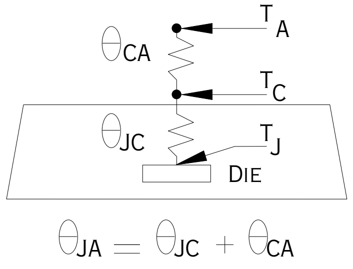
- Theta junction to case (Theta JC) for this product is 30°C/W.
- Theta case to ambient (Theta CA) for this part is 100°C/W.
- Theta Junction to ambient (Theta JA) is 130°C/W.

Maximum power dissipation PD for this package at 25°C is:

- PD(max) = (TJ (max) – TA)/Theta JA
- With TJ = 175°C (Maximum junction temperature of die)
- PD(max) = (175 – 25)/130 = 1.15W

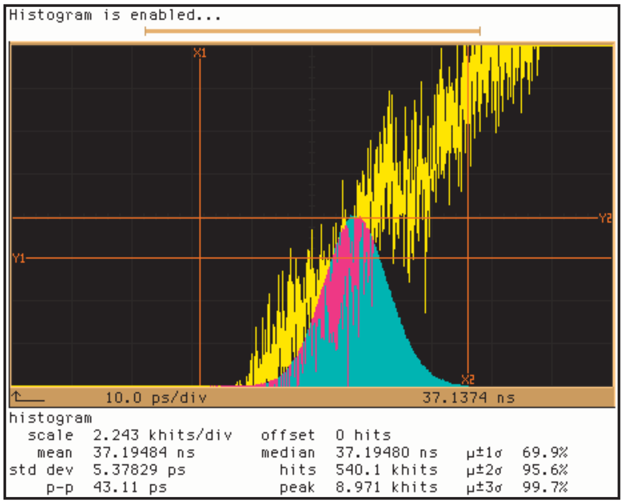


(Figure 1)



Period Jitter

As data rates increase, effects of jitter become critical with its budgets tighter. Jitter is the deviation of a timing event of a signal from its ideal position. Jitter is complex and is composed of both random and deterministic jitter components. Random jitter (RJ) is theoretically unbounded and Gaussian in distribution. Deterministic jitter (DJ) is bounded and does not follow any predictable distribution. DJ is also referred to as systematic jitter. A technique to measure period jitter (RMS) one standard deviation (1σ) and peak-to-peak jitter in time domain is to use a high sampling rate (>8G samples/s) digitizing oscilloscope. Figure shows an example of peak-to-peak jitter and RMS jitter (1σ) of a QT78AC-24MHz, at 5.0Vdc.



```
Histogram is enabled...
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```
histogram
  scale  2.243 khits/div   offset  0 hits
   mean  37.19484 ns       median  37.19480 ns   μ±1σ  69.9%
std dev  5.37829 ps          hits  540.1 khits   μ±2σ  95.6%
    p-p  43.11 ps            peak  8.971 khits   μ±3σ  99.7%
```

RMS jitter (1σ): 5.37ps Peak-to-peak jitter: 43ps

Phase Noise and Phase Jitter Integration

Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at an offset frequency from the carrier, e.g. 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, etc. Phase noise measurement is made with an Agilent E5052A Signal Source Analyzer (SSA) with built-in outstanding low-noise DC power supply source. The DC source is floated from the ground and isolated from external noise to ensure accuracy and repeatability.

In order to determine the total noise power over a certain frequency range (bandwidth), the time domain must be analyzed in the frequency domain, and then reconstructed in the time domain into an rms value with the unwanted frequencies excluded. This may be done by converting L(f) back to Sφ(f) over the bandwidth of interest, integrating and performing some calculations.

Symbol	Definition
$\int\mathcal{L}(f)$	Integrated single side band phase noise (dBc)
$S\varphi\ (f)=(180/\Pi)x\sqrt{2\int\mathcal{L}(f)df}$	Spectral density of phase modulation, also known as RMS phase error (in degrees)
RMS jitter = $S\varphi\ (f)/(fosc.360°)$	Jitter(in seconds) due to phase noise. Note Sφ (f) in degrees.

The value of RMS jitter over the bandwidth of interest, e.g. 10kHz to 20MHz, 10Hz to 20MHz, represents 1 standard deviation of phase jitter contributed by the noise in that defined bandwidth.

DCO	REV	REVISION SUMMARY	PAGE	DATE
6389	-	Rename document from QT78 (Revision H, January 2011) (ECO #10085) to QPDS-0124	All	1/31/17
		Add frequency vs. temperature code 19 and 16	3	
		Ordering information reformatted into one graphic (previously 4 separate graphics)	3	
		Add SAC305 solder dip option	3	
8029	A	Revise 'Description' and 'Features'	1	3/27/18
		Revise Enable/Disable Voltages for clarification/accuracy	2	
		Change Output Current for HCMOS options	2	
		Revise Rise and Fall time Limits	2	
		Revise Start-up Times	2	