

FEATURES

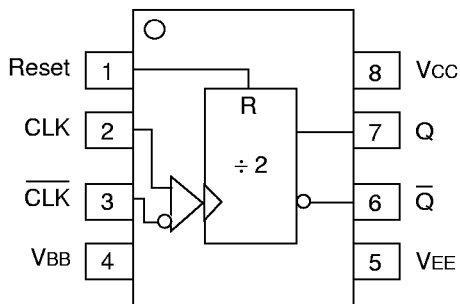
- 3.3V and 5V power supply options
- 510ps propagation delay
- 3.0GHz toggle frequency
- High bandwidth output transistions
- Internal 75KΩ input pull-down resistors
- ESD protection of 2000V
- Available in 8-pin SOIC package

DESCRIPTION

The SY10/100EL32V are integrated ÷2 dividers. The differential clock inputs and the VBB allow a differential, single-ended or AC-coupled interface to the device. If used, the VBB output should be bypassed to ground with a 0.01µF capacitor. Also note that the VBB is designed to be used as an input bias on the EL32V only; the VBB output has limited current sink and source capability.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-on, the internal flip-flop will attain a random state; the reset allows for the synchronization of multiple EL32Vs in a system.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
CLK	Clock Inputs
Reset	Asynchronous Reset
VBB	Reference Voltage Output
Q	Data Outputs

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{EE} = V_{EE} (\text{Min.})$ to $V_{EE} (\text{Max.})$; $V_{CC} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
IEE	Power Supply Current	10EL	—	25	30	—	25	30	—	25	30	—	25	30	mA
		100EL	—	25	30	—	25	30	—	25	30	—	29	35	
VBB	Output Reference Voltage	10EL	-1.43	—	-1.30	-1.38	—	-1.27	-1.35	—	-1.25	-1.31	—	-1.19	V
		100EL	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	μA	

NOTE:

1. Parametric values specified at: 10/100EL32V Series: -3.0V to -5.5V.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{EE} = V_{EE} (\text{Min.})$ to $V_{EE} (\text{Max.})$; $V_{CC} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f _{MAX}	Maximum Toggle Frequency	2.2	3.0	—	2.6	3.0	—	2.6	3.0	—	2.6	3.0	—	GHz
t _{PLH}	Prop Delay to Output D	360	500	640	410	500	590	420	510	600	450	540	630	ps
t _{PHL}	Reset to Q	390	540	690	440	540	640	440	540	640	450	550	650	
V _{PP}	Minimum Input Swing ⁽²⁾	150	—	—	150	—	—	150	—	—	150	—	—	mV
V _{CMR}	Common Mode Range ⁽³⁾	-1.3	—	-0.4	-1.4	—	-0.4	-1.4	—	-0.4	-1.4	—	-0.4	V
t _r	Output Rise/Fall Times Q (20% to 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps
t _f														

NOTES:

1. Parametric values specified at: 10/100EL32V Series: -3.0V to -5.5V.
2. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 .
3. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = -3.3V. Note for PECL operation, the V_{CMR} (min) will be fixed at $3.3V - |V_{CMR} (\text{min})|$.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	V _{EE} Range (V)
SY10EL32VZC	Z8-1	Commercial	-3.0 to -5.5
SY10EL32VZCTR	Z8-1	Commercial	-3.0 to -5.5
SY100EL32VZC	Z8-1	Commercial	-3.0 to -5.5
SY100EL32VZCTR	Z8-1	Commercial	-3.0 to -5.5

8 LEAD PLASTIC SOIC (Z8-1)

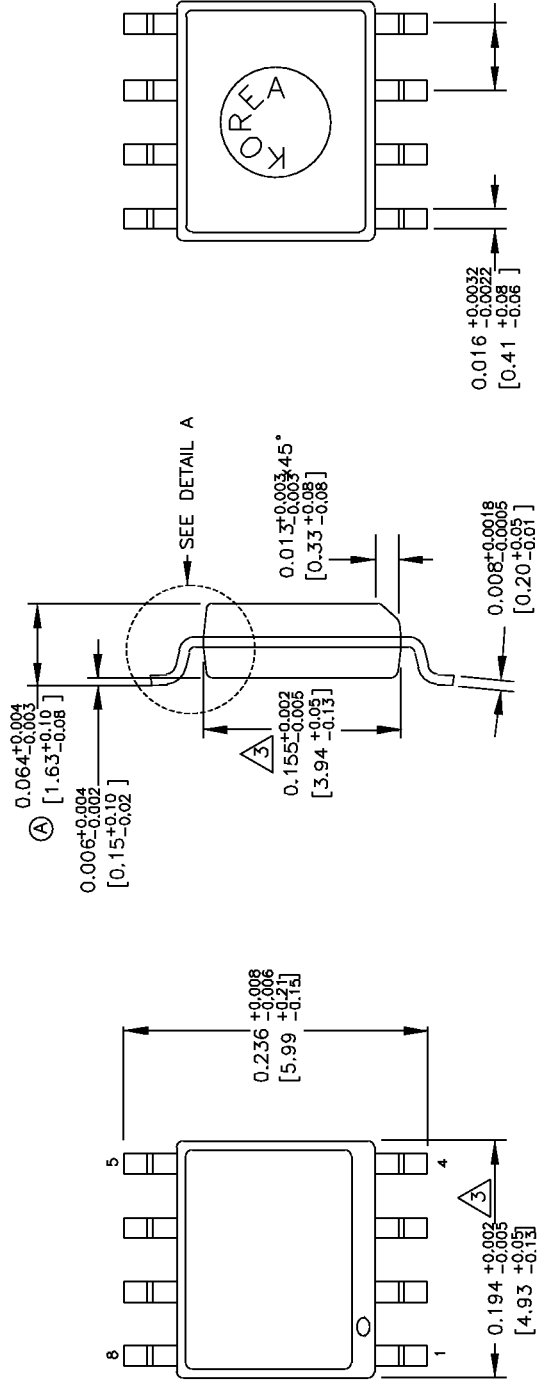
FILE/REV #: PD0032A03 PD/0032/ASCORP PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
00	NEW OUTLINE DRAWING.	01/20/94
01	CONVERT TO AUTOCAD, REFERENCE AMKOR DWG. NO. 00019 REV.05. MAKE (A) SAME AS JEDEC.	12/14/95
02	ADDED LEAD WIDTH AND PITCH DIMENSIONS, CORRECTED TYPOS.	03/12/97
03	CONVERT DWG TO REL.13 AND ONE PAGE DOCUMENT.	02/20/98

TOP VIEW

END VIEW

BOTTOM VIEW



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
 2. CONTROLLING DIMENSION: INCHES.
- △ DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.



APPROVALS	DATE	APPROVALS	DATE	SIZE	8 LEAD PLASTIC SOIC (.150"WIDE)
ORIGINATOR:	02/23/98	QUALITY:		A	PACKAGE OUTLINE
TERMIN G. URRUTIA		MARSHALL WILDER			
CHK'D:		DOCUMENT CONTROL			
WON CHANG		BRIAN SANFILIPPO			
RELEASE DATE:					

3250 SCOTT BOULEVARD
SANTA CLARA, CA, 95054
TEL: 408-980-9191
FAX: 408-567-7878

SCALE N/A
REVISION 03

THESE SPECIFICATIONS ARE THE PROPERTY OF SYNERGY SEMICONDUCTOR, ARE ISSUED IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, OR USED AS THE BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS WITHOUT WRITTEN PERMISSION.

