FEATURES

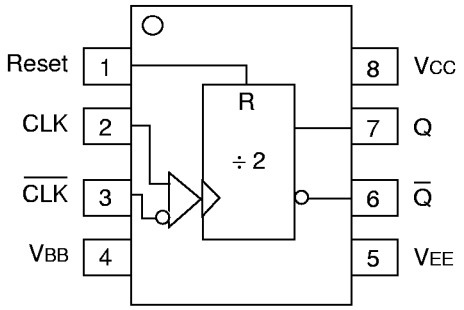
- 3.3V and 5V power supply options
- 510ps propagation delay
- 3.0GHz toggle frequency
- High bandwidth output transistions
- Internal 75KΩ input pull-down resistors
- ESD protection of 2000V
- Available in 8-pin SOIC package

DESCRIPTION

The SY10/100EL32V are integrated ÷2 dividers. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC-coupled interface to the device. If used, the V_{BB} output should be bypassed to ground with a 0.01µF capacitor. Also note that the V_{BB} is designed to be used as an input bias on the EL32V only; the V_{BB} output has limited current sink and source capability.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-on, the internal flip-flop will attain a random state; the reset allows for the synchronization of multiple EL32Vs in a system.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
CLK	Clock Inputs
Reset	Asynchronous Reset
V_{BB}	Reference Voltage Output
Q	Data Outputs

Rev.: C Amendment: /0
Issue Date: August, 1998

DC ELECTRICAL CHARACTERISTICS[1]

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter		T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	10EL	—	25	30	—	25	30	—	25	30	—	25	30	mA
		100EL	—	25	30	—	25	30	—	25	30	—	29	35	
V_{BB}	Output Reference Voltage	10EL	–1.43	—	–1.30	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19	V
		100EL	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	
I_{IH}	Input HIGH Current		—	—	150	—	—	150	—	—	150	—	—	150	µA

NOTE:

1. Parametric values specified at: 10/100EL32V Series: -3.0V to -5.5V.

AC ELECTRICAL CHARACTERISTICS[1]

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Toggle Frequency	2.2	3.0	—	2.6	3.0	—	2.6	3.0	—	2.6	3.0	—	GHz
t_{PLH} t_{PHL}	Prop Delay to Output D Reset to Q	360 390	500 540	640 690	410 440	500 540	590 640	420 440	510 540	600 640	450 450	540 550	630 650	ps
V_{PP}	Minimum Input Swing[2]	150	—	—	150	—	—	150	—	—	150	—	—	mV
V_{CMR}	Common Mode Range[3]	–1.3	—	–0.4	–1.4	—	–0.4	–1.4	—	–0.4	–1.4	—	–0.4	V
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

NOTES:

1. Parametric values specified at: 10/100EL32V Series: -3.0V to -5.5V.
2. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.
3. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR} (min) will be fixed at 3.3V – |V_{CMR} (min)|.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	V_{EE} Range (V)
SY10EL32VZC	Z8-1	Commercial	-3.0 to -5.5
SY10EL32VZCTR	Z8-1	Commercial	-3.0 to -5.5
SY100EL32VZC	Z8-1	Commercial	-3.0 to -5.5
SY100EL32VZCTR	Z8-1	Commercial	-3.0 to -5.5

8 LEAD PLASTIC SOIC (Z8-1)