SH-2: SH7040 Product Brief

SH7000 Series 32-Bit RISC Embedded Controller

HITACHI

PMH12TO004D1
Preliminary Rev 0.1
January 16, 1997

Features

- 28 MHz at 5 V, 16 MHz at 3.3 V
- SuperH™ RISC engine (CPU)
  - — Single-cycle execution of basic instructions
  - — 16-bit fixed instruction set
  - — Five-stage pipeline
  - — Load/store register architecture
  - — Sixteen 32-bit general registers, three 32-bit control registers, four 32-bit system registers
- ROM/RAM: (See table 1)
- Multiply and accumulate unit (MAC)
  - — 32 bit × 32 bit, 64 bit → 64 bit
  - — MAC executed in 2 to 4 cycles
- Bus state controller (BSC)
  - — DRAM/PSRAM refresh
  - — 16/8-bit (QFP-112) or 32/16/8-bit QFP-144) external data paths
  - — Programmable wait states
- Cache memory
  - — 1-kbyte instruction cache
  - — 2-kbyte RAM as address/data array when cache is enabled
- Four-channel direct memory access controller (DMAC)
  - — Data transfers between on-chip or external memory, I/O, and peripheral modules
  - — Selectable priorities and modes
  - — Cycle steal transfers, single/dual address transfer modes, direct/indirect transfer modes
- Data transfer controller (DTC)
- Interrupt controller (INTC)
  - — 43 internal and 17 external sources (NMI, IRL0–IRL3 encoded)
- 16-bit × 5 channel multifunction timer/pulse unit (MTU)
- 16-bit × 2 channel compare match timer (CMT)
- Watchdog timer (WDT)
- Clock pulse generation (CPG) with PLL circuit

- User break controller (UBC) supporting debugging functions
- Two-channel serial communications interface (SCI)
- I/O ports
  - — 74 I/O, plus 8 input (QFP-112)
  - — 98 I/O, plus 8 input (QFP-144)
- 10-bit × 8 channel A/D converter
- –20°C to +75°C operating temperature range
- 112-pin QFP (SH7040/42), 144-pin QFP (SH7041/43)
- 0.6-micron high-speed CMOS technology
- Complete development systems support

Related Manuals

- *SH Series Overview*
- *SH7040 Hardware Manual*
- *SH7000/7600 Programming Manual*

See also http://www.halsp.hitachi.com.

Block Diagram

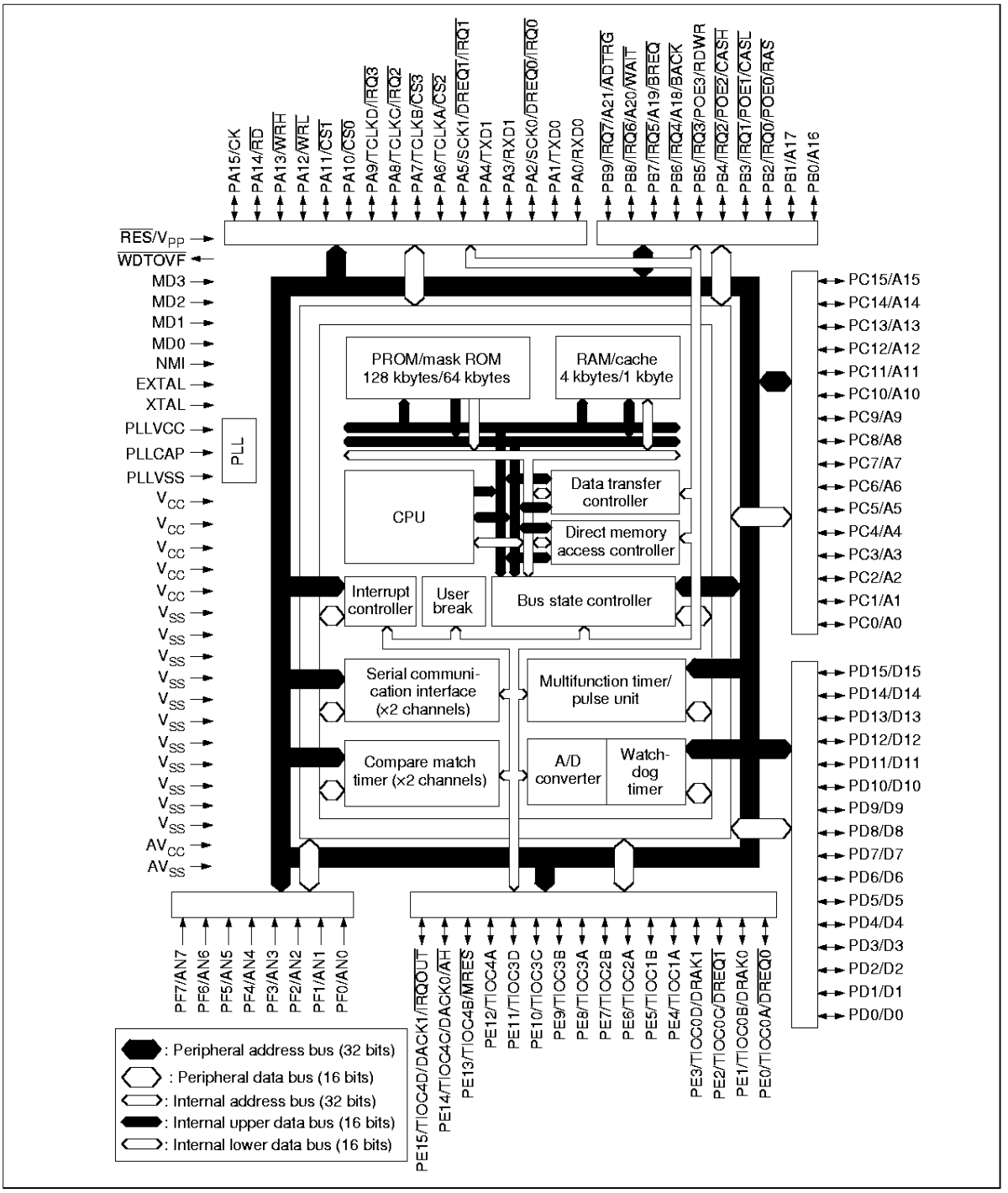

Figure 1 SH7040/SH7042

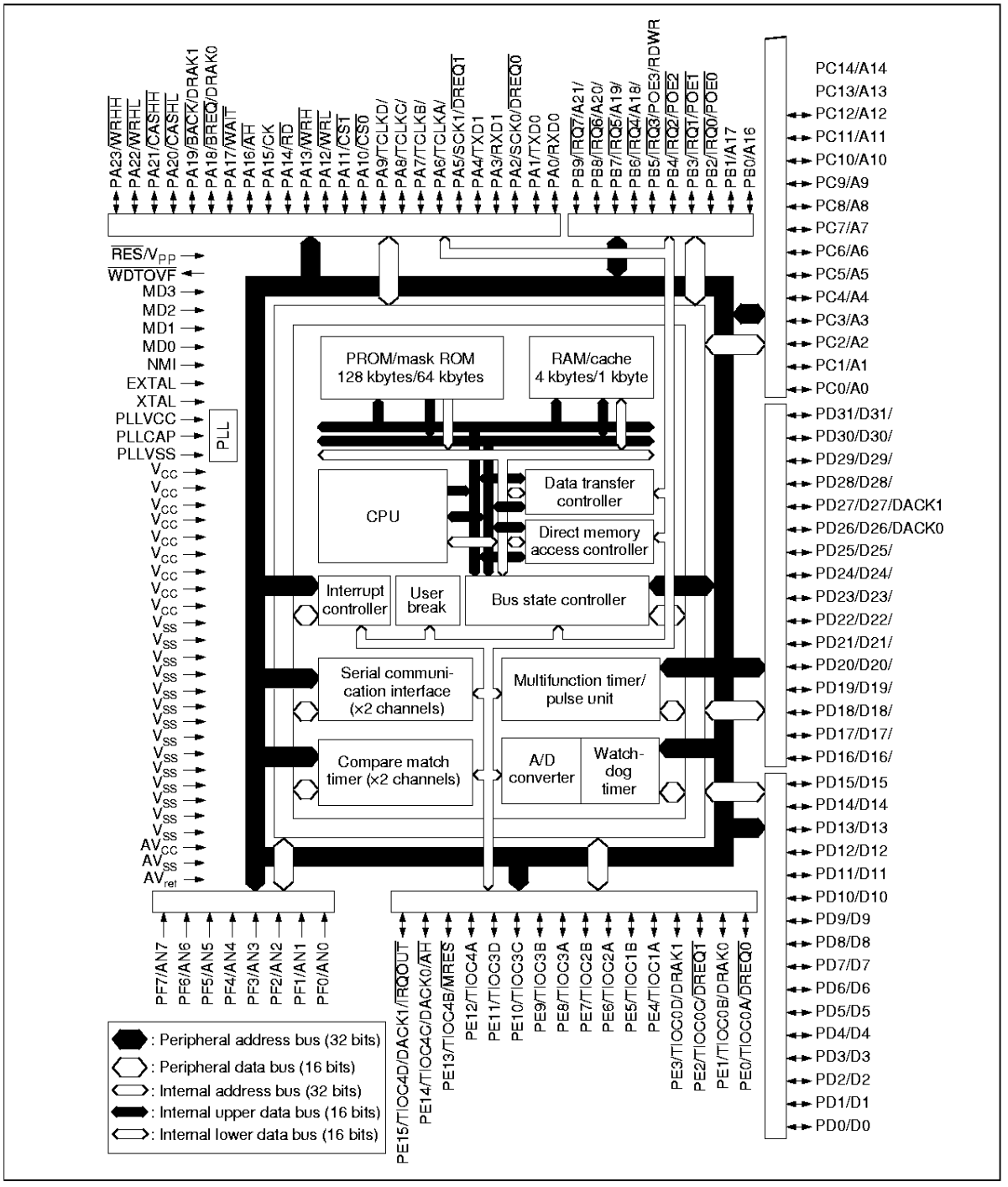

Figure 2 SH7041/SH7043 Block Diagram

Table 1 SH7040 Members

	External Datapath (bits)	ROM (kbyte)	RAM (kbyte)	ZTAT™ (kbyte)	Package (QFP)
SH7040*	16/8	64	4	—	112
SH7041*	32/16/8	64	4	—	144
SH7042	16/8	128	4	128	112
SH7043	32/16/8	128	4	128	144

Note: Available mid-1997. Use the SH7042/43.

Table 2 SH7040 Enhancements Compared to the SH7034

Feature	SH7034	SH704x
CPU (instruction set)	SH7000 CPU (56 instructions)	SH7600 CPU (62 instructions)*
Operation frequency	20 MHz	28 MHz*
Multiply and accumulate unit	16 bit	32 bit*
Address bus	22 bit	22 bit
Data bus	16 bit	16 bit and 32 bit*
Memory (ROM/RAM)	64 kbyte/4 kbyte	128 kbyte/4 kbyte*
INTC	16 level	16 level
DMAC	4 ch	4 ch (compatible with SH7000)
SCI	2 ch	2 ch
16-bit timer	5 ch	7 ch*
10-bit A/D	8 ch	8 ch (sample and hold 2 ch)*
WDT	Yes	Yes
UBC	1 ch	1 ch
CPG	Duty adjustment circuit (× 1)	PLL (× 1, 2, 4)*
Single chip mode	No	Yes*
PKG	QFP-112	QFP-112 (data bus 16 bit), QFP-144 (data bus 32 bit)*

Note: Improvements.

Instruction Set By Classification (Total: 61 Types)

Table 3 Data Transfer (5 Types)

Operation Code	Function
MOV	Data transfer, immediate data transfer, peripheral module and structural data transfers
MOVA	Effective address transfer
MOVT	T-bit transfer
SWAP	Swap of upper and lower bytes
XTRCT	Extraction of middle of connected registers

Table 4 Arithmetic Operations (20 Types)

Operation Code	Function
ADD	Binary addition
ADDC	Binary addition with carry
ADDV	Binary addition with overflow check
CMP/cond.	Comparison
DIV1	Division
DIV0S	Initialization of signed division
DIV0U	Initialization of unsigned division
DMULS	Signed double-length multiplication
DMULU	Unsigned double-length multiplication
DT	Decrement and test
EXTS	Sign extension
EXTU	Zero extension
MAC	Multiply/accumulate, double-length multiply/accumulate operation
MULS	Signed multiplication (16× 16 bits)
MULU	Unsigned multiplication (16× 16 bits)
NEG	Negation
NEGC	Negation with borrow
SUB	Binary subtraction
SUBC	Binary subtraction with borrow
SUBV	Binary subtraction with underflow check

Table 5 Logic Operations (6 Types)

Operation Code	Function
AND	Logic AND
NOT	Bit inversion
OR	Logical OR
TAS	Memory test and bit set
TST	Logical AND and T bit set
XOR	Exclusive OR

Table 6 Shift Instructions (10 Types)

Operation Code	Function
ROTL	One-bit left rotation
ROTR	One-bit right rotation
ROTCL	One-bit left rotation with T bit
ROTCR	One-bit right rotation with T bit
SHAL	One-bit arithmetic left shift
SHAR	One-bit arithmetic right shift
SHLL	One-bit logical left shift
SHLLn	n-bit logical left shift
SHLR	One-bit logical right shift
SHLRn	n-bit logical right shift

Table 7 Branch Instructions (9 Types)

Operation Code	Function
BF	Conditional branch (T = 0)
BT	Conditional branch (T = 1)
BRA	Unconditional branch
BRAF	Unconditional branch
BSR	Branch to subroutine procedure
BSRF	Branch to subroutine procedure
JMP	Unconditional branch
JSR	Branch to subroutine procedure
RTS	Return from subroutine procedure

Table 8 System Control (11 Types)

Operation Code	Function
CLRT	T bit clear
CLRMAC	MAC register clear
LDC	Load to control register
LDS	Load to system register
NOP	No operation
RTE	Return from exception processing
SETT	T bit set
SLEEP	Shift into power-down mode
STC	Storing control register data
STS	Storing system register data
TRAPA	Trap exception processing

DC Characteristics

Table 9 Current Consumption (Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, AV_{CC} = V_{CC} ± 10%, AVref = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C)

Mode	Symbol	Min	Type	Max	Unit	Remarks
Normal operation	I_{CC}	—	80	130	mA	f = 16.7 MHz
Normal operation	I_{CC}	—	160	230	mA	f = 28 MHz
In sleep mode	I_{CC}	—	70	110	mA	f = 16.7 MHz
In sleep mode	I_{CC}	—	140	200	mA	f = 28 MHz
In standby mode	I_{CC}	—	0.01	5	µA	Ta ≤ 50°C
In standby mode	I_{CC}	—	—	20	µA	Ta > 50°C

AC Characteristics

Table 10 Clock Timing (Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, AV_{CC} = V_{CC} ± 10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figures
Operating frequency	f_{OP}	4	28	MHz	3
Clock cycle time	t_{cyc}	35	250	ns	3
Clock low-level pulse width	t_{CL}	10	—	ns	3
Clock high-level pulse width	t_{CH}	10	—	ns	3
Clock rise time	t_{CR}	—	5	ns	3
Clock fall time	t_{CF}	—	5	ns	3
EXTAL clock input frequency	f_{EX}	4	10	MHz	4
EXTAL clock input cycle time	t_{EXcyc}	100	250	ns	4
EXTAL clock low-level input pulse width	t_{EXL}	40	—	ns	4
EXTAL clock high-level input pulse width	t_{EXH}	40	—	ns	4
EXTAL clock input rise time	t_{EXR}	—	5	ns	4
EXTAL clock input fall time	t_{EXF}	—	5	ns	4
Reset oscillation settling time	t_{OSC1}	10	—	ms	5
Standby return clock settling time	t_{OSC2}	10	—	ms	5

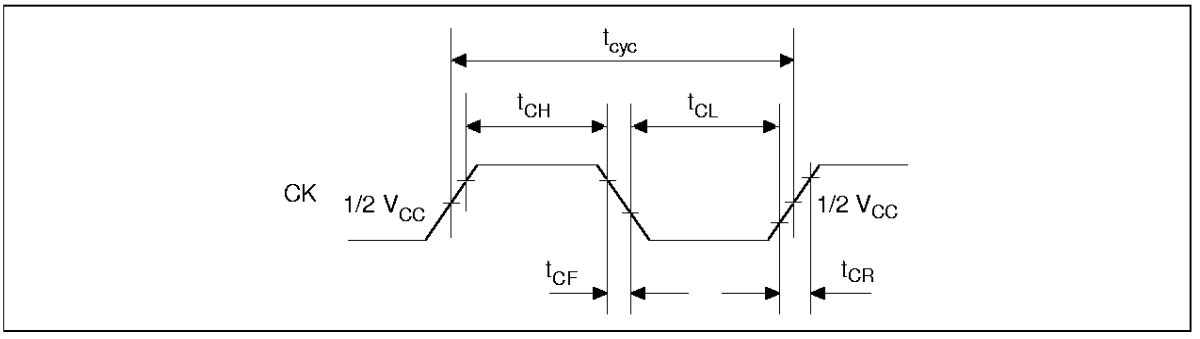

Figure 3 System Clock Timing

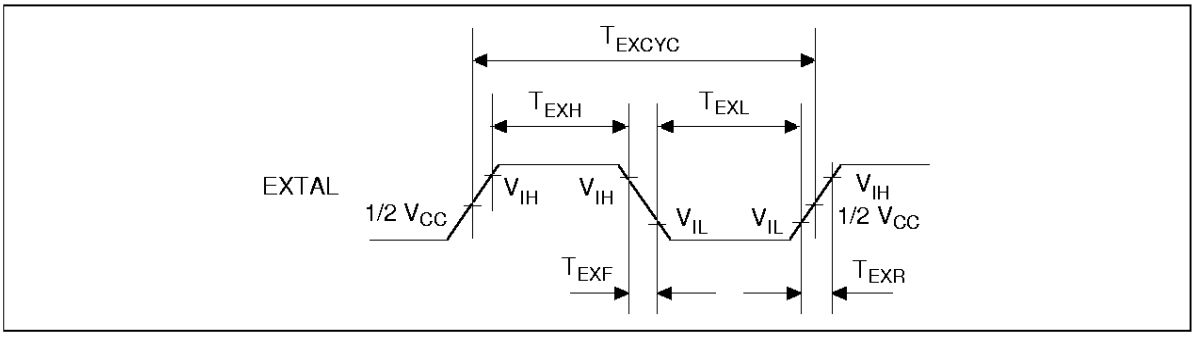

Figure 4 EXTAL Clock Input Timing

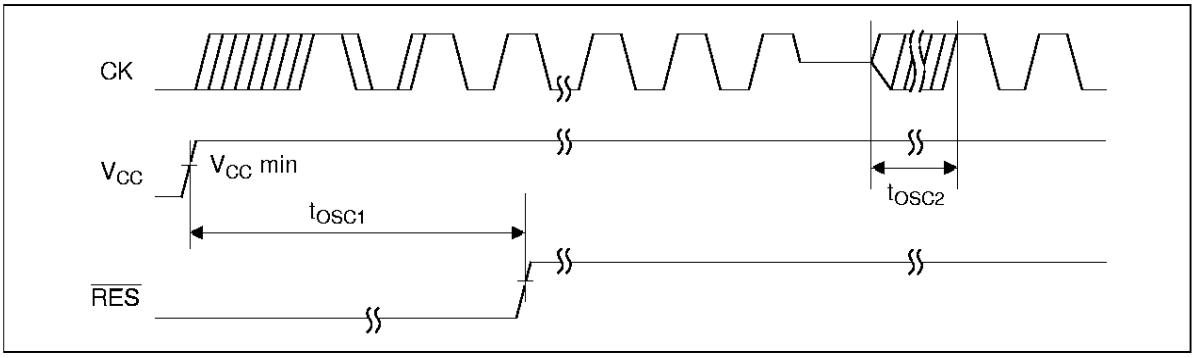

Figure 5 Oscillation Settling Time

Pin Diagrams

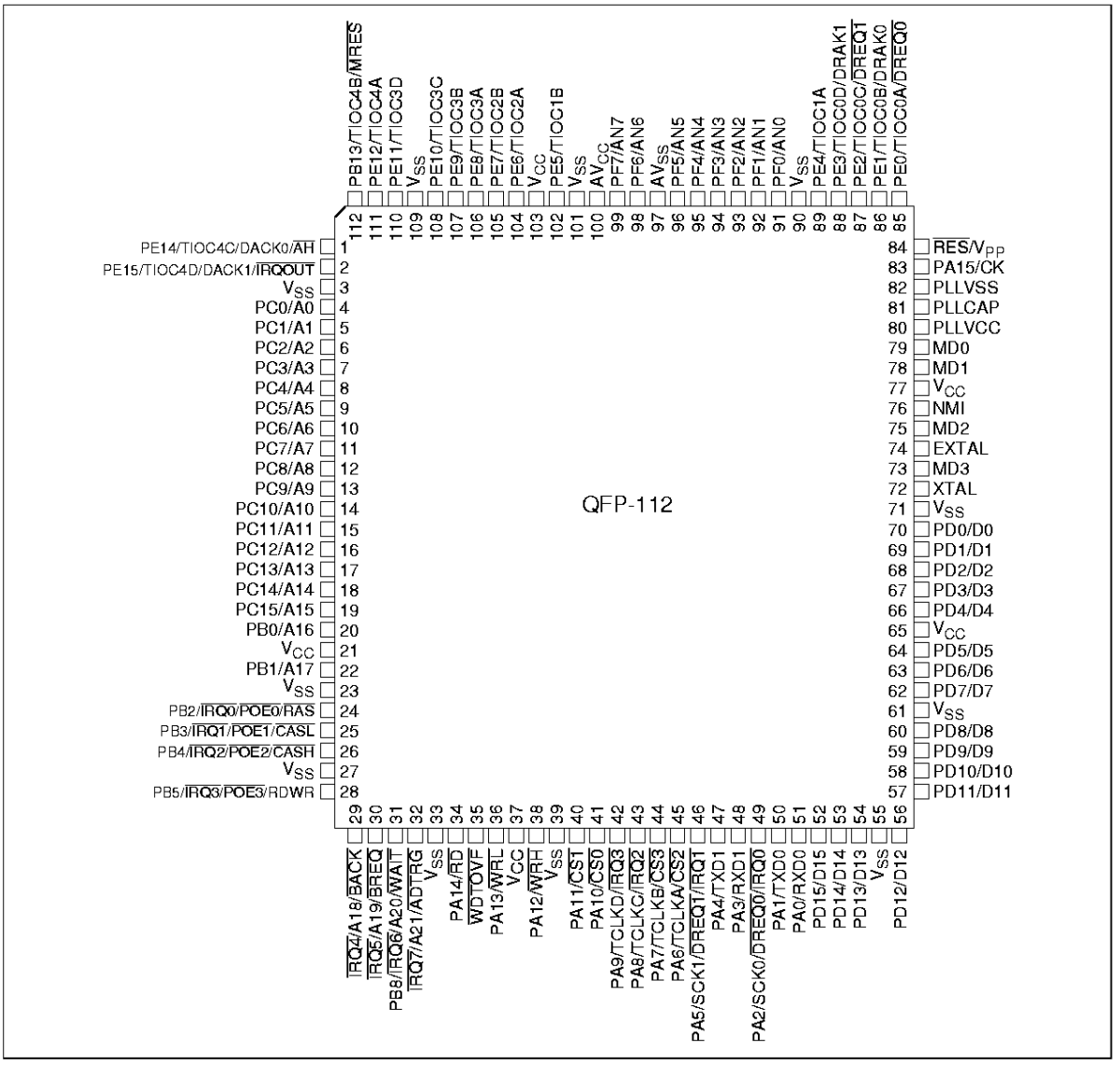

Figure 6 SH7040/42 Pin Diagram (QFP-112)

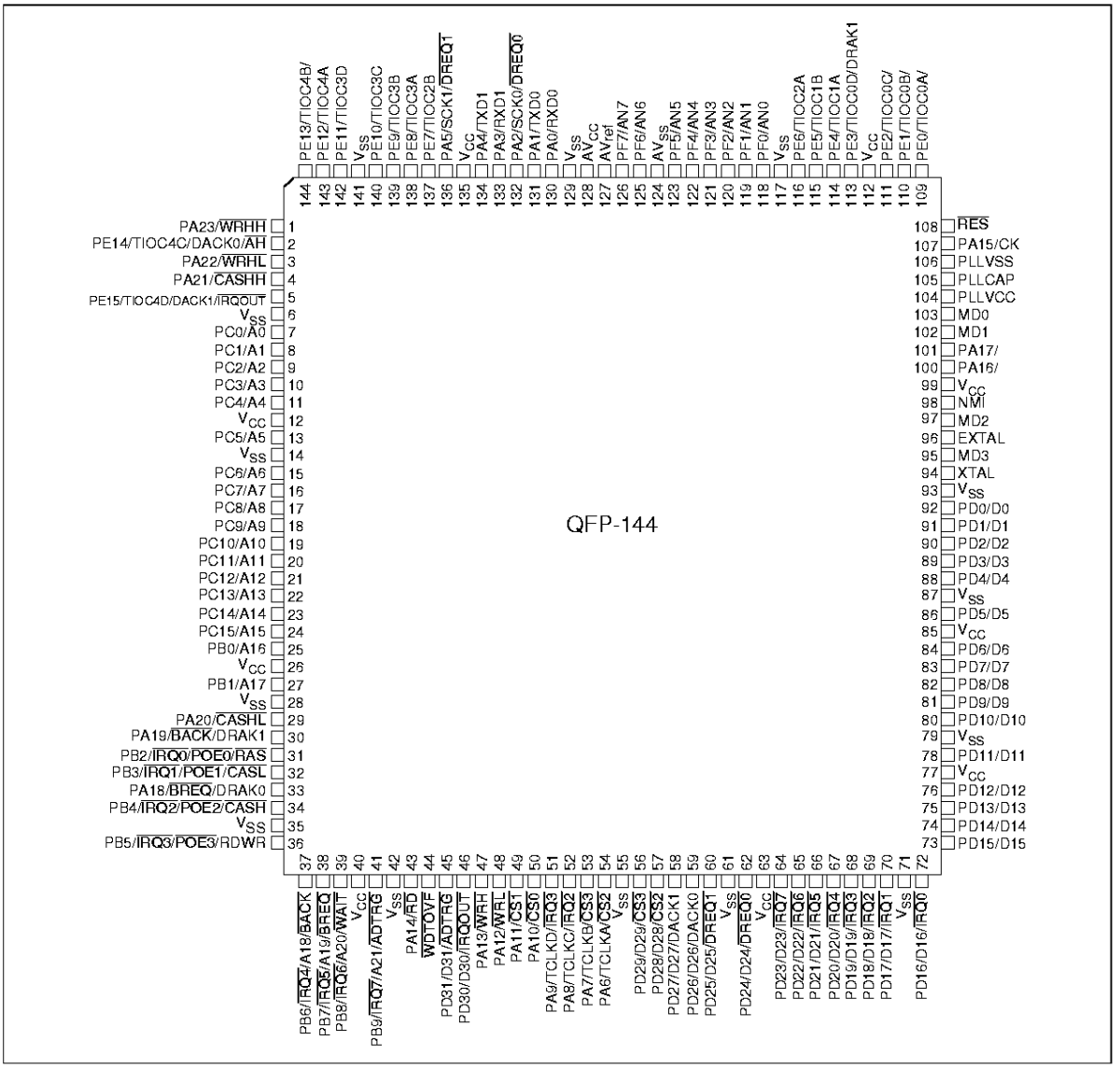

Figure 7 SH7041/43 Pin Diagram (QFP-144)

Package Information

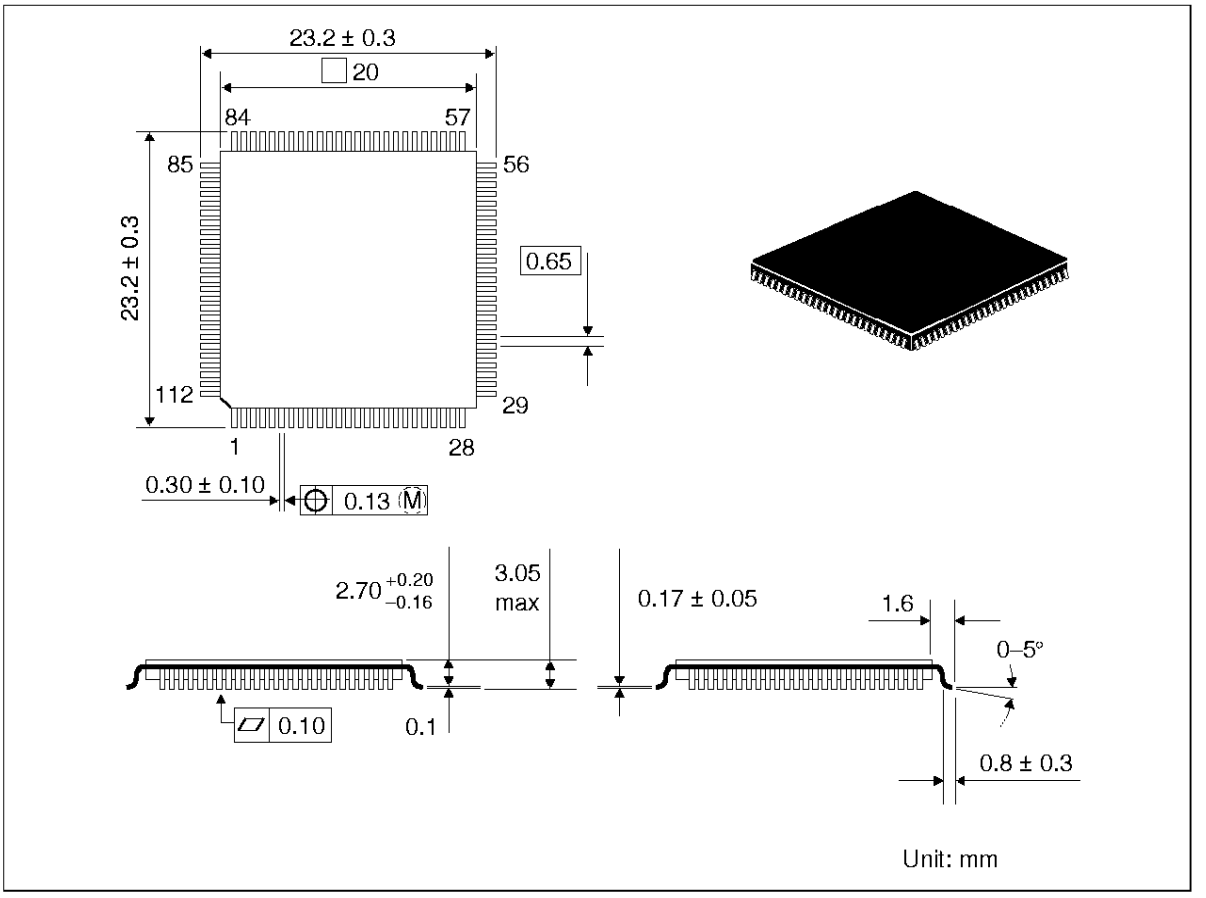

Figure 8 SH7040/42 Package Dimensions (QFP-112)

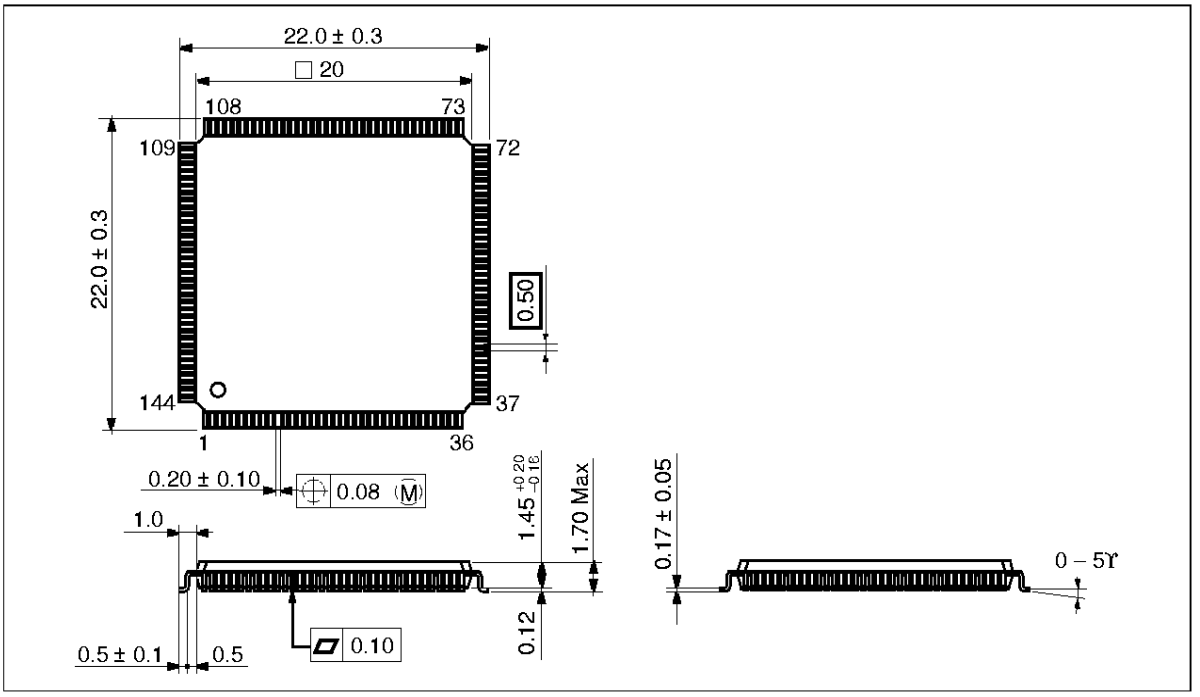

Figure 9 SH7041/43 Package Dimensions (QFP-144)

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