

## 3.3V/2.5V 1:11 LVCMOS Zero Delay Clock Generator

The MPC9352 is a 3.3V or 2.5V compatible, 1:11 PLL based clock generator targeted for high performance clock tree applications. With output frequencies up to 200 MHz and output skews lower than 200 ps the device meets the needs of most demanding clock applications.

### Features

- Configurable 11 outputs LVCMOS PLL clock generator
- Fully integrated PLL
- Wide range of output clock frequency of 16.67 MHz to 200 MHz
- Multiplication of the input reference clock frequency by 3, 2, 1, 3 ÷ 2, 2 ÷ 3, 1 ÷ 3 and 1 ÷ 2
- 2.5V and 3.3V LVCMOS compatible
- Maximum output skew of 200 ps
- Supports zero-delay applications
- Designed for high-performance telecom, networking and computing applications
- 32 lead LQFP package
- Ambient Temperature Range -40°C to +85°C

### Functional Description

The MPC9352 is a fully 3.3V or 2.5V compatible PLL clock generator and clock driver. The device has the capability to generate output clock signals of 16.67 to 200 MHz from external clock sources. The internal PLL optimized for its frequency range and does not require external loop filter components. One output of the MPC9352 has to be connected to the PLL feedback input FB\_IN to close the external PLL feedback path. The output divider of this output setting determines the PLL frequency multiplication factor. This multiplication factor, F\_RANGE and the reference clock frequency must be selected to situate the VCO in its specified lock range. The frequency of the clock outputs can be configured individually for all three output banks by the FSELx pins supporting systems with different but phase-aligned clock frequencies.

The PLL of the MPC9352 minimizes the propagation delay and therefore supports zero-delay applications. All inputs and outputs are LVCMOS compatible. The outputs are optimized to drive parallel terminated 50Ω transmission lines. Alternatively, each output can drive up to two series terminated transmission lines giving the device an effective fanout of 22.

The device also supports output high-impedance disable and a PLL bypass mode for static system test and diagnosis. The MPC9352 is package in a 32 ld LQFP.

**MPC9352**

**LOW VOLTAGE  
3.3V/2.5V LVCMOS 1:11  
CLOCK GENERATOR**



**FA SUFFIX  
32 LEAD LQFP PACKAGE  
CASE 873A**



**Table 1: PIN CONFIGURATION**

Pin	I/O	Type	Function
CCLK	Input	LVC MOS	PLL reference clock signal
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to an output
F_RANGE	Input	LVC MOS	PLL frequency range select
FSELA	Input	LVC MOS	Frequency divider select for bank A outputs
FSELB	Input	LVC MOS	Frequency divider select for bank B outputs
FSELC	Input	LVC MOS	Frequency divider select for bank C outputs
PLL_EN	Input	LVC MOS	PLL enable/disable
MR/OE	Input	LVC MOS	Output enable/disable (high-impedance tristate) and device reset
QA0-4, QB0-3, QC0-1	Output	LVC MOS	Clock outputs
GND	Supply	Ground	Negative power supply
VCCA	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V <sub>CCA</sub> . Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core

**Table 2: FUNCTION TABLE**

Control	Default	0	1
F_RANGE, FSELA, FSELB, and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 1 and Table 2 for supported frequency ranges and output to input frequency ratios.			
F_RANGE	0	VCO ÷ 1 (High input frequency range)	VCO ÷ 2 (Low input frequency range)
FSELA	0	Output divider ÷ 4	Output divider ÷ 6
FSELB	0	Output divider ÷ 4	Output divider ÷ 2
FSELC	0	Output divider ÷ 2	Output divider ÷ 4
MR/OE	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset, the PLL feedback loop is open and the VCO is operating at its lowest frequency. The MPC9352 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CCLK).
PLL_EN	0	Normal operation mode with PLL enabled.	Test mode with PLL disabled. CCLK is substituted for the internal VCO output. MPC9352 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.

**Table 3: GENERAL SPECIFICATIONS**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$V_{TT}$	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
$C_{PD}$	Power Dissipation Capacitance		10		pF	Per output
$C_{IN}$	Input Capacitance		4.0		pF	Inputs

**Table 4: ABSOLUTE MAXIMUM RATINGS<sup>a</sup>**

Symbol	Characteristics	Min	Max	Unit	Condition
$V_{CC}$	Supply Voltage	-0.3	3.6	V	
$V_{IN}$	DC Input Voltage	-0.3	$V_{CC}+0.3$	V	
$V_{OUT}$	DC Output Voltage	-0.3	$V_{CC}+0.3$	V	
$I_{IN}$	DC Input Current		$\pm 20$	mA	
$I_{OUT}$	DC Output Current		$\pm 50$	mA	
$T_S$	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 5: DC CHARACTERISTICS** ( $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ$  to  $85^\circ C$ )

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$V_{IH}$	Input high voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
$V_{IL}$	Input low voltage			0.8	V	LVC MOS
$V_{OH}$	Output High Voltage	2.4			V	$I_{OH} = -24$ mA <sup>a</sup>
$V_{OL}$	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24$ mA $I_{OL} = 12$ mA
$Z_{OUT}$	Output impedance		14 - 17		$\Omega$	
$I_{IN}$	Input Current <sup>b</sup>			$\pm 200$	$\mu A$	$V_{IN} = V_{CC}$ or $V_{IN} = GND$
$I_{CCA}$	Maximum PLL Supply Current		3.0	5.0	mA	$V_{CCA}$ Pin
$I_{CCQ}^c$	Maximum Quiescent Supply Current			1.0	mA	All $V_{CC}$ Pins

- a The MPC9352 is capable of driving  $50\Omega$  transmission lines on the incident edge. Each output drives one  $50\Omega$  parallel terminated transmission line to a termination voltage of  $V_{TT}$ . Alternatively, the device drives up to two  $50\Omega$  series terminated transmission lines.
- b Inputs have pull-down resistors affecting the input current.
- c  $I_{CCQ}$  is the DC current consumption of the device with all outputs open in high impedance state and the inputs in its default state or open.

**Table 6: AC CHARACTERISTICS** ( $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ$  to  $85^\circ C$ )<sup>a</sup>

Symbol	Characteristics	Min	Typ	Max	Unit	Condition	
$f_{ref}$	Input reference frequency in PLL mode <sup>b</sup>	+4 feedback	50.0		100.0	MHz	
		+6 feedback	33.3		66.6	MHz	
		+8 feedback	25.0		50.0	MHz	
		+12 feedback	16.67		33.3	MHz	
	Input reference frequency in PLL bypass mode <sup>c</sup>				250.0	MHz	
$f_{VCO}$	VCO lock frequency range <sup>d</sup>	200		400	MHz		
$f_{MAX}$	Output Frequency	+2 output <sup>e</sup>	100		200	MHz	
		+4 output	50		100	MHz	
		+6 output	33.3		66.6	MHz	
		+8 output	25		50	MHz	
		+12 output	16.67		33.3	MHz	
$f_{refDC}$	Reference Input Duty Cycle	25		75	%		
$t_r, t_f$	CCLK Input Rise/Fall Time			1.0	ns	0.8 to 2.0V	
$t_{(\emptyset)}$	Propagation Delay CCLK to FB_IN (static phase offset)	$f_{ref} > 40$ MHz	-50		+150	ps	PLL locked
		$f_{ref} < 40$ MHz	-200		+150	ps	
$t_{sk(O)}$	Output-to-output Skew <sup>f</sup>	all outputs, any frequency			200	ps	
		within QA output bank			200	ps	
		within QB output bank			100	ps	
		within QC output bank			100	ps	
DC	Output duty cycle	47	50	53	%		
$t_r, t_f$	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V	
$t_{PLZ, HZ}$	Output Disable Time			8	ns		
$t_{PZL, LZ}$	Output Enable Time			10	ns		
$t_{JIT(CC)}$	Cycle-to-cycle jitter	output frequencies mixed			400	ps	
		outputs are in any +4 and +6 combination			250	ps	
		all outputs same frequency			100	ps	
$t_{JIT(PER)}$	Period Jitter	output frequencies mixed			200	ps	
		outputs are in any +4 and +6 combination			150	ps	
		all outputs same frequency			75	ps	
$t_{JIT(\emptyset)}$	I/O Phase Jitter	+4 feedback divider RMS (1 $\sigma$ ) <sup>g</sup>		15		ps	
		+6 feedback divider RMS (1 $\sigma$ )		20		ps	
		+8 feedback divider RMS (1 $\sigma$ )		18 - 20		ps	
		+12 feedback divider RMS (1 $\sigma$ )		25		ps	
BW	PLL closed loop bandwidth <sup>h</sup>	+4 feedback		3.0 - 10.0		MHz	
		+6 feedback		1.5 - 6.0		MHz	
		+8 feedback		1.0 - 3.5		MHz	
		+12 feedback		0.5 - 2.0		MHz	
$t_{LOCK}$	Maximum PLL Lock Time			10	ms		

a AC characteristics apply for parallel output termination of  $50\Omega$  to  $V_{TT}$ .

b PLL mode requires  $PLL\_EN=0$  to enable the PLL and zero-delay operation. It is not recommended to use a +2 divider for feedback.

c In PLL bypass mode, the MPC9352 divides the input reference clock.

d The input frequency  $f_{ref}$  on CCLK must match the VCO frequency range divided by the feedback divider ratio FB:  $f_{ref} = f_{VCO} \div FB$ .

e See Table 9 and Table 10 for output divider configurations.

f See application section for part-to-part skew calculation.

g See application section for a jitter calculation for other confidence factors than 1  $\sigma$ .

h -3 dB point of PLL transfer characteristics.

**Table 7: DC CHARACTERISTICS** ( $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ$  to  $85^\circ C$ )

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$V_{IH}$	Input high voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
$V_{IL}$	Input low voltage	-0.3		0.7	V	LVC MOS
$V_{OH}$	Output High Voltage	1.8			V	$I_{OH} = -15 \text{ mA}^a$
$V_{OL}$	Output Low Voltage			0.6	V	$I_{OL} = 15 \text{ mA}$
$Z_{OUT}$	Output impedance		17 - 20		$\Omega$	
$I_{IN}$	Input Current			$\pm 200$	$\mu A$	$V_{IN} = V_{CC}$ or GND
$I_{CCA}$	Maximum PLL Supply Current		2.0	5.0	mA	$V_{CCA}$ Pin
$I_{CCQb}$	Maximum Quiescent Supply Current			1.0	mA	All $V_{CC}$ Pins

- a The MPC9352 is capable of driving  $50\Omega$  transmission lines on the incident edge. Each output drives one  $50\Omega$  parallel terminated transmission line to a termination voltage of  $V_{TT}$ . Alternatively, the device drives up to two  $50\Omega$  series terminated transmission lines per output.
- b  $I_{CCQ}$  is the DC current consumption of the device with all outputs open in high impedance state and the inputs in its default state or open.

**Table 8: AC CHARACTERISTICS** ( $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ$  to  $85^\circ C$ )<sup>a</sup>

Symbol	Characteristics	Min	Typ	Max	Unit	Condition	
$f_{ref}$	Input reference frequency in PLL mode <sup>b</sup>	+4 feedback	50.0		100.0	MHz	
		+6 feedback	33.3		66.6	MHz	
		+8 feedback	25.0		50.0	MHz	
		+12 feedback	16.67		33.3	MHz	
	Input reference frequency in PLL bypass mode <sup>c</sup>				250.0	MHz	
$f_{VCO}$	VCO lock frequency range <sup>d</sup>	200		400	MHz		
$f_{MAX}$	Output Frequency	+2 output <sup>e</sup>	100		200	MHz	
		+4 output	50		100	MHz	
		+6 output	33.3		66.6	MHz	
		+8 output	25		50	MHz	
		+12 output	16.67		33.3	MHz	
$f_{refDC}$	Reference Input Duty Cycle	25		75	%		
$t_r, t_f$	CCLK Input Rise/Fall Time			1.0	ns	0.8 to 2.0V	
$t_{(\phi)}$	Propagation Delay CCLK to FB_IN (static phase offset)	$f_{ref} > 40$ MHz	-50		+150	ps	PLL locked
		$f_{ref} < 40$ MHz	-200		+150	ps	
$t_{sk(O)}$	Output-to-output Skew <sup>f</sup>	all outputs, any frequency			200	ps	
		within QA output bank			200	ps	
		within QB output bank			100	ps	
		within QC output bank			100	ps	
DC	Output duty cycle	47	50	53	%		
$t_r, t_f$	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V	
$t_{PLZ, HZ}$	Output Disable Time			8	ns		
$t_{PZL, ZH}$	Output Enable Time			10	ns		
$t_{JIT(CC)}$	Cycle-to-cycle jitter	output frequencies mixed			400	ps	
		outputs are in any +4 and +6 combination			250	ps	
		all outputs same frequency			100	ps	
$t_{JIT(PER)}$	Period Jitter	output frequencies mixed			200	ps	
		outputs are in any +4 and +6 combination			150	ps	
		all outputs same frequency			75	ps	
$t_{JIT(\phi)}$	I/O Phase Jitter	+4 feedback divider RMS (1 $\sigma$ ) <sup>g</sup>		15		ps	
		+6 feedback divider RMS (1 $\sigma$ )		20		ps	
		+8 feedback divider RMS (1 $\sigma$ )		18 - 20		ps	
		+12 feedback divider RMS (1 $\sigma$ )		25		ps	
BW	PLL closed loop bandwidth <sup>h</sup>	+4 feedback		1.0 - 8.0		MHz	
		+6 feedback		0.7 - 3.0		MHz	
		+8 feedback		0.5 - 2.5		MHz	
		+12 feedback		0.4 - 1.0		MHz	
$t_{LOCK}$	Maximum PLL Lock Time			10	ms		

a AC characteristics apply for parallel output termination of  $50\Omega$  to  $V_{TT}$ .

b PLL mode requires  $PLL\_EN=0$  to enable the PLL and zero-delay operation. It is not recommended to use a +2 divider for feedback.

c In PLL bypass mode, the MPC9352 divides the input reference clock.

d The input frequency  $f_{ref}$  on CCLK must match the VCO frequency range divided by the feedback divider ratio FB:  $f_{ref} = f_{VCO} \div FB$ .

e See Table 9 and Table 10 for output divider configurations.

f See application section for part-to-part skew calculation.

g See application section for a jitter calculation for other confidence factors than 1  $\sigma$ .

h -3 dB point of PLL transfer characteristics.

## APPLICATIONS INFORMATION

## Programming the MPC9352

The MPC9352 supports output clock frequencies from 16.67 to 200 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 400 MHz for stable and optimal operation. The FSELA, FSELB, FSELC pins select the

desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:1, 1:2, 1:3, 3:2 as well as 2:3, 3:1 and 2:1. Table 1 illustrates the various output configurations and frequency ratios supported by the MPC9352. See also Table 9, Table 10 and Figure 3 to Figure 6 for further reference. A  $\div 2$  output divider cannot be used for feedback.

Table 9: MPC9352 Example Configuration (F\_RANGE = 0)

PLL Feedback	fref <sup>a</sup> [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO $\div 4^b$	50-100	0	0	0	fref (50-100 MHz)	fref (50-100 MHz)	fref $\cdot 2$ (100-200 MHz)
		0	0	1	fref (50-100 MHz)	fref (50-100 MHz)	fref (50-100 MHz)
		1	0	0	fref $\cdot 2\div 3$ (33-66 MHz)	fref (50-100 MHz)	fref $\cdot 2$ (100-200 MHz)
		1	0	1	fref $\cdot 2\div 3$ (33-66 MHz)	fref (50-100 MHz)	fref (50-100 MHz)
VCO $\div 6^c$	33.3-66.67	1	0	0	fref (33-66 MHz)	fref $\cdot 3\div 2$ (50-100 MHz)	fref $\cdot 3$ (100-200 MHz)
		1	0	1	fref (33-66 MHz)	fref $\cdot 3\div 2$ (50-100 MHz)	fref $\cdot 3\div 2$ (50-100 MHz)
		1	1	0	fref (33-66 MHz)	fref $\cdot 3$ (100-200 MHz)	fref $\cdot 3$ (100-200 MHz)
		1	1	1	fref (33-66 MHz)	fref $\cdot 3$ (100-200 MHz)	fref $\cdot 3\div 2$ (50-100 MHz)

- a. fref is the input clock reference frequency (CLK)
- b. QAx connected to FB\_IN and FSELA=0
- c. QAx connected to FB\_IN and FSELA=1

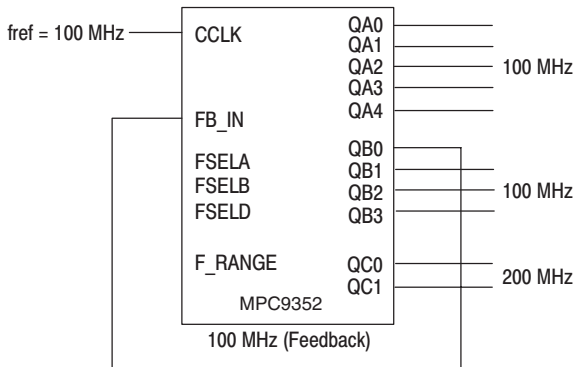
Table 10: MPC9352 Example Configurations (F\_RANGE = 1)

PLL Feedback	fref <sup>a</sup> [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO $\div 8^b$	25-50	0	0	0	fref (25-50 MHz)	fref (25-50 MHz)	fref $\cdot 2$ (50-100 MHz)
		0	0	1	fref (25-50 MHz)	fref (25-50 MHz)	fref (25-50 MHz)
		1	0	0	fref $\cdot 2\div 3$ (16-33 MHz)	fref (25-50 MHz)	fref $\cdot 2$ (50-100 MHz)
		1	0	1	fref $\cdot 2\div 3$ (16-33 MHz)	fref (25-50 MHz)	fref (25-50 MHz)
VCO $\div 12^c$	16.67-33.3	1	0	0	fref (16-33 MHz)	fref $\cdot 3\div 2$ (25-50 MHz)	fref $\cdot 3$ (50-100 MHz)
		1	0	1	fref (16-33 MHz)	fref $\cdot 3\div 2$ (25-50 MHz)	fref $\cdot 3\div 2$ (25-50 MHz)
		1	1	0	fref (16-33 MHz)	fref $\cdot 3$ (50-100 MHz)	fref $\cdot 3$ (50-100 MHz)
		1	1	1	fref (16-33 MHz)	fref $\cdot 3$ (50-100 MHz)	fref $\cdot 3\div 2$ (25-50 MHz)

- a. fref is the input clock reference frequency (CLK)
- b. QAx connected to FB\_IN and FSELA=0
- c. QAx connected to FB\_IN and FSELA=1

Example Configurations for the MPC9352

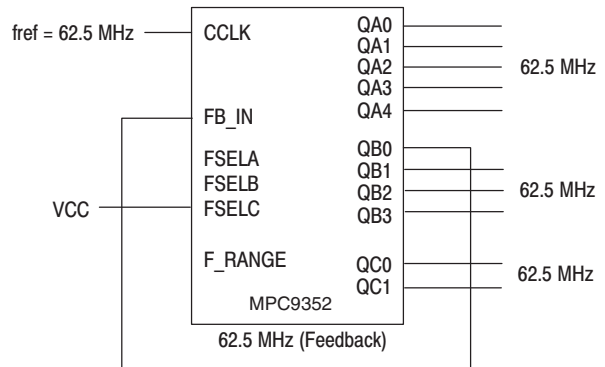
Figure 3. MPC9352 Default Configuration



MPC9352 default configuration (feedback of QB0 = 100 MHz). All control pins are left open.

Frequency range	Min	Max
Input	50 MHz	100 MHz
QA outputs	50 MHz	10 MHz
QB outputs	50 MHz	100 MHz
QC outputs	100 MHz	200 MHz

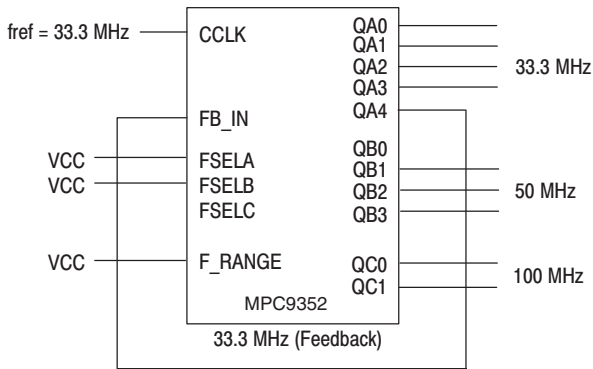
Figure 4. MPC9352 Zero Delay Buffer Configuration



MPC9352 zero-delay (feedback of QB0 = 62.5 MHz). All control pins are left open except FSELB = 1. All outputs are locked in frequency and phase to the input clock.

Frequency range	Min	Max
Input	50 MHz	100 MHz
QA outputs	50 MHz	10 MHz
QB outputs	50 MHz	100 MHz
QC outputs	50 MHz	100 MHz

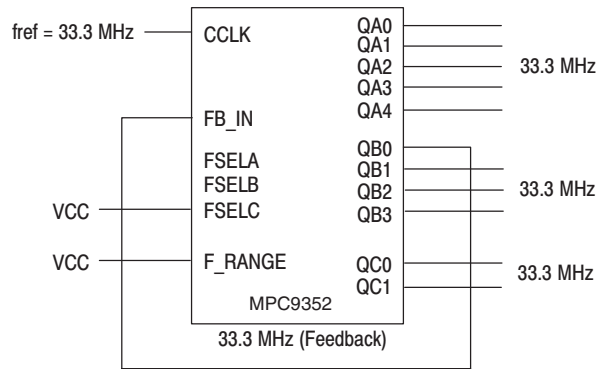
Figure 5. MPC9352 Default Configuration



MPC9352 configuration to multiply the reference frequency by 3, 3+2 and 1. PLL feedback of QA4 = 33.3 MHz.

Frequency range	Min	Max
Input	25 MHz	50 MHz
QA outputs	50 MHz	10 MHz
QB outputs	50 MHz	100 MHz
QC outputs	100 MHz	200 MHz

Figure 6. MPC9352 Zero Delay Buffer Config. 2



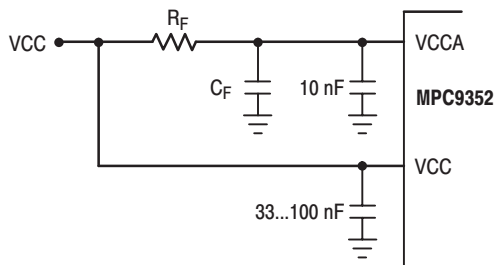
MPC9352 zero-delay (feedback of QB0 = 33.3 MHz). Equivalent to Table 2 except F\_RANGE = 1 enabling a lower input and output clock frequency.

Frequency range	Min	Max
Input	25 MHz	50 MHz
QA outputs	25 MHz	50 MHz
QB outputs	25 MHz	50 MHz
QC outputs	25 MHz	50 MHz

**Power Supply Filtering**

The MPC9352 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V<sub>CCA</sub> (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9352 provides separate power supplies for the output buffers (V<sub>CC</sub>) and the phase-locked loop (V<sub>CCA</sub>) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V<sub>CCA</sub> pin for the MPC9352. Figure 7. illustrates a typical power supply filter scheme. The MPC9352 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R<sub>F</sub>. From the data sheet the I<sub>CCA</sub> current (the current sourced through the V<sub>CCA</sub> pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V (V<sub>CC</sub>=3.3V or V<sub>CC</sub>=2.5V) must be maintained on the V<sub>CCA</sub> pin. The resistor R<sub>F</sub> shown in Figure 7. “V<sub>CCA</sub> Power Supply Filter” should have a resistance of 5–15Ω (V<sub>CC</sub>=3.3V) or 9-10Ω (V<sub>CC</sub>=2.5V) to meet the voltage drop criteria.

R<sub>F</sub> = 5–15Ω for V<sub>CC</sub> = 3.3V  
 R<sub>F</sub> = 9–10Ω for V<sub>CC</sub> = 2.5V  
 C<sub>F</sub> = 22 μF for V<sub>CC</sub> = 3.3V  
 C<sub>F</sub> = 22 μF for V<sub>CC</sub> = 2.5V



**Figure 7. V<sub>CCA</sub> Power Supply Filter**

The minimum values for R<sub>F</sub> and the filter capacitor C<sub>F</sub> are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7. “V<sub>CCA</sub> Power Supply Filter”, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9352 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power

supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Using the MPC9352 in zero-delay applications**

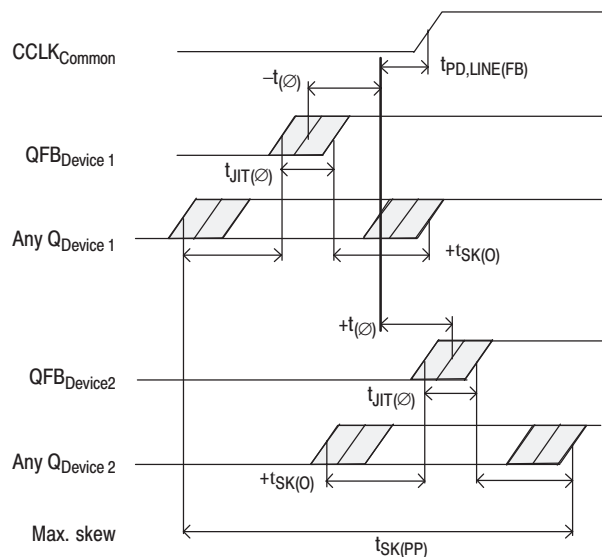
Nested clock trees are typical applications for the MPC9352. Designs using the MPC9352 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9352 clock driver allows for its use as a zero delay buffer. One example configuration is to use a +4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

**Calculation of part-to-part skew**

The MPC9352 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9352 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:



**Figure 8. MPC9352 max. device-to-device skew**

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 11.

**Table 11: Confidence Factor CF**

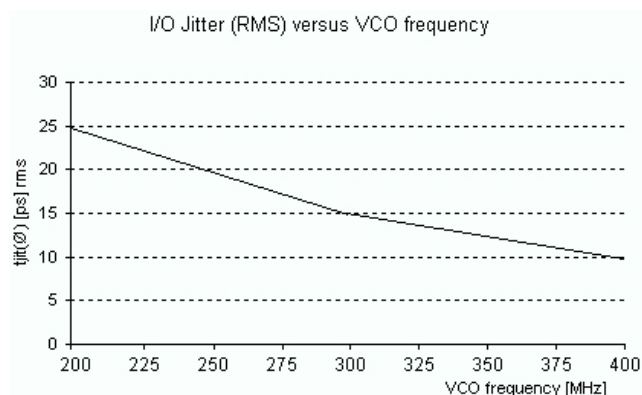
CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ( $\pm 3\sigma$ ) is assumed, resulting in a worst case timing uncertainty from input to any output of -445 ps to 395 ps relative to CCLK:

$$t_{SK(PP)} = [-200ps...150ps] + [-200ps...200ps] + [(15ps \cdot -3)...(15ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-445ps...395ps] + t_{PD, LINE(FB)}$$

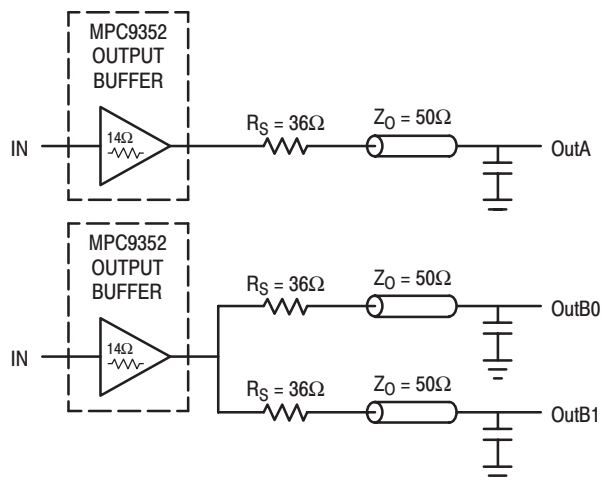
Due to the frequency dependence of the I/O jitter, Figure 9. “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

**Figure 9. Max. I/O Jitter versus frequency**

### Driving Transmission Lines

The MPC9352 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to  $V_{CC} \div 2$ .

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9352 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 10. “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9352 clock driver is effectively doubled due to its capability to drive multiple lines.

**Figure 10. Single versus Dual Transmission Lines**

The waveform plots in Figure 11. “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9352 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9352. The output waveform in Figure 11. “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$

$$Z_0 = 50\Omega \parallel 50\Omega$$

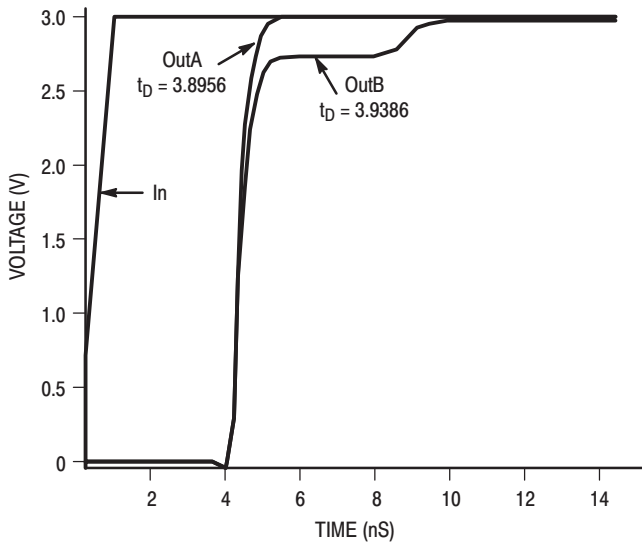
$$R_S = 36\Omega \parallel 36\Omega$$

$$R_0 = 14\Omega$$

$$V_L = 3.0 ( 25 \div (18+17+25))$$

$$= 1.31V$$

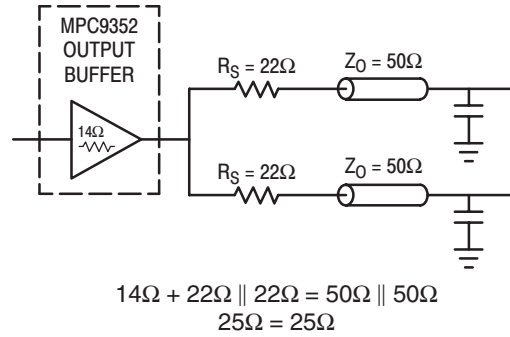
At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).



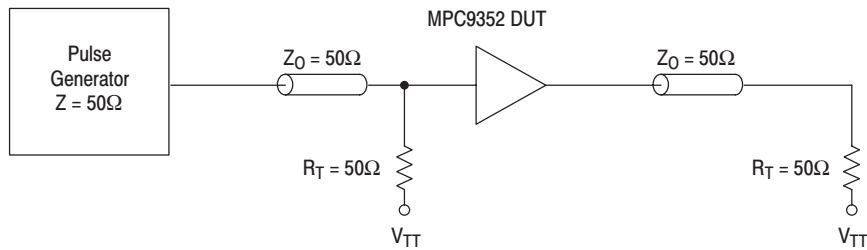
**Figure 11. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better

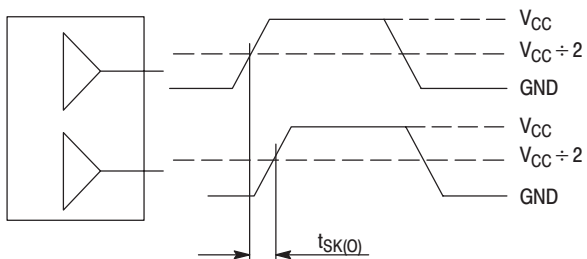
match the impedances when driving multiple lines the situation in Figure 12. “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



**Figure 12. Optimized Dual Line Termination**

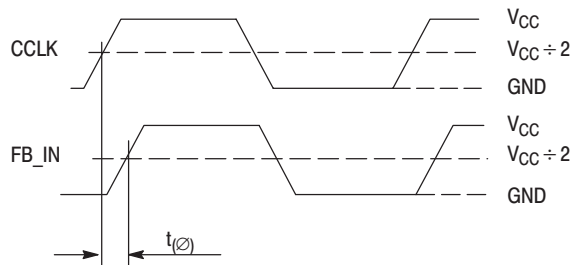


**Figure 13. CCLK MPC9352 AC test reference for  $V_{CC} = 3.3V$  and  $V_{CC} = 2.5V$**

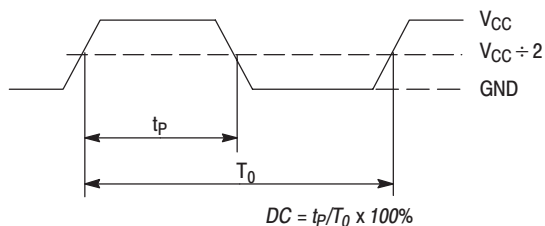


The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 14. Output-to-output Skew  $t_{SK(O)}$**

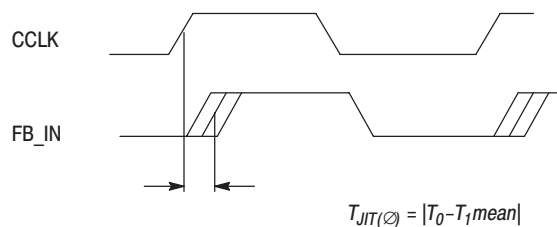


**Figure 15. Propagation delay ( $t_{\phi}$ , static phase offset) test reference**



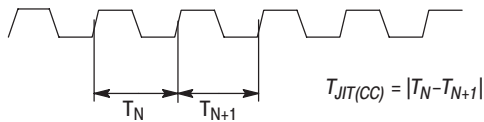
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 16. Output Duty Cycle (DC)**



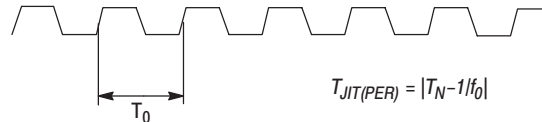
The deviation in  $t_0$  for a controlled edge with respect to a  $t_0$  mean in a random sample of cycles

**Figure 17. I/O Jitter**



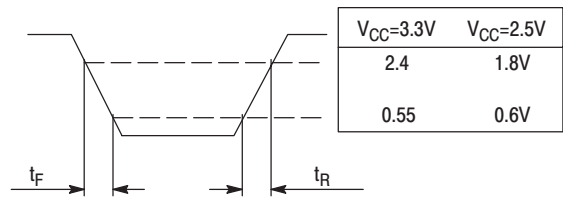
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 18. Cycle-to-cycle Jitter**



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

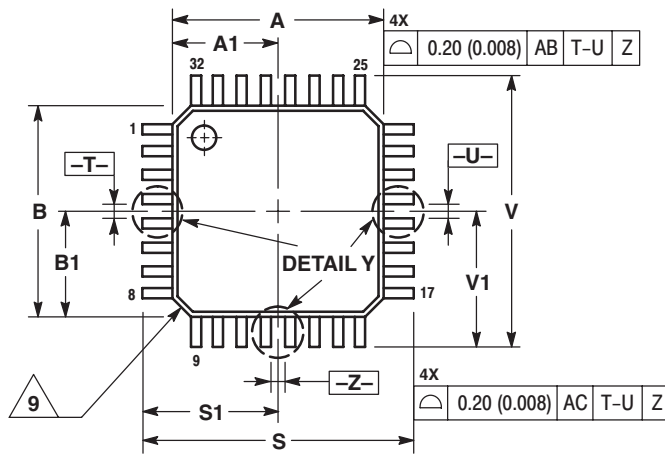
**Figure 19. Period Jitter**



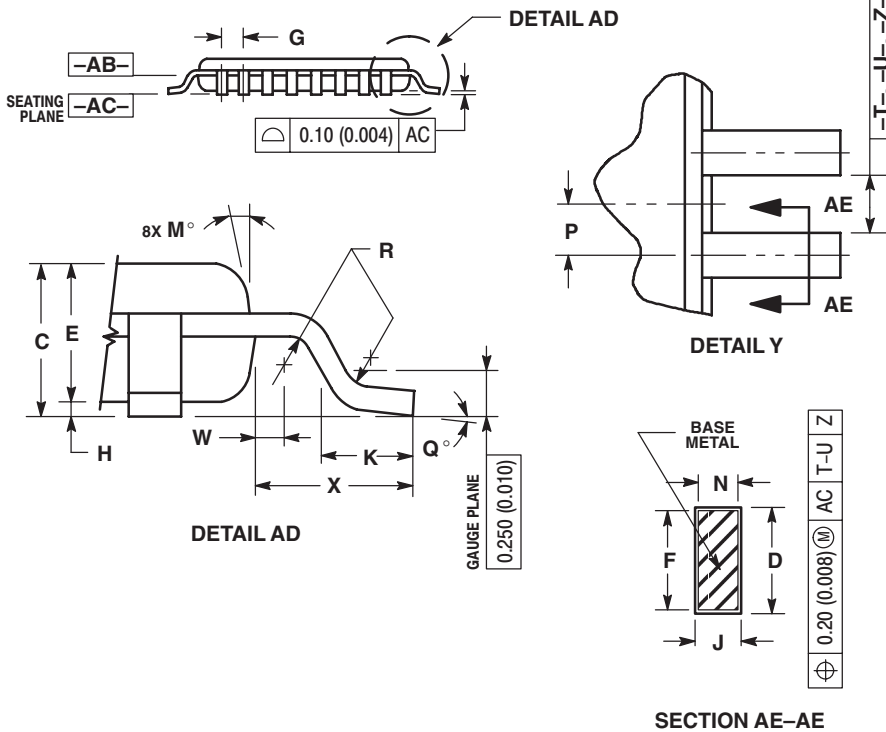
**Figure 20. Output Transition Time Test Reference**

OUTLINE DIMENSIONS

FA SUFFIX  
LQFP PACKAGE  
CASE 873A-02  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
  4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
  5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
  6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
  7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
  8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
  9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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