UCC3275

PRELIMINARY

H-Bridge Power Amplifier with 11-Bit D/A

FEATURES

- Power H-Bridge Amplifier with 11 Bit DAC
- Internal Self Test
- Four-wire 10MHz Serial Interface
- 1µs DAC Output Rise Time
- 1 Ohm On-Resistance Output Transistors
- 1.2 Amp Continuous Operation
- Orderly Shutdown with V5 as low as Zero and with VL as low as 3V
- Complete Voltage and Current Sense Amps
- 20kHz Power Amplifier Bandwidth
- Complete Park Management

DESCRIPTION

The UCC3275 is a combination Voice-Coil Motor (VCM) H-bridge amplifier and an 11 bit D/A converter (DAC). The amplifier forces the current values specified by the DAC and is feedback monitored by an on-chip current-sense instrumentation amplifier. An additional instrumentation amplifier is provided to sense the voltage across the load, providing a voltage which approximates the motor velocity. To extend the current control resolution, the current loop gain can be switched without disturbing open loop poles and zeros.

The UCC3275 is capable of parking the motor under full-power conditions. This function can be implemented under user control by using the voltage sense amplifier to derive velocity. The UCC3275 is also capable of independently controlling and sequencing a supply fault park with orderly shutdown. Parking in this mode is under voltage control, and can be powered by energy recovered from the spindle motor. The UCC3275 also provides a brake signal at the end of the fault park sequence.

The UCC3275 also contains a boost power converter and power management system. The boost regulator generates an elevated 17.5V from the power to the chip. This elevated voltage is used to drive the gates of the DMOS power devices and other functions on the IC. During a fault park, an output filter capacitor is required to provide voltage for the low-power support circuits. The power management functions include a precision voltage reference, power supply monitor comparators, a power-on reset monostable, and temperature sensing circuits. Functioning of essential blocks is maintained with input supply voltages as low as 3V so that during power faults, full control is maintained.

The UCC3275 also contains a serial interface and an 11-bit DAC, with all of the functions required to take data directly from a three-wire serial data bus and convert it to a precise voltage. The serial data interface is capable of clock frequencies as high as 10MHz. The UCC3275 accepts commands encoded as twos-complement binary.

The data converter in the UCC3275 uses a unique segmented architecture which is inherently monotonic, offers differential linearity better than 1 LSB, integral linearity better than 2 LSB, and fast conversion. This segmented conversion technique is completely static, so periodic updating is not required. This converter does not require an output sampling circuit to achieve low glitch energy and smooth transitions.

The serial interface allows data to be written into the UCC3275 which sets DAC output, power amplifier range, and system modes. The interface also allows data to be read back from the UCC3275, indicating the state of the IC and also allowing for self-test. The read-back data includes the entire write register, a thermal warning flag, and the output of the current sense comparator.

The UCC3275 can perform a system self-test using the current sense comparator and the serial interface. System performance is assured if the current sense comparator responds low to a current command below the current-sense threshold and high to a command higher than threshold.

The UCC3275 is packaged in a 44 lead power PLCC package which uses 8 leads specifically for heat conduction and grounding. This package is capable of 1.6 Watts continuous power dissipation if the heat conducting leads are directly connected to circuit board copper area of at least one square inch (645 square mm).

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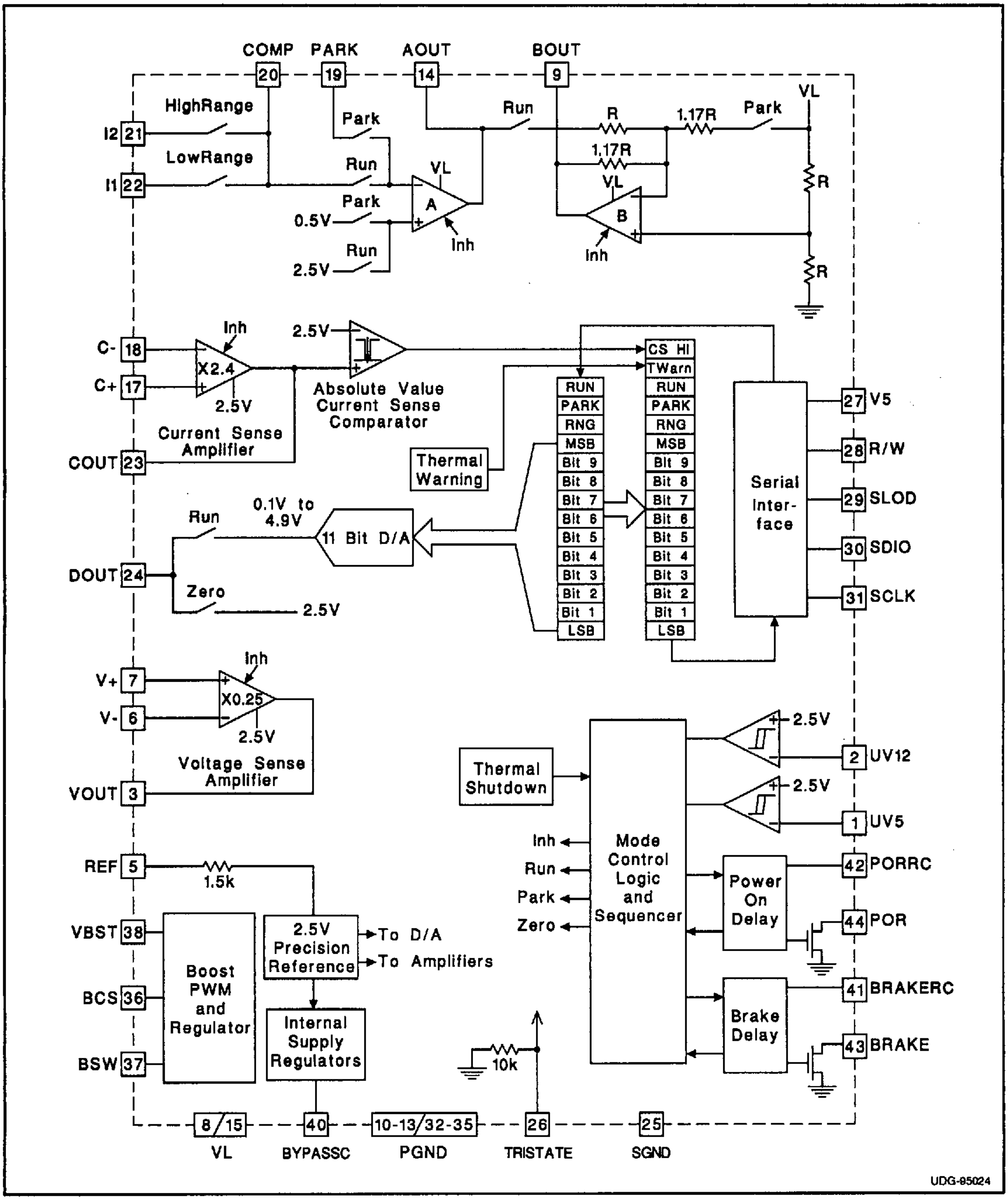
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

VL Supply Voltage	18V
V5 Supply Voltage	7V
Input Voltage	
Any Analog Input Except C-, V+	–0.3V to VL+0.3V
Input Voltage, C-, V+	–2V to VL+2V
Input Voltage, Any Digital Input	–0.3V to V5+0.3V
Output Voltage, BRAKE	–0.3V to 20V
Output Voltage, POR	–0.3V to 7V
AOUT, BOUT Peak Output Current	
(1ms on, 5% duty cycle)	±1.5A
AOUT, BOUT Continuous Output Current	±1.2A
Storage Temperature	–65°C to +150°C
Junction Temperature	–55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

All voltages with respect to GND. Currents are positive into, negative out of the specified terminal.

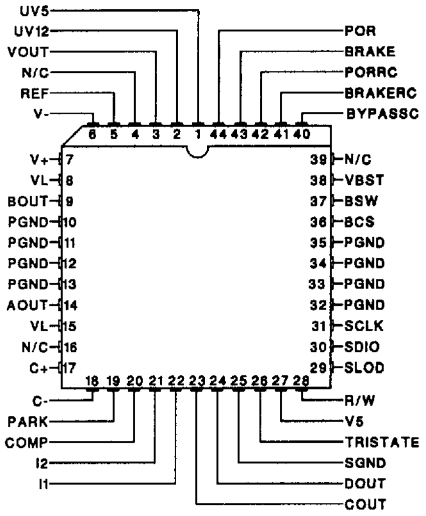
THERMAL DATA

Thermal Resistance Junction to Leads, θ_{JL}	12°C/W
Thermal Resistance Junction to Ambient, θ_{JA}	24-38°C/W

Exact thermal resistance from Junction to Ambient is a function of the circuit board material used and layout. Consult Packaging Section of Databook for additional thermal information.

CONNECTION DIAGRAM

PLCC-44 (Top View)
QP Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications apply for V5 = 5V, VL = 12V, 0°C < T_A < +70°C, and T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
VL Quiescent Current	RUN Mode, 10.8V < VL < 13.2V		12	20	mA
VL Sleep Current	SLEEP Mode, 10.8V < VL < 13.2V		1.7	3.0	mA
V5 Current	4.5V < V5 < 6V		0.1	1.0	mA
Power Op Amp Section					
Non-inverting Input Voltage, B Amp	VL = 12V	5.8	6.0	6.2	V
Input Bias Current		–345	–150		nA
Large Signal Voltage Gain, A Amp	Output Swing from 1V to 10V		70		dB
Gain-Bandwidth Product, A Amp			4.5		MHz
Phase Margin, A Amp	(Note 1)		45		degrees
Slew Rate, A Amp			1.3		V/µs
Gain, B Amp			1.17		V/V
Bandwidth, 3dB, B Amp	(Note 1)		2.3		MHz
Total Saturation Resistance, A and B Amp	I_{OUT} = 1A, VL = 11.4V		2.1	3.5	Ω
Parasitic Diode Forward Voltage Drop	I_{OUT} = 1A		1.1		V
Offset Referred to Current Sense Input	D/A Register Contains 000, Low Range, RI1 = 1.3k from COUT to I1, RD1 = 19.6k from DOUT to I1	–10		10	mV
A Amp Input Switch On Resistance	Inverting Input, (Note 1)		275		Ω
A Amp Input Capacitance, Any Input	I1, I2, COMP, or PARK, (Note 1)		9		pF
Undervoltage Comparator Section					
Rising Threshold		2.4	2.5	2.6	V
Hysteresis			40		mV
POR Reset Time	RDP = 1MΩ, CDP = 0.22µF		220		ms

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, all specifications apply for V5 = 5V, VL = 12V, 0°C < T_A < +70°C, and T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Comparator Section (cont.)					
PORRC Float Voltage	RDP = 1MΩ, CDP = 0.22µF	6.2	6.9	8.2	V
PORRC Leakage Current	PORRC = 8.2V	-1.0	0.1	1.0	µA
POR On Resistance	I_{OUT} = 10mA		15	40	Ω
POR Leakage Current	POR = 7V	-250		250	nA
Thermal Shutdown Temperature	(Note 1)		165		°C
Thermal Warning Temperature	(Note 1)		145		°C
DAC Section					
Differential Nonlinearity	V5 = 5V			1	LSB
Integral Nonlinearity	(Note 2)			2	LSB
DOUT Full Scale Output Voltage		4.75	4.90	5.05	V
DOUT Zero Scale Output Voltage		0.08	0.10	0.12	V
Conversion Time 0-90%	From Input of 14th Bit			1.0	µs
Full Scale Temperature Coefficient	0°C to 70°C (Note 1, 3)		250		ppm/°C
Power Supply Rejection	10.0V < VL < 13.2V	60	74		dB
REF Voltage	No load on REF	2.42	2.50	2.58	V
REF Output Impedance	0µA < I_{REF} < 10µA	0.5	1.5	3.0	KΩ
PARK Section					
Recommended A Amp Cont. Park Current	Set by R_{PI} & R_{PF}			100	mA
Retract Time	RDB = 1MΩ, CDB = 0.22µF		220		ms
BRAKERC Float Voltage	RDB = 1MΩ, CDB = 0.22µF	6.2	6.9	8.2	V
BRAKERC Leakage Current	BRAKERC = 8.2V	-250		250	nA
A Amp Input Reference in Park		0.475	0.500	0.525	V
B Amp Grounded Saturation Resistance	I_{OUT} = 1A		1.0	1.5	Ω
AOUT to BOUT "Park" Voltage	RPF = 0Ω, RPI disconnected, no load	0.475	0.500	0.525	V
BRAKE Low Voltage	I_{BRAKE} = 100µA		0.02	0.81	V
BRAKE Leakage Current	BRAKE = 20V			250	nA
VSENSE Amplifier Section					
Input Offset Voltage	V_{CM} = 6V	–20		20	mV
Input CMRR	0V < V_{IN} < VL			2000	µV/V
Voltage Gain	0V < V– < VL, V_{DIFF} = ±1.2V	0.23	0.25	0.27	V/V
Bandwidth, 3dB	(Note 1)		1.8		MHz
V+ to V– Differential Input Resistance			160		kΩ
Available Output Current	1V < VOUT < VL–1V	±600			µA
Current Sense Amplifier Section					
Input Offset Voltage	V_{CM} = 6V	–6		6	mV
Input CMRR	0V < V_{IN} < VL		1000	2000	µV/V
Voltage Gain	0V < C+ < VL, V_{DIFF} = ±1.2V	2.35	2.40	2.45	V/V
Bandwidth, 3dB	(Note 1)		300		kHz
Slew Rate			1.0		V/µs
Available Output Current	0V < COUT < VL	±600			µA
Current Sense Comparator Threshold	Voltage between C+ and C–		50		mV

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, all specifications apply for V5 = 5V, VL = 12V, 0°C < T_A < +70°C, and $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Serial Interface Section					
Logic Input Threshold	SCLK, SDIO, SLOD, RW, TRISTATE	1.5	2.5	3.5	V
Serial Interface Logic Input Current	SCLK, SDIO, SLOD, RW	-5		5	μA
TRISTATE Input Resistance	0V < TRISTATE < V5	5	10	20	kΩ
Logic Input Capacitance	(Note 1)			10	pF
R/W setup time to SCLK high (TRWS)		100			ns
SLOD setup time to SCLK high (TSLS)		100			ns
R/W hold time after SCLK high (TRWH)		100			ns
SLOD hold time after SCLK high (TSLH)		100			ns
R/W high to SDIO Valid from Hi-Z (TRWD)			18	50	ns
SCLK high to Data Valid (TSKD)			25	50	ns
Data setup time to SCLK high (TDS)		30			ns
Data hold time after SCLK high (TDH)		10			ns
SDIO tri-state after SLOD high (TSDZ)		30			ns
SDIO tri-state after R/W low (TRWZ)		30			ns
SCLK period (TPER)		100			ns
SCLK Duty Cycle (TDC)		40	50	60	%
Recycle Time between accesses (TREC)		100			ns
Boost Section					
Switch On Resistance	IBSW = 50mA		100		Ω
BCS Current Sense Rising Threshold Voltage		0.18	0.20	0.22	V
VBST Peak Rising Threshold		17.0	17.5	18.0	V
VBST Hysteresis			250		mV
BYPASSC Float Voltage	No Load on BYPASSC	6.2	6.9	8.2	V

Note 1: Guaranteed by design. Not 100% tested in production.

Note 2: Integral nonlinearity is defined as the worst deviation of the converter output from the best-fit straight line through all converter output codes.

Note 3: Temperature coefficient is defined by the difference between the highest value and the lowest value of the parameter in the temperature range divided by the 25°C value of the parameter, divided by the total temperature range.

SERIAL INTERFACE DATA REGISTER

BIT	LABEL	DESCRIPTION
0	D/A Bit 0	LSB
1	D/A Bit 1	
2	D/A Bit 2	
3	D/A Bit 3	
4	D/A Bit 4	
5	D/A Bit 5	
6	D/A Bit 6	
7	D/A Bit 7	
8	D/A Bit 8	
9	D/A Bit 9	
10	D/A Bit 10	MSB
11	High-Range	Gain Select; Range = 0 connects I1 (low range); Range = 1 connects I2 (high range)
12	Park	Retract. Park = 1 with Run = 1 forces retraction. If Run = 0, Park is ignored.
13	Run	Run = 0 forces AOUT and BOUT low, stops boost, reduces supply current.
14	(not used)	
15	(not used)	

SERIAL INTERFACE OUTPUT REGISTER

BIT	LABEL	DESCRIPTION
0	D/A Bit 0	LSB
1	D/A Bit 1	
2	D/A Bit 2	
3	D/A Bit 3	
4	D/A Bit 4	
5	D/A Bit 5	
6	D/A Bit 6	
7	D/A Bit 7	
8	D/A Bit 8	
9	D/A Bit 9	
10	D/A Bit 10	MSB
11	High Range	Read back Gain Select bit.
12	Park	Read back Retract bit.
13	Run	Read back Run bit.
14	T Warning	Thermal Warning - This bit is 1 if die temperature is greater than 145°C
15	CS High	CS High - This bit is 1 if the current sense amp input is greater than ±50mV

SERIAL INTERFACE DESCRIPTION

The write cycle is initiated by setting SLOD low, setting R/W low, and loading 16 data bits from SDIO with the rising edges of SCLK.

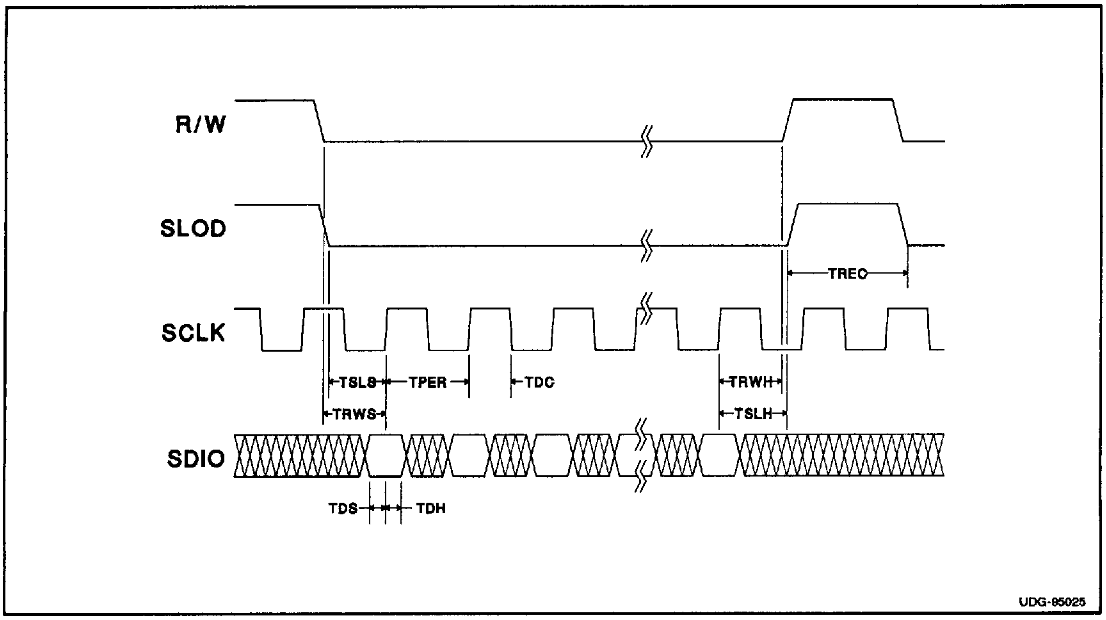
The write cycle has one register, no address bits, and 14 data bits. Data clocks into the register starting with bit 0. When 14 data bits have been clocked in and a 15th clock pulse is received, then the DATA REGISTER is loaded with the data and the commanded actions will occur. Additional clock pulses are ignored until SLOD is brought high and then low again.

The read cycle is initiated by setting SLOD low with R/W high. This causes the UCC3275 to assert the level on SDIO. The read cycle has one register, no address bits, and 16 data bits. Data is clocked onto SDIO on the rising edges of SCLK. This data contains the contents of the Serial Interface Data Register as well as two status bits. Data is clocked out of the register starting with bit 0.

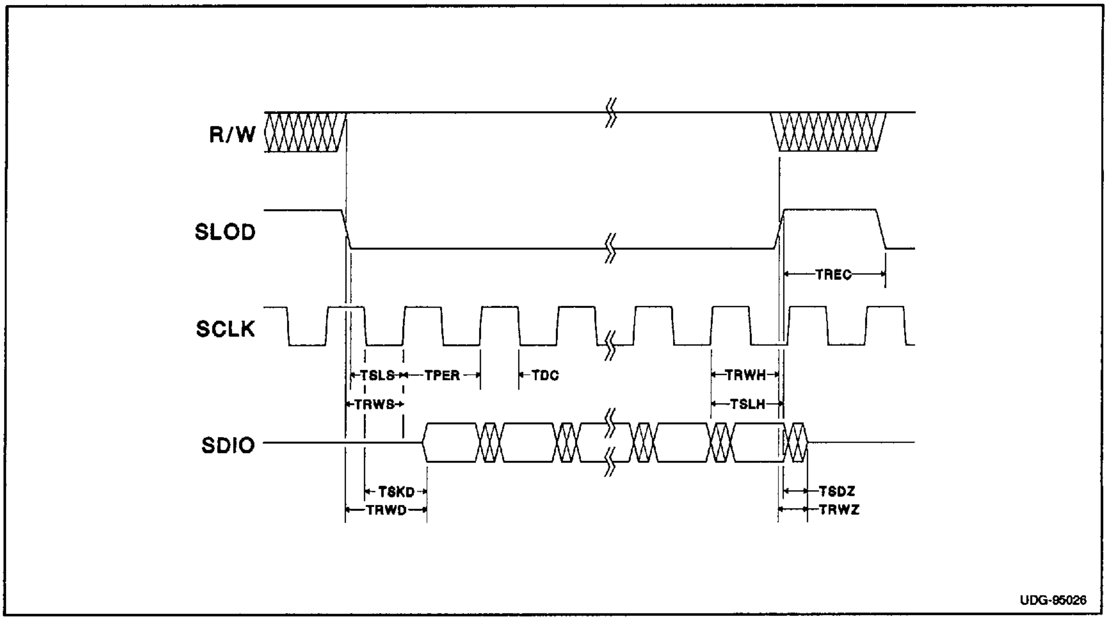
The contents of the Data Register can be used for system self-test, as can the CS High bit. The T Warning bit should be used as an alarm and should force the drive to enter a state with reduced power dissipation so that the UCC3275 and the entire drive can cool down.

Note: All data is positive logic. True, logic 1, high, and high voltage are synonymous.

SERIAL INTERFACE WRITE CYCLE TIMING DIAGRAM



SERIAL INTERFACE READ CYCLE TIMING DIAGRAM



PIN DESCRIPTIONS:

AOUT: The output of the A power amplifier.

BCS: Connect this pin to one side of the current sense resistor that monitors the Boost inductor. Connect the other side of the current sense resistor to PGND.

BOUT: The output of the B power amplifier.

BRAKE: Open-drain output pulled low after the brake delay-time elapses.

BSW: Connect this pin to one terminal of the Boost inductor and the anode of the Boost rectifier. Connect the other terminal of the Boost inductor to +12V.

BYPASSC: This pin is connected to an internally generated bias supply which is used for precision analog functions. Connect this pin to an 0.1µF ceramic capacitor. Connect the other side of the capacitor to SGND. Do not connect this pin to any other circuitry.

C+, C-: Inputs to the Current-Sense Instrumentation Amplifier. The C- input is specially built to allow operation with input voltage as low as -2V.

COMP: The external current loop compensation components RC and CC go between this pin and AOUT.

COUT: Output of the Current-Sense Instrumentation Amplifier.

BRAKERC: The time between when a fault initiates PARK and when BRAKE is asserted is set by the resistor and capacitor on BRAKERC. Select $10k \leq RDB \leq 1Meg$.

DOUT: The output of the 11-bit DAC. For optimum slew rate and settling time, minimize the load capacitance on DOUT.

I1: First inverting input of the A power amplifier. When activated by the range bit of the data latch, an output current proportional to the DAC output multiplied by RD1/RI1 is commanded.

I2: Second inverting input of the A power amplifier. When activated by the range bit of the data latch, an output current proportional to the DAC output multiplied by RD2/RI2 is commanded.

PARK: RPI and RPF connect to this pin to set the fault park voltage across the load.

POR: Open-drain output from the POR monostable. POR is pulled low when the IC is first powered up, and remains low until the end of the PORRC cycle. POR also pulls low in a fault and stays low until the fault is cleared and the timer cycles.

PORRC: The time delay of the POR monostable is set by the capacitor and resistor from PORRC to ground, CDP and RDP. Select $10k \leq RDP \leq 1Meg$.

PGND: This ground is used for the power amplifiers and for some digital circuitry.

REF: The 2.5V precision reference of the data converter is connected to REF through a current limiting resistor. The current limiting resistor is not tightly controlled and has a strong change with temperature. Keep REF load current under 10µA and REF load capacitance under 200pF.

R/W: The data registers in the UCC3275 will accept data from the serial bus when R/W is high and will write data onto the bus when R/W is low.

SCLK: Data is clocked into the DAC on rising edges of SCLK after SLOD goes low. After 16 rising edges of SCLK, the data accepted is latched into the output register and the DAC is updated.

SGND: This ground pin is used for critical signals. Connect SGND to PGND in only one place, at the source of input current.

SLOD: SLOD is the digital chip-select input to the UCC3275. SLOD going low selects the IC and enables clocking of data from SDIO.

SDIO: After SLOD goes low, data is clocked into the DAC from the SDIO input on the rising edges of SCLK.

TRISTATE: To facilitate testing, outputs from this IC can be opened by pulling TRISTATE high. TRISTATE is internally pulled low so in normal operation, TRISTATE can be disconnected.

V5: This 5V supply input is used for all digital circuits on the UCC3275 and for some analog circuits. Bypass this supply to PGND.

UV12: Input to the UV12 comparator. Voltage divider RA12 and RB12 set the trip point of the UV12 comparator.

UV5: Input to the UV5 comparator. Voltage divider RA5 and RB5 set the trip point of the UV5 comparator.

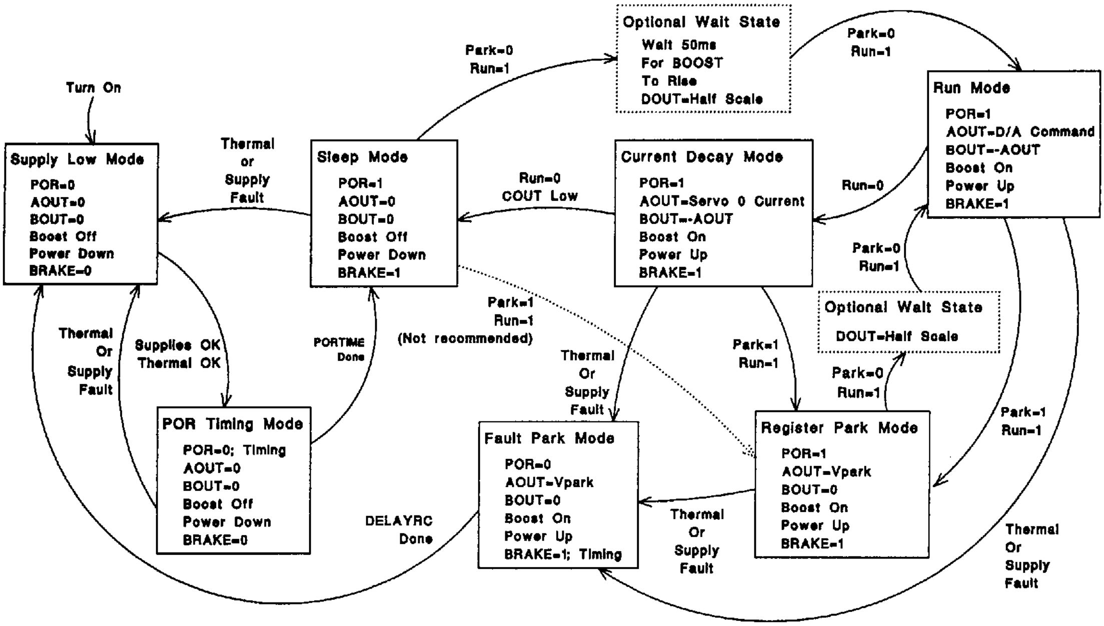
V+, V-: Inputs to the Voltage-Sense Instrumentation Amplifier. The V+ input is specially built to allow operation with input voltage as low as -2V.

VBST: This is the output of the Boost converter. Connect a filter capacitor from VBST to PGND. That capacitor supplies power during fault park modes. Also connect VBST to the cathode of the boost rectifier.

VL: VL supplies power to the analog control functions on the IC and to the VCM output stage. VL should be connected to a +12V supply through an isolation diode and should also be pulled up with energy recovered from the spindle motor during park. Bypass VL directly to PGND.

VOUT: Output of the Voltage-Sense Instrumentation Amplifier.

MODES OF OPERATION



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RUN MODE

In the RUN mode, all circuits (Power and Instrumentation Amplifiers, DAC, Boost, Park Logic, Power Management, and I/O Bus) are operational. Commands from the serial interface such as DAC output voltage and range are accepted and converted to load current commands by the power amplifiers.

If desired, the UCC3275 can implement head parking while in RUN mode under continuous control of the system processor. This manual parking function allows feedback control of load current and also allows estimation of the load velocity by sensing back EMF voltage across the load with the voltage sense amplifier.

SLEEP MODE

In SLEEP mode, all circuits are inhibited except for power monitoring circuits (under voltage comparators, power-on reset, and I/O bus). Both AOUT and BOUT are held to ground to dissipate any load current.

CURRENT DECAY MODE

It is essential to allow any load current to decay before entering sleep mode. When SLEEP is commanded from RUN mode, the UCC3275 enters CURRENT DECAY mode, and remains in this mode until the current sense amplifier detects current below a predetermined threshold. In this mode, the DAC output goes to 2.5V, causing the amplifiers to slew the load to zero current as quickly as possible.

SUPPLY LOW MODE

When power is first applied to the UCC3275, it immediately sequences into SUPPLY LOW mode and sets the data register to not-PARK and not-RUN. In this mode, POR is asserted low and BRAKE is asserted low. Also, in this mode, supply current is minimized by turning off all amplifiers and turning off the boost converter. In this mode, both AOUT and BOUT will be held at ground. The UCC3275 will remain in this mode until both power supplies ramp up to predetermined acceptable supply threshold voltages.

MODES OF OPERATION (continued)

POR TIMING MODE

During SUPPLY LOW mode, POR and BRAKE are asserted low. This puts the system processor into a predetermined starting state and holds the spindle fixed. When all supply and temperature faults are cleared, the UCC3275 will sequence to SLEEP mode through POR TIMING mode.

In POR TIMING mode, the UCC3275 continues to assert POR and BRAKE low, and waits for the PORRC network to complete a cycle. After the PORRC has elapsed, the UCC3275 sequences into SLEEP mode, releasing POR and releasing BRAKE.

FAULT PARK MODE

In the event of a fault, such as supply dropout or overtemperature, the UCC3275 will sequence to SUPPLY LOW mode and remain there until the fault clears. If the fault occurred during RUN mode or REGISTER PARK mode, the UCC3275 will sequence through FAULT PARK mode before entering SUPPLY LOW mode. This intermediary mode parks the heads of the disk drive and decreases load current to a safe enough level.

FAULT PARK mode causes the heads to park by applying a predetermined voltage across the load. This voltage consists of the output of the A amplifier, AOUT, minus the output of the B amplifier, BOUT. In fault park mode, BOUT is regulated to zero volts. AOUT immediately goes to the following voltage:

$$AOUT = 0.5V \bullet \frac{RPF+RPI}{RPI}$$

With AOUT at a fixed voltage and BOUT at 0V, load current will exponentially slew to a steady-state value determined by load resistance and load voltage.

When the UCC3275 enters FAULT PARK mode, the BRAKERC timer will start timing. At the end of the BRAKERC time, the heads will certainly be parked and the load current will decay to the steady-state park current. At this time, the current is very close to steady-state value, so is low enough to allow the UCC3275 to enter SUPPLY LOW mode.

It is not possible to go from FAULT PARK mode to RUN mode without sequencing through supply low mode, POR TIMING mode, and SLEEP mode. This sequence of modes forces the UCC3275 through predictable operating conditions and assures that faults are adequately addressed.

REGISTER PARK MODE

The UCC3275 can command head parking under serial interface control. If the serial interface commands head parking, the UCC3275 will immediately enter REGISTER PARK mode. In this mode, the load voltage is commanded to the same fixed voltages as in FAULT PARK mode.

REGISTER PARK mode differs from FAULT PARK mode in that it is a stable state which will not time out. BRAKERC is not timing during REGISTER PARK mode. Also, it is possible and practical to go from REGISTER PARK mode to RUN mode, where it is not possible to immediately go from FAULT PARK mode to RUN mode.

OPTIONAL WAIT STATES

In SLEEP mode, the boost converter is off, and the boost supply is lower than the running boost voltage. Sequencing from SLEEP mode to RUN mode, there will be a time during which the boost supply voltage will be below normal regulated level. During this time, if the power amplifier outputs attempt to command load current, load voltage may not reach full supply voltage and load current may not ramp up to desired current at the expected rate. This might have undesirable effects on the servo loop response.

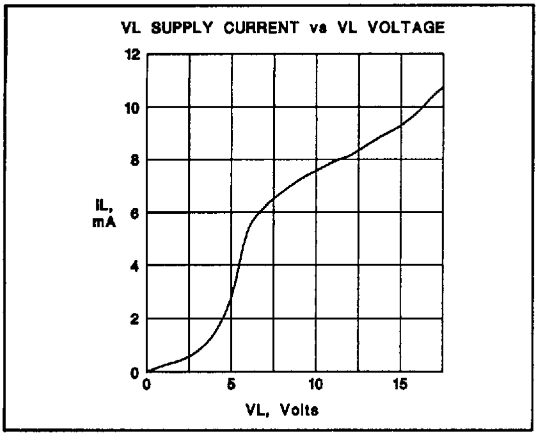
To avoid loop problems such as overshoot and unexpected current rise delay, the system processor should command zero load current when first sequencing from SLEEP mode to RUN mode.

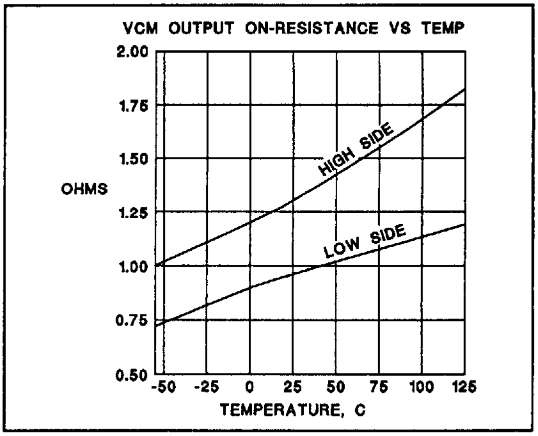
This mode which resembles RUN mode but also has DOUT at half scale is called an "optional wait state". For smoothest operation, remain in this optional wait state for 50ms before commanding a normal load current. After a delay time of 50ms, the boost will be up to running level, so commands will be effectively implemented by the power amplifiers.

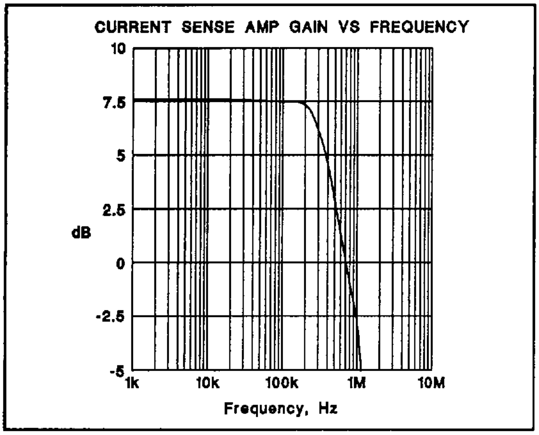
A similar optional wait state is recommended between REGISTER PARK mode and RUN mode. However, as the boost is running during REGISTER PARK mode, it is not necessary or useful to wait in this optional wait state longer than 1ms.

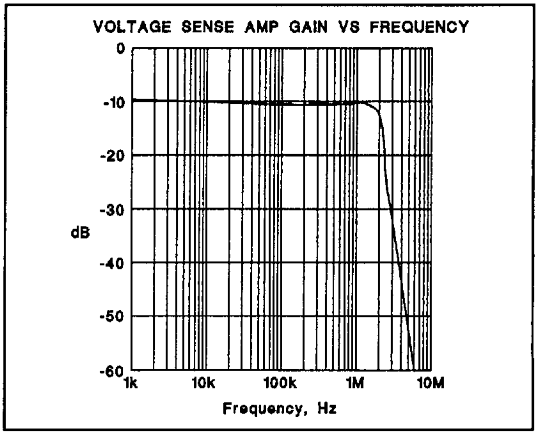
Should it be necessary to get immediate load current, these optional wait states can be bypassed. However, the performance of the servo system might be degraded for a short time while the boost rises and the system stabilizes.

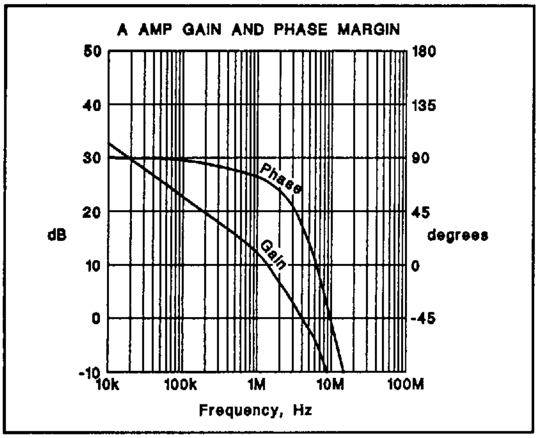
TYPICAL CHARACTERISTICS

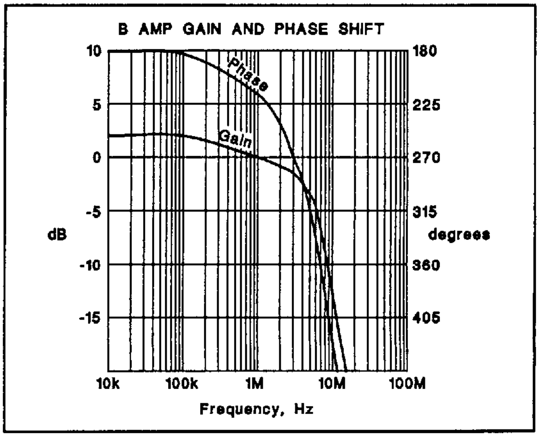

VL SUPPLY CURRENT vs VL VOLTAGE


VCM OUTPUT ON-RESISTANCE VS TEMP


CURRENT SENSE AMP GAIN VS FREQUENCY


VOLTAGE SENSE AMP GAIN VS FREQUENCY


A AMP GAIN AND PHASE MARGIN


B AMP GAIN AND PHASE SHIFT

INTERNAL TIMERS

The UCC3275 contains two independent timers, the *power-on reset* timer and the *brake delay* timer. Although controlled by different signals, the two timers are electrically identical.

POWER-ON RESET TIMER

The *power-on reset* timer is a one-shot multivibrator circuit. The timer has one control pin PORRC, and one output pin POR. When the UCC3275 is initially turned on, POR is pulled low. POR will remain low until both power-supply comparator inputs UV5 and UV12 receive valid signals, indicating that both supplies are high enough for the UCC3275 to operate dependably. POR will also stay low if the UCC3275 internal temperature is greater than the thermal shutdown temperature.

If both power-supply comparator inputs and the thermal shutdown circuit show that the UCC3275 is in its normal operating regions, then the *power-on reset* timer will start timing, but POR will still stay low. After the *power-on reset* timer completes timing, POR will become high impedance.

The *power-on reset* time is set by the value of the resistor and capacitor connected from PORRC to ground. It is suggested that the resistor be 100k ohms and that the capacitor value be selected for the appropriate time from the following equation:

$$T_{POR} = R_{DP} \bullet C_{DP}$$

When the *power-on reset* timer is not timing, PORRC is held at approximately 6.9V. During timing, PORRC will decay from approximately 6.9V down to approximately 4.36V.

BRAKE-DELAY TIMER

The *brake delay* timer is also a one-shot multivibrator circuit. This timer has one control pin BRAKERC, and one output pin BRAKE.

When the UCC3275 is initially turned on, the part enters Supply-Low mode. In this mode, BRAKE is pulled low. Similarly, during POR timing mode, BRAKE is still held low. BRAKE is released to high-impedance when the UCC3275 enters Sleep mode, and remains high-impedance during Run mode, Current Decay mode, and Register Park mode.

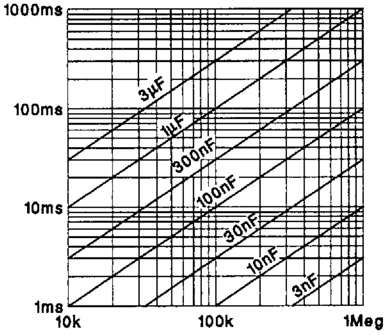
In the event of a fault, such as reaching thermal shutdown temperature or a supply dropping below the supply-comparator threshold, the UCC3275 will enter Fault Park mode. When entering Fault Park mode, the *brake delay* timer will start timing. The UCC3275 will remain in Fault Park mode while the *brake delay* timer is timing, and will go to Supply Low mode after the time elapses. During Fault Park mode, BRAKE will remain high impedance. BRAKE will pull low when the UCC3275 enters Supply Low mode.

The *brake delay* time is set by the value of the resistor and capacitor connected from BRAKERC to ground. It is suggested that the resistor be 100k ohms and that the capacitor value be selected for the appropriate time from the following equation:

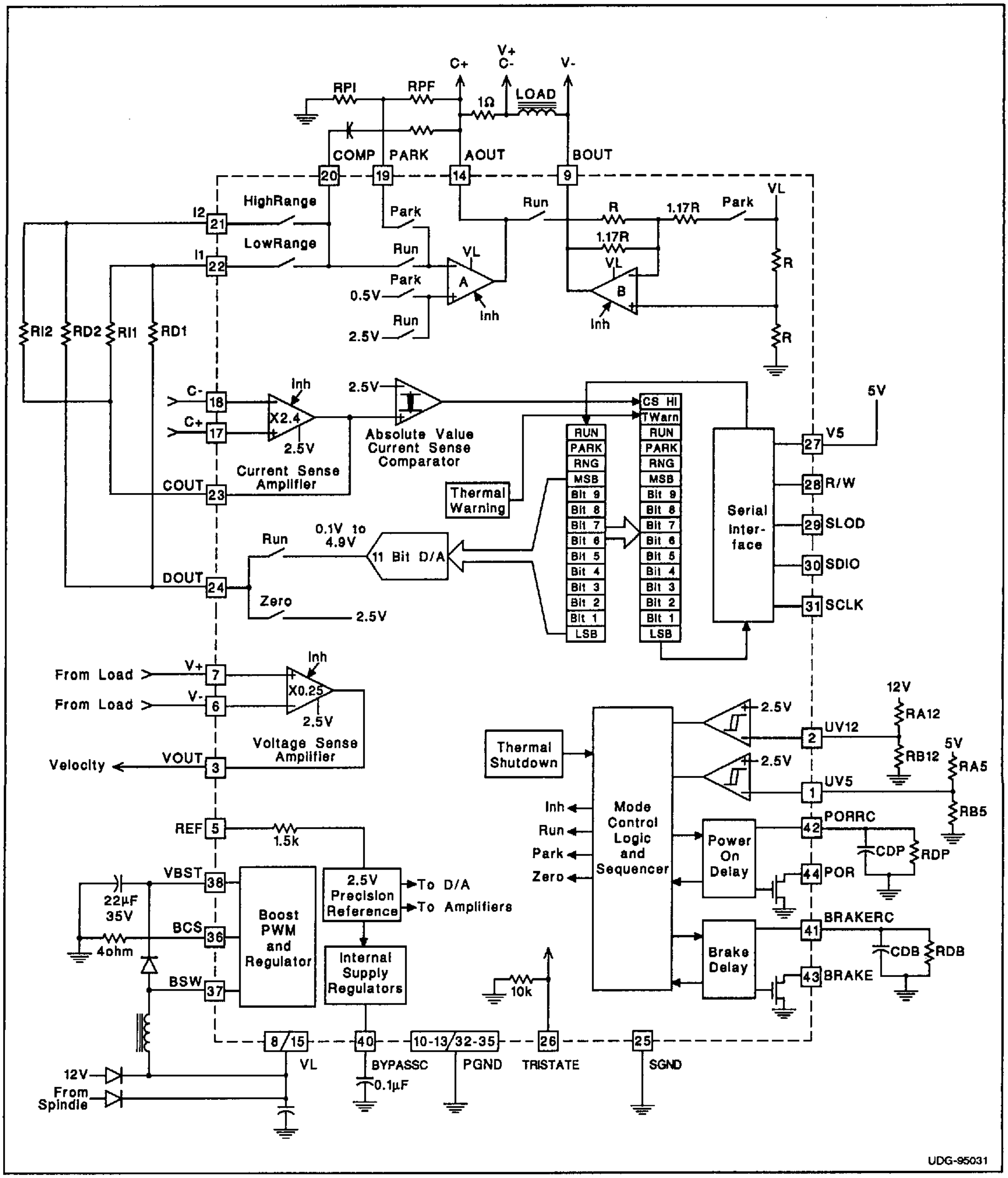
$$T_{BRAKEDELAY} = R_{DB} \bullet C_{DB}$$

When the *brake delay* timer is not timing, BRAKERC is held at approximately 6.9V. During timing, BRAKERC will decay from approximately 6.9V down to approximately 4.36V.

TIMER PERIOD VS RD AND CD

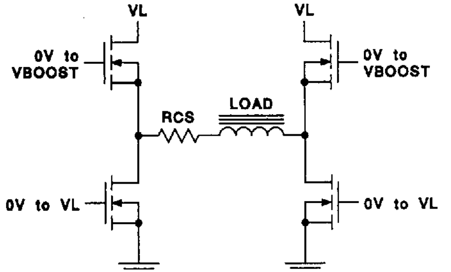


TYPICAL APPLICATION



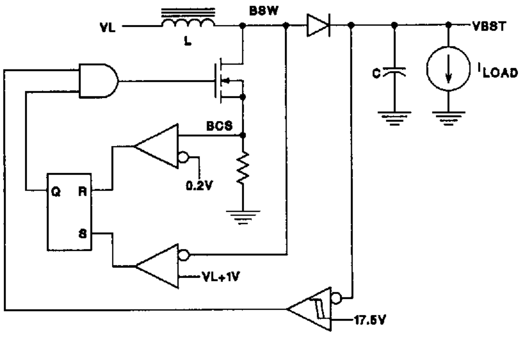
BOOST CIRCUIT DESCRIPTION

The power output stage of the UCC3275 uses N-channel power MOSFETs for both the high side and the low side drive transistors. The low side power MOSFET operates as a common source amplifier, while the high side power MOSFET operates as a source follower.

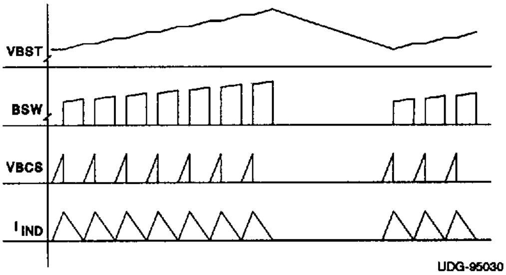


To achieve output swing close to the positive power supply (VL), the gate of the high side power MOSFET must exceed VL by at least 4 volts. The UCC3275 contains a boost PWM regulator to generate a higher voltage power supply for this function.

The boost PWM regulator in the UCC3275 operates as a variable frequency switching regulator with fixed peak current, zero valley current, and hysteresis to regulate voltage. This PWM is much more efficient than a charge pump, and requires few external components.



When the voltage on the output of the boost regulator (VBST) is less than the desired 17.5V, the switching circuit will operate continuously at a nearly constant duty cycle. This switching will raise the boost output voltage to 17.5V. When the output reaches 17.5V, the boost will shut down and allow the VBST to droop down to 17.25V before more switching cycles begin.



The frequency of these bursts of switching is set by the size of the boost reservoir capacitor, the boost load current, the boost voltage hysteresis and the boost transfer rate. The boost voltage decay time is:

$$T_D = C\frac{\Delta V_{VBST}}{I_{LOAD}}$$

In a typical system, C=22μF, ILOAD=5mA, and ΔV=250mV, so TD will be 1.1ms.

The boost charge time is:

$$T_C = C\frac{\Delta V_{VBST}}{I_{BOOST}\bullet\frac{VL}{VBST} - I_{LOAD}}$$

In the same system, IBOOST=IPEAK/2=25mA, VBST=17.5V, and VL=11.4V, so TC will be 0.49ms. This gives a burst duty cycle of 31% and a burst frequency of 630Hz.

The boosting sequence operates at a much higher frequency and is governed by different equations. When the boost voltage is lower than the regulation point, the PWM switches from *inductor charge* mode to *inductor discharge into load* mode. *Inductor charge* mode occurs with VL applied to the inductor, and the inductor current ramping from zero to IPEAK:

$$T_{IC} = L\frac{I_{PEAK}}{VL}$$

In our above system, L=100μH, VL=11.4V, and IPEAK=50mA, so TIC will be 0.44μs.

During *inductor discharge into load* mode, the inductor discharges at a rate determined by the voltage across the inductor VBST - VL, so:

$$T_{ID} = L\frac{I_{PEAK}}{VBST - VL}$$

With VL=11.4V, VBST=17.5V, L=100μH, and IPEAK=50mA, TID will be 0.82μs. Combined with the previous calculation which showed a TIC of 0.44μs, the boost frequency is 800kHz.

TESTABILITY AND SELF-TEST

Each UCC3275 is rigorously tested at the factory to assure that all functions and parameters perform according to specification. In most cases, the electrical characteristics of the part have been measured in a circuit similar to an actual application. Some electrical stress characteristics have been tested using pulse loads or other tests which assure performance without exposing the product to abusive thermal cycling.

In addition to exhaustive factory testing, the UCC3275 contains two different circuit blocks to aid users in production test and debug of finished systems: CURRENT COMPARATOR and TRI STATE.

CURRENT COMPARATOR

When the UCC3275 is connected in a typical system, load current can be commanded from the serial interface. Load current is sensed by a resistor in series with the load and amplified by the current sense amplifier. The output of the current sense amplifier drives the current sense comparator, which in turn drives a serial interface register bit.

If the UCC3275 and associated circuitry are operating normally, then the load current can be accurately commanded from the serial interface, and the load current can be accurately monitored by the current sense comparator and the serial interface register bit.

The following procedure can be implemented in system test software to confirm that the UCC3275 and associated circuitry is operating correctly.

1. Apply power to the system.
2. Wait for POR timing to complete.
3. Command PARK = 0 and RUN = 1 from the serial interface.
4. Wait 50ms for the boost to stabilize.
5. Command "LOW RANGE", serial interface code 00000000000 (hex 000).
6. Wait 5ms for the load current to stabilize.
7. Read the SERIAL INTERFACE OUTPUT register. The **CS HIGH** bit should be **low**, indicating that the load has very little current in it.
8. Command "LOW RANGE", serial interface code 00001000000 (hex 040).
9. Wait 5ms for the load current to stabilize.
10. Read the SERIAL INTERFACE OUTPUT register. The **CS HIGH** bit should be **high**, indicating that the load has significant positive current in it.
11. Command "LOW RANGE", serial interface code 11111000000 (hex 7C0).
12. Wait 5ms for the load current to stabilize.
13. Read the SERIAL INTERFACE OUTPUT register. The **CS HIGH** bit should be **high**, indicating that the load has significant negative current in it.

If the SERIAL INTERFACE OUTPUT register CS HIGH bit is not correct at any of these three reads, then the system is malfunctioning.

TRI STATE

If the UCC3275 system has been tested as described above and fails one or more of the register reads, then the TRI STATE function can help a production system locate the board problem.

With a bad board or subsystem, the defective component can be identified easiest if various parts of the board are disconnected from each other. The TRI STATE function is a logic input which physically disconnects most internal circuitry from bonding pads, allowing individual components to be tested with guided probes and bed-of-nails testers.

To assert TRI STATE, pull the TRI STATE input high.

The following terminals are **not** opened by asserting TRI STATE:

AOUT
BCS
BOUT
BSW
COUT
PGND
SIGGND
VBST
VL
VOUT