

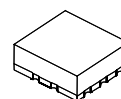
2.1GHz Band LNA GaAs MMIC

■GENERAL DESCRIPTION

NJG1116HB3 is a LNA IC designed for 2.1GHz band W-CDMA cellular phone. This IC has the function which passes LNA, and high gain mode or low gain mode can be chosen.

An ultra small and ultra thin package of USB8 is adopted.

■PACKAGE OUTLINE



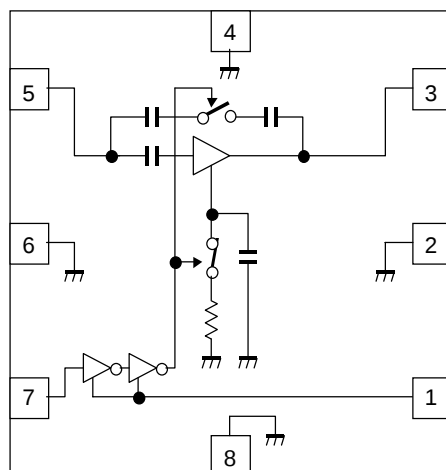
NJG1116HB3

■FEATURES

- | | | |
|-------------------------------------|--|---|
| ●Low voltage operation | +2.7V typ | |
| ●Low current consumption | 2.0mA typ. | @V _{CTL} =2.7V |
| | 2uA typ. | @V _{CTL} =0V |
| ●High gain | 14.7dB typ. | @V _{CTL} =2.7V, f _{RF} =2140MHz |
| ●Low noise figure | 1.6dB typ. | @V _{CTL} =2.7V, f _{RF} =2140MHz |
| ●Pout at 1dB Gain Compression point | -13.0dBm typ. | @V _{CTL} =2.7V, f _{RF} =2140MHz |
| | +11.0dBm typ. | @V _{CTL} =0V, f _{RF} =2140MHz |
| ●High input IP3 | -3dBm typ. | @V _{CTL} =2.7V, f _{RF} =2140MHz |
| | +3dBm typ. | @V _{CTL} =0V, f _{RF} =2140MHz |
| ●Small package | USB8-B3 (Package size: 1.5x1.5x0.75mm) | |

■PIN CONFIGURATION

HB3 Type
(Top View)



Pin Connection

1. V_{INV}
2. GND
3. RF OUT
4. GND
5. RF IN
6. GND
7. V_{CTL}
8. GND

Note: Specifications and description listed in this catalog are subject to change without prior notice.

NJG1116HB3

■ABSOLUTE MAXIMUM RATINGS

($T_a=+25^{\circ}\text{C}$, $Z_s=Z_i=50\Omega$)

PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
Operating voltage	V_{DD}		5.0	V
Inverter supply voltage	V_{INV}		5.0	V
Control voltage	V_{CTL}		5.0	V
Input power	P_{in}	$V_{DD}=2.7\text{V}$	+15	dBm
Power dissipation	P_D		135	mW
Operating temperature	T_{opr}		-40~+85	$^{\circ}\text{C}$
Storage temperature	T_{stg}		-55~+125	$^{\circ}\text{C}$

■ELECTRICAL CHARACTERISTICS 1 (DC)

($V_{DD}=V_{INV}=2.7\text{V}$, $T_a=+25^{\circ}\text{C}$, $Z_s=Z_i=50\Omega$)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating voltage	V_{DD}		2.5	2.7	4.5	V
Inverter supply voltage	V_{INV}		2.5	2.7	4.5	V
Control voltage (High)	$V_{CTL(H)}$		2.0	2.7	V_{INV}	V
Control voltage (Low)	$V_{CTL(L)}$		0	0	0.8	V
Operating current1	I_{DD1}	RF OFF, $V_{CTL}=2.7\text{V}$	-	2.0	2.7	MA
Operating current2	I_{DD2}	RFOFF, $V_{CTL}=0\text{V}$	-	2	30	UA
Inverter current1	I_{INV1}	RF OFF, $V_{CTL}=2.7\text{V}$	-	50	100	UA
Inverter current2	I_{INV2}	RF OFF, $V_{CTL}=0\text{V}$	-	110	200	UA
Control current	I_{CTL}	RF OFF, $V_{CTL}=2.7\text{V}$	-	20	50	UA

■ELECTRICAL CHARACTERISTICS 2 (LNA High Gain Mode)

($V_{DD}=V_{INV}=2.7V$, $V_{CTL}=2.7V$, $\text{freq}=2140\text{MHz}$, $T_a=+25^\circ\text{C}$, $Z_s=Z_l=50\Omega$, TEST CIRCUIT)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating frequency	freq		2110	2140	2170	MHz
Small signal gain1	Gain1		13.0	14.7	16.0	dB
Noise figure1	NF1		-	1.6	2.0	dB
Pin at 1dB gain compression point1	$P_{-1\text{dB(IN)1}}$		-16.0	-13.0	-	dBm
Input 3rd order intercept point	IIP3_1	$f_1=f_{RF}$, $f_2=f_{RF}+100\text{kHz}$, $P_{in}=-36\text{dBm}$	-6.0	-3.0	-	dBm
RF Input VSWR1	$VSWR_i$ 1		-	1.5	2.0	-
RF Output VSWR1	$VSWR_o$ 1		-	1.5	2.2	-

■ELECTRICAL CHARACTERISTICS 2 (LNA Low Gain Mode)

($V_{DD}=V_{INV}=2.7V$, $V_{CTL}=0V$, $\text{freq}=2140\text{MHz}$, $T_a=+25^\circ\text{C}$, $Z_s=Z_l=50\Omega$, TEST CIRCUIT)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating frequency	freq		2110	2140	2170	MHz
Small signal gain2	Gain2		-5.0	-4.0	-2.5	dB
Noise figure2	NF2		-	4.0	5.0	dB
Pin at 1dB gain compression point2	$P_{-1\text{dB(IN)2}}$		+8.0	+11.0	-	dBm
Input 3rd order intercept point2	IIP3_2	$F_1=f_{RF}$, $f_2=f_{RF}+100\text{kHz}$, $P_{in}=-36\text{dBm}$	0	+3.0	-	dBm
RF Input VSWR2	$VSWR_i$ 2		-	1.9	2.3	-
RF Output VSWR2	$VSWR_o$ 2		-	1.7	2.1	-

■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	VINV	Inverter voltage supplies terminal.
2	GND	Ground terminal. (0V)
3	RFOUT	RF output terminal. The RF signal is output through external matching circuit connected to this terminal. Please connected inductance L3 and power supply as shown in test circuit, since this terminal is also the terminal of LNA power supply.
4	GND	Ground terminal. (0V)
5	RFIN	RF input terminal. The RF signal is input through external matching circuit connected to this terminal. A DC blocking capacitor is not required.
6	GND	Ground terminal. (0V)
7	VCTL	Control voltage supply terminal. The High level voltage of this terminal controls LNA High Gain Mode. The Low level voltage of this terminal controls LNA Low Gain Mode.
8	GND	Ground terminal. (0V)

CAUTION

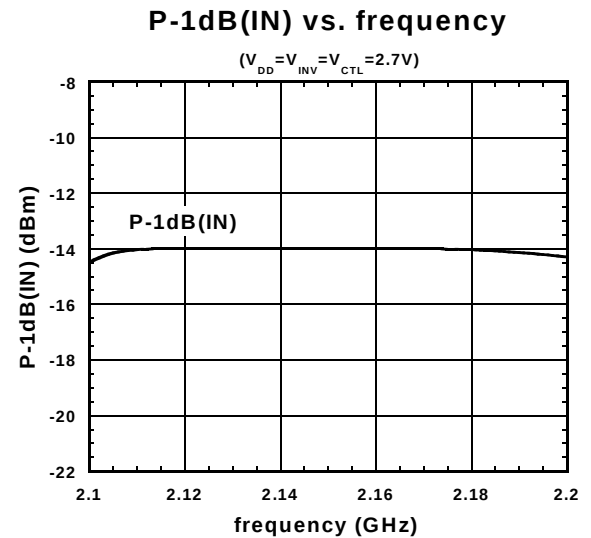
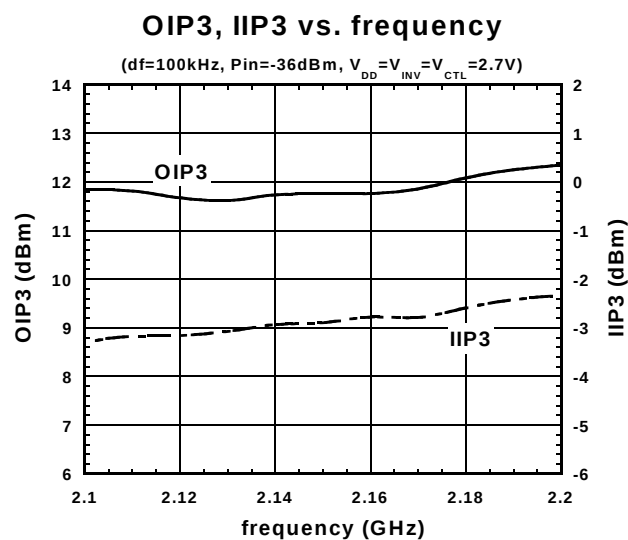
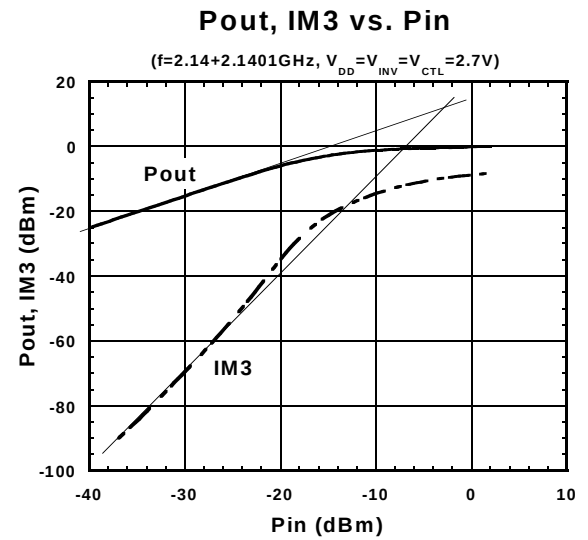
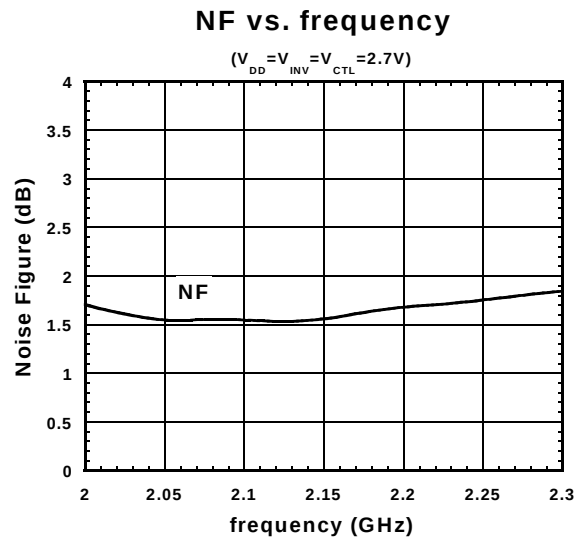
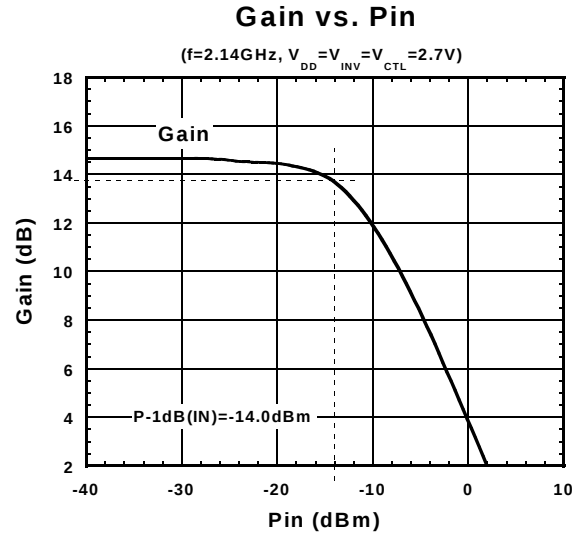
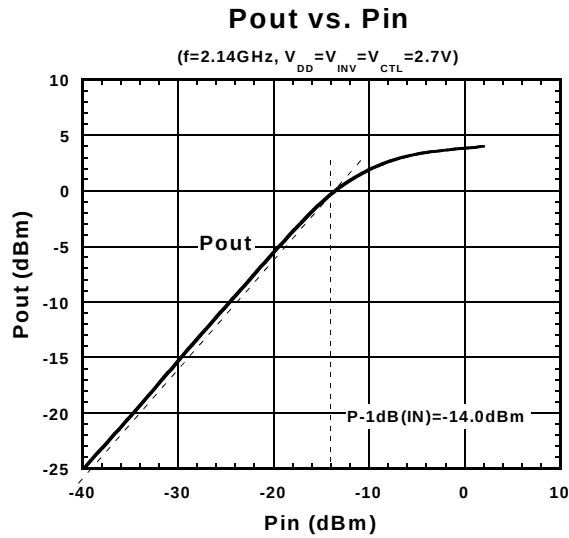
- 1) Ground terminal (No.2, 4, 6, 8) should be connected to the ground plane as low inductance as possible.

■ TRUTH TABLE

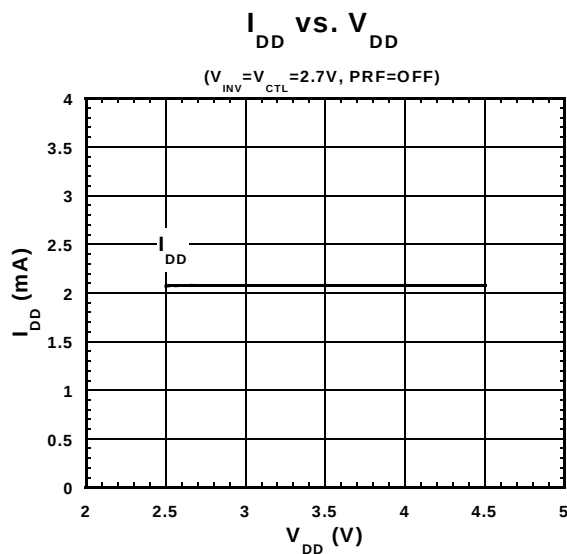
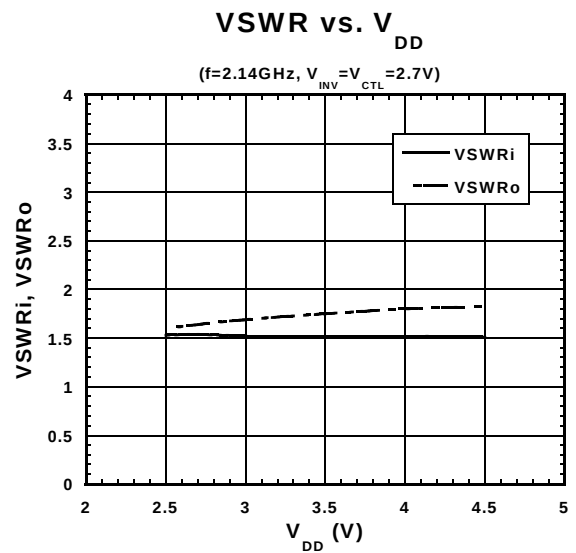
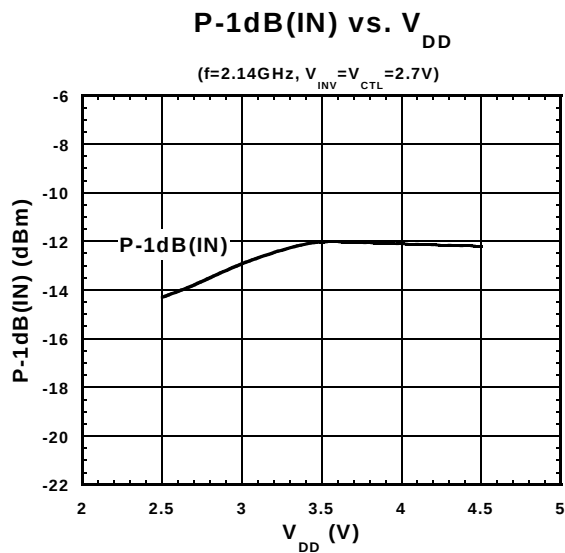
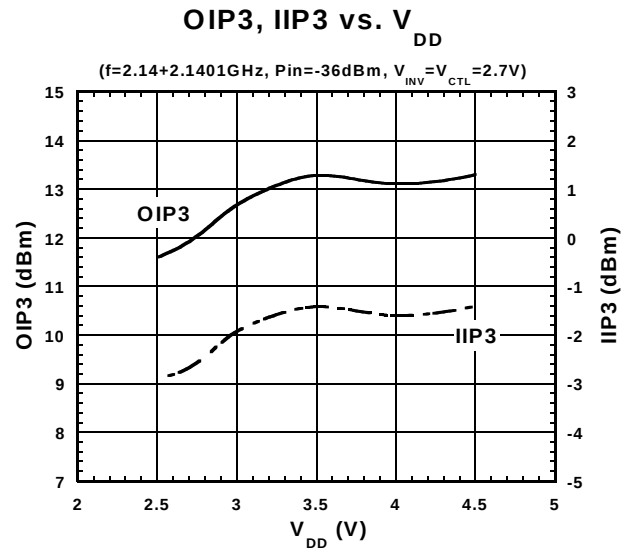
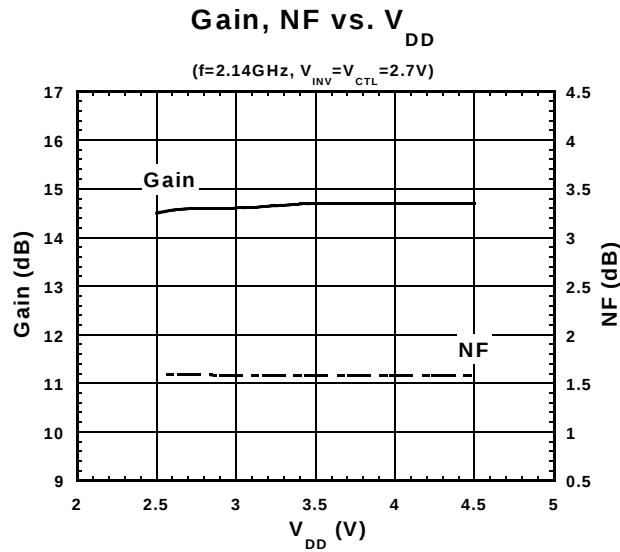
V _{CTL}	Operating Current	Bypass circuit	LNA Mode
L	OFF	ON	Low Gain Mode
H	ON	OFF	High Gain Mode

"H"=V_{CTL}(H), "L"=V_{CTL}(L)

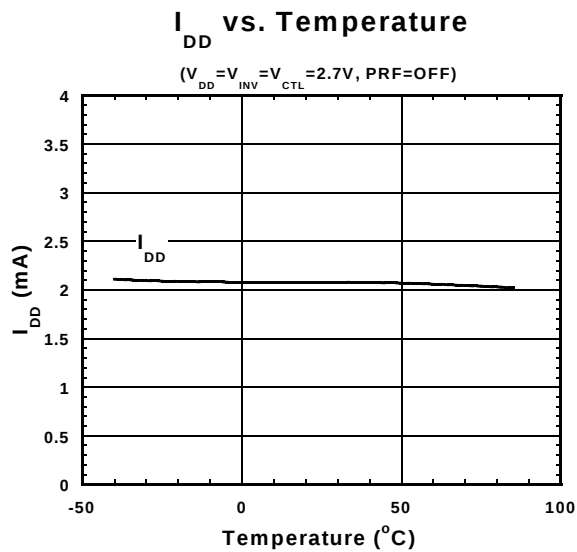
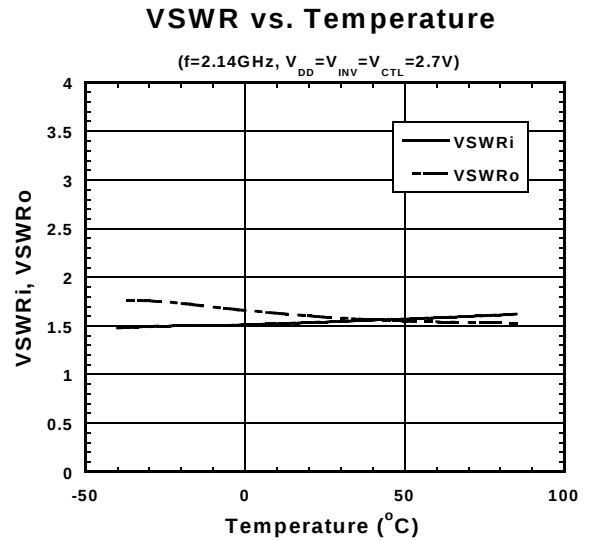
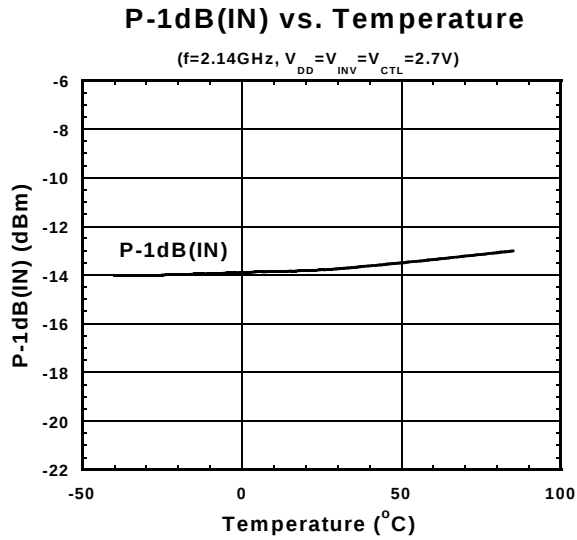
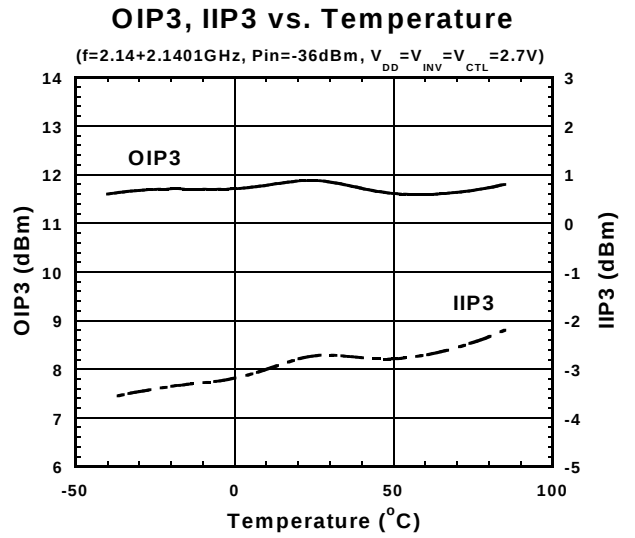
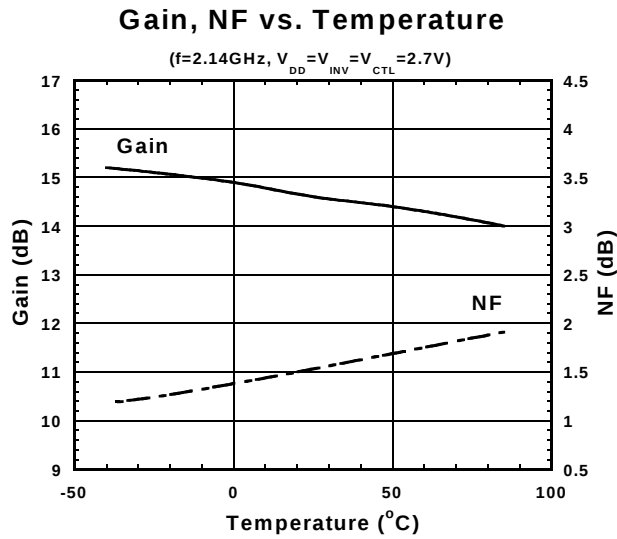
ELECTRICAL CHARACTERISTICS (LNA High Gain Mode)



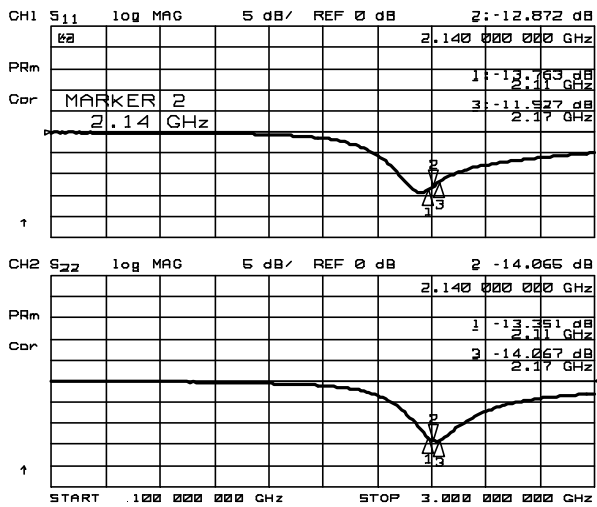
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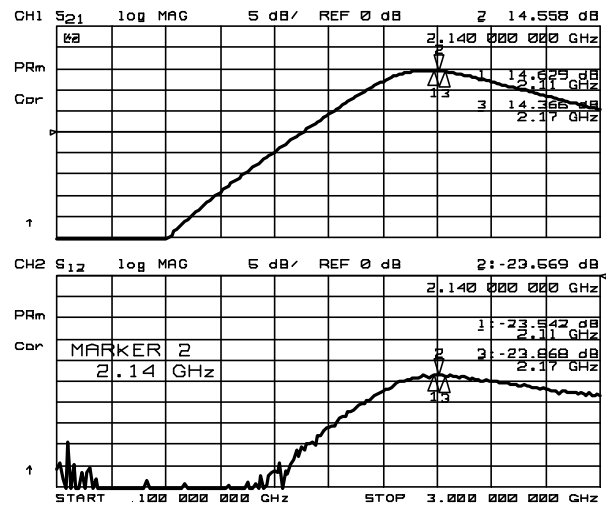
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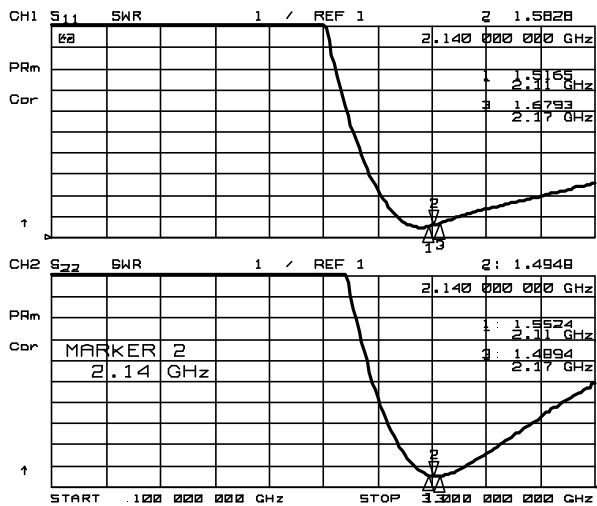
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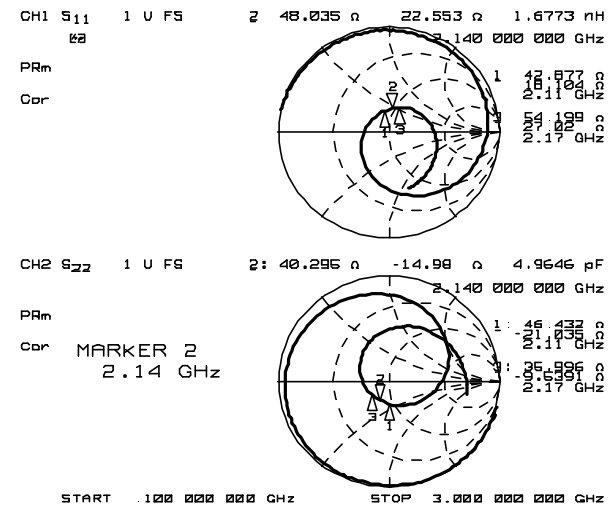
S11, S22



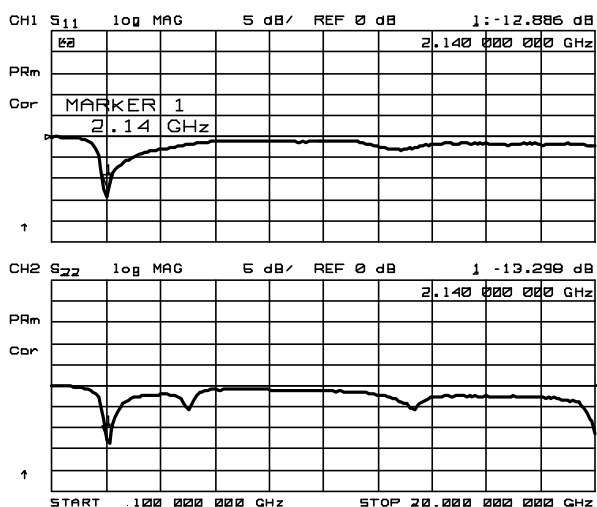
S21, S12



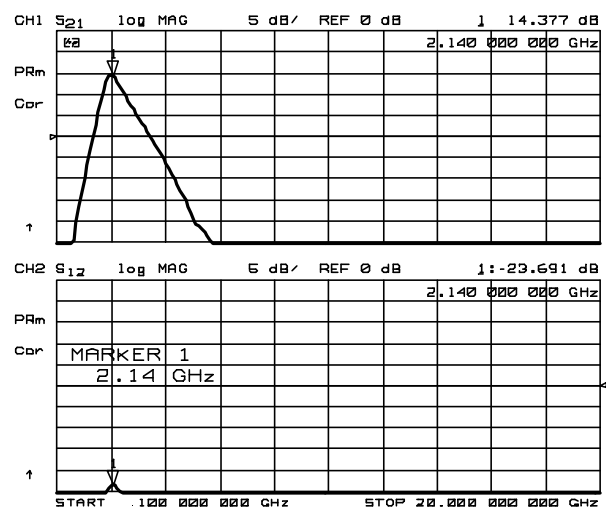
VSWR



Zin, Zout

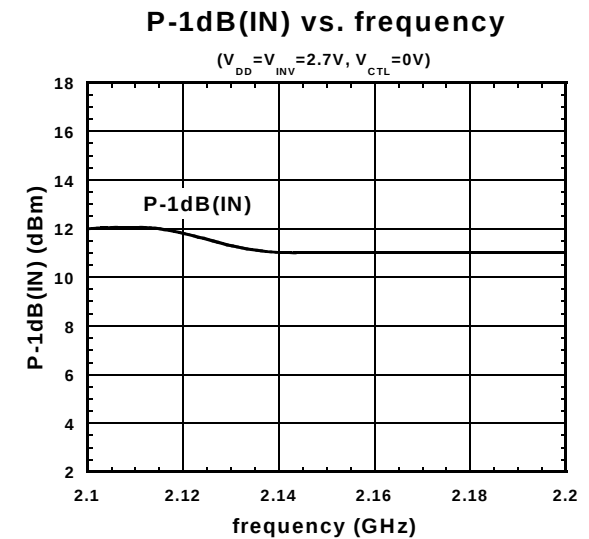
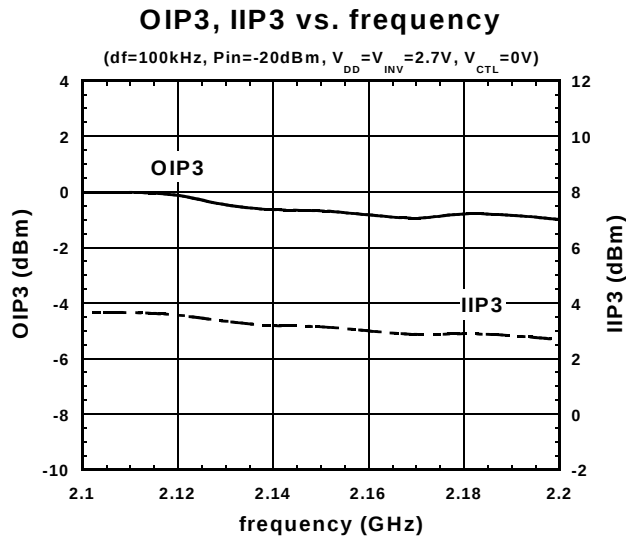
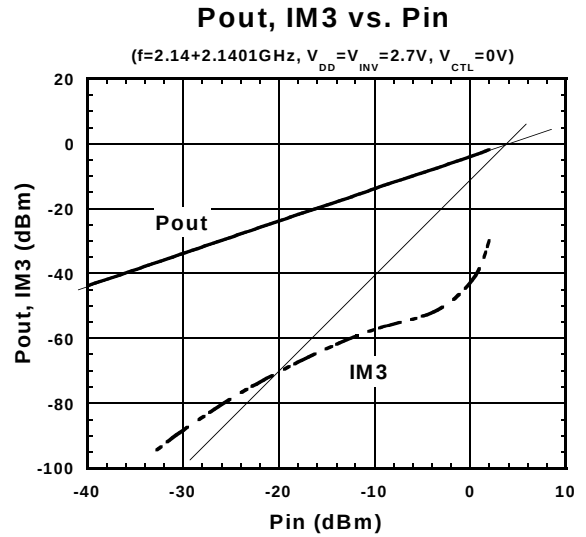
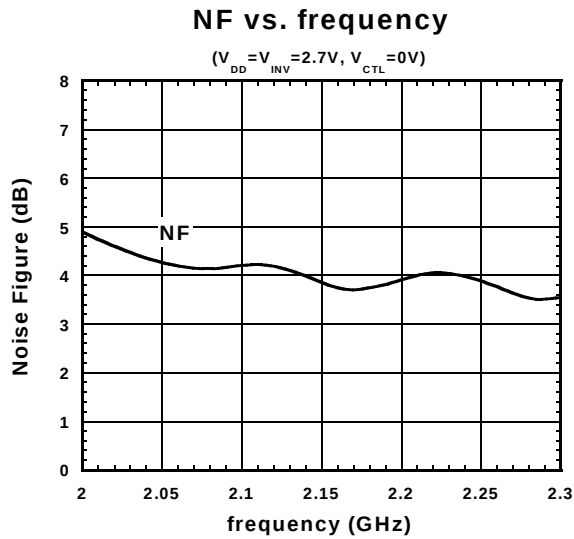
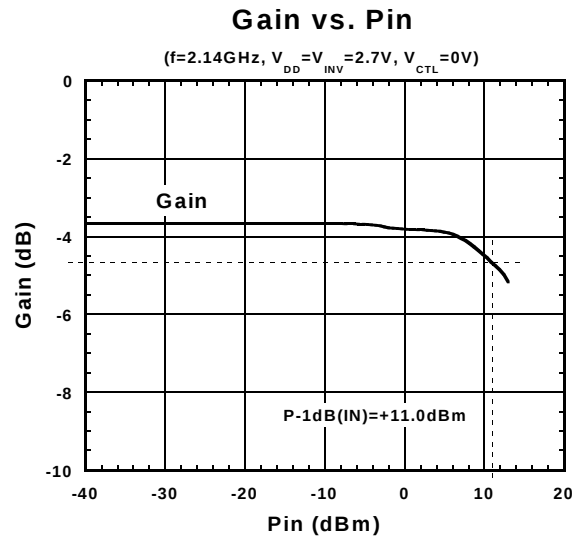
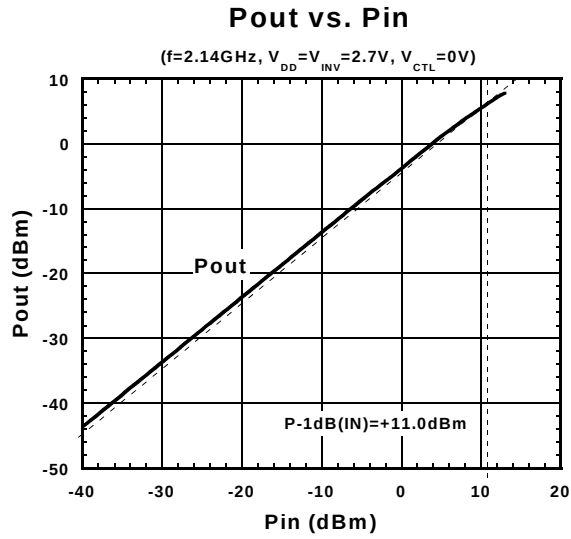


S11, S22 (100MHz~20GHz)



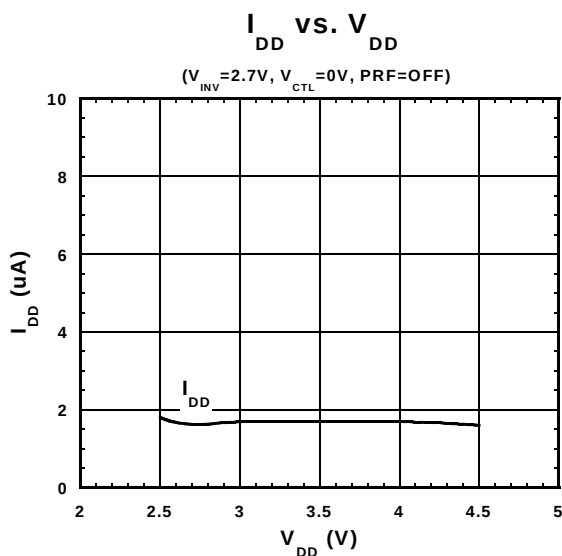
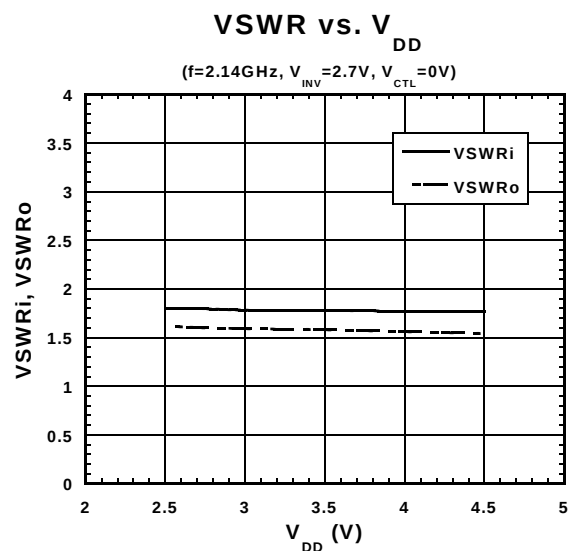
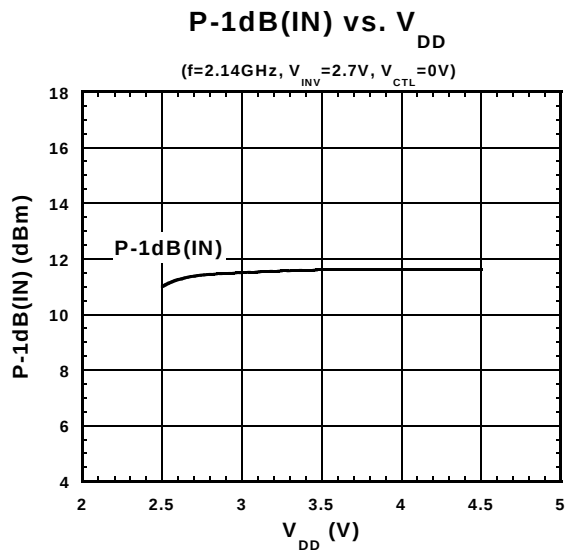
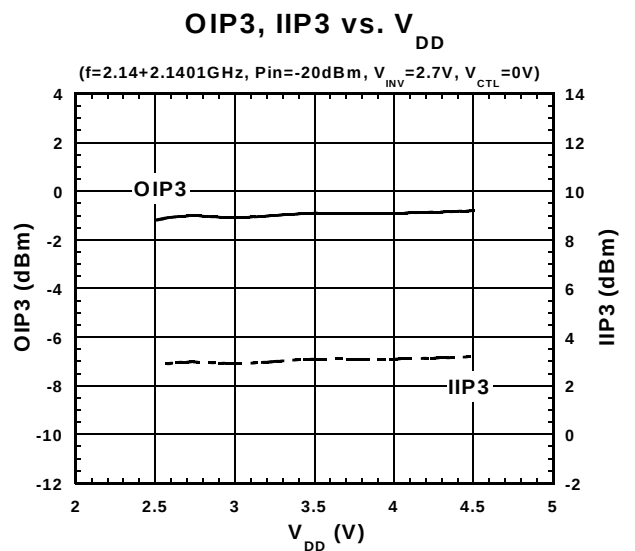
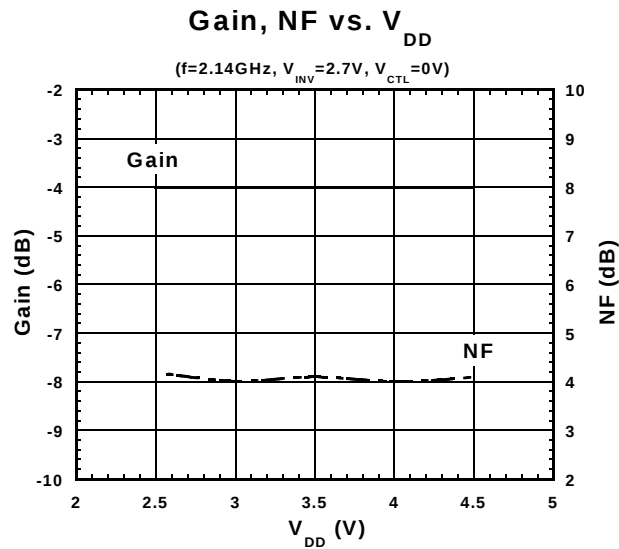
S21, S12 (100MHz~20GHz)

ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)

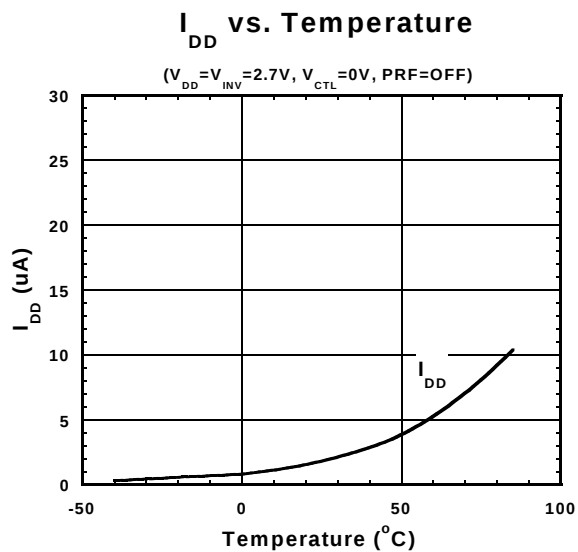
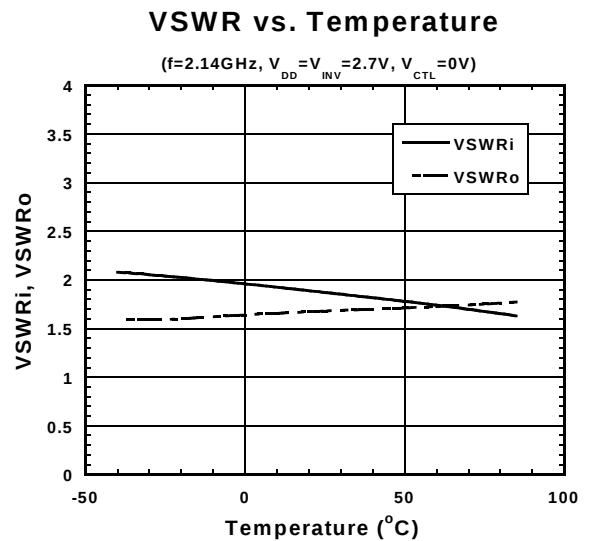
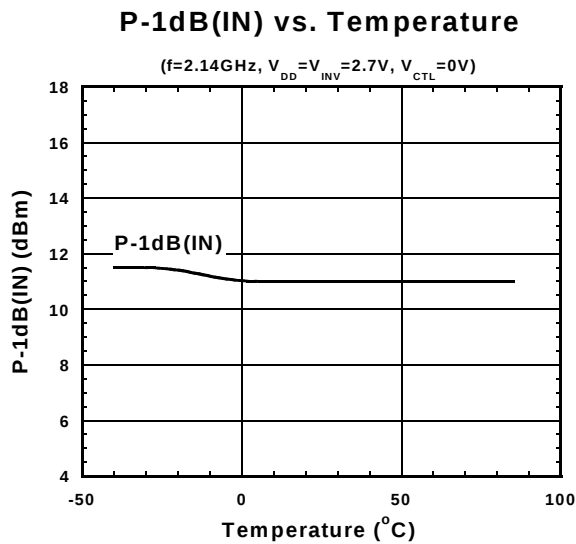
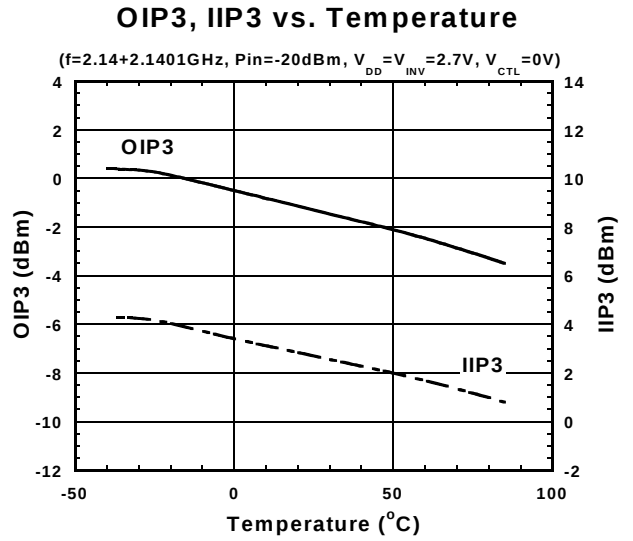
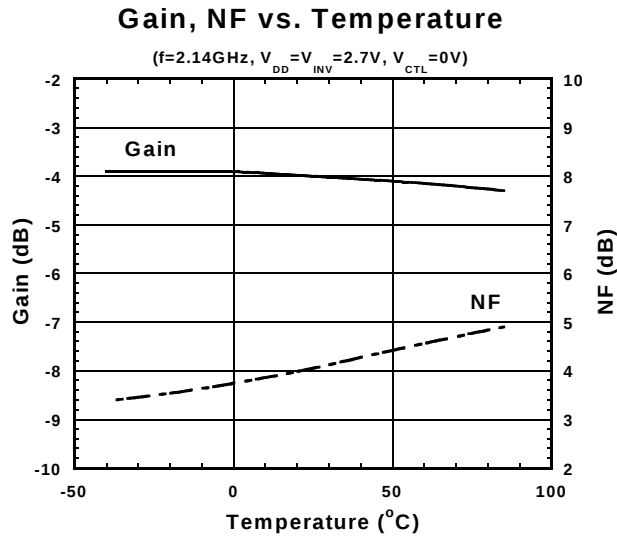


NJG1116HB3

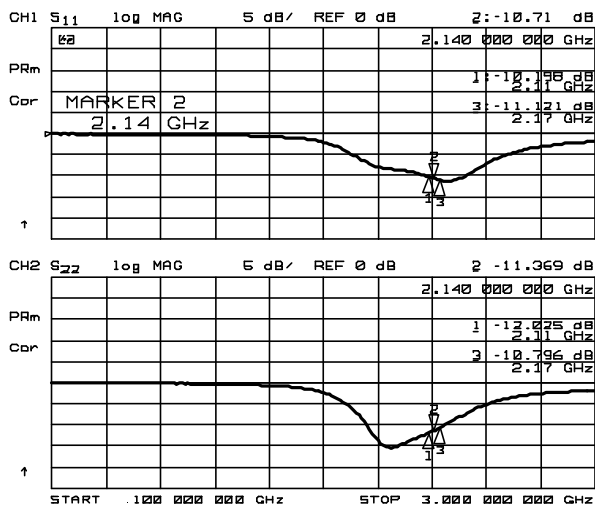
ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)



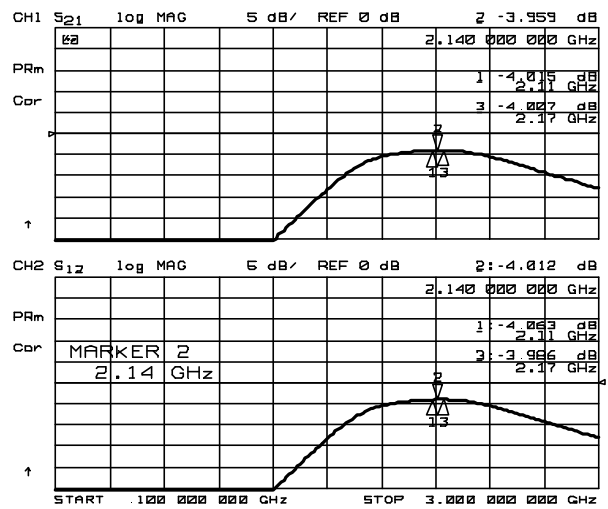
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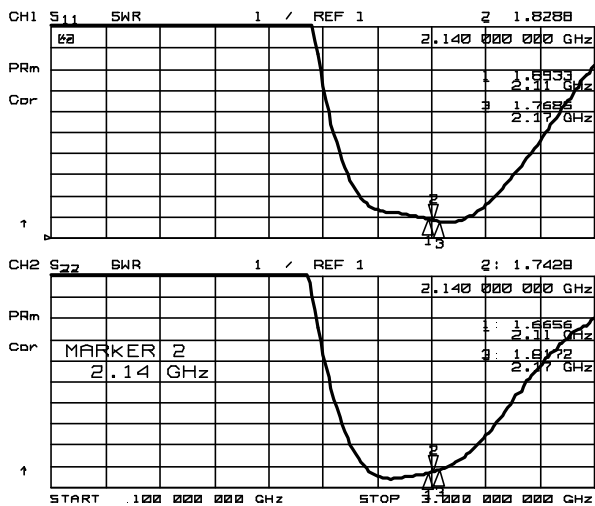
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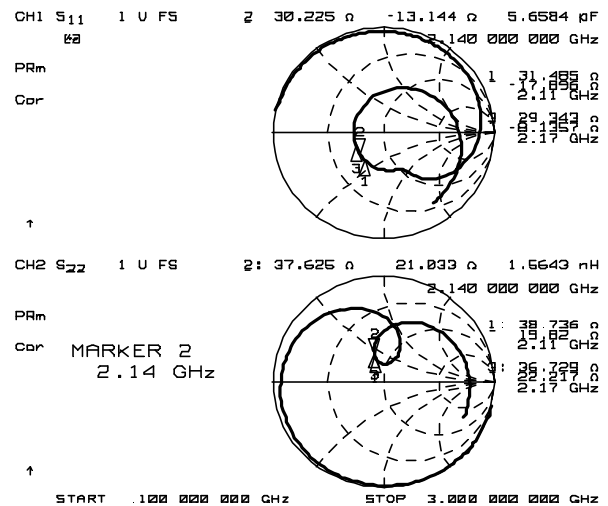
S11, S22



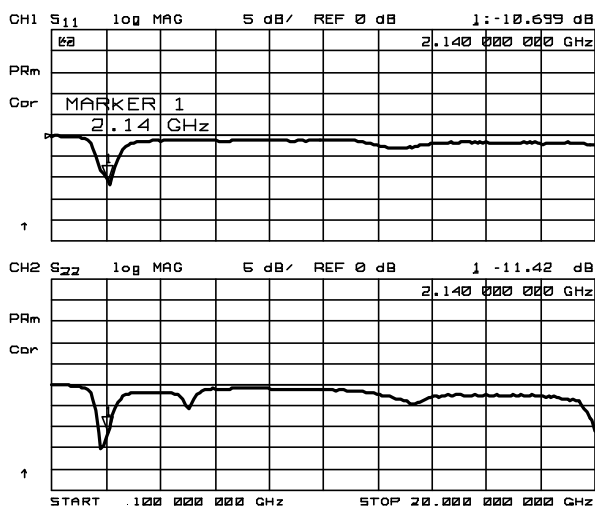
S21, S12



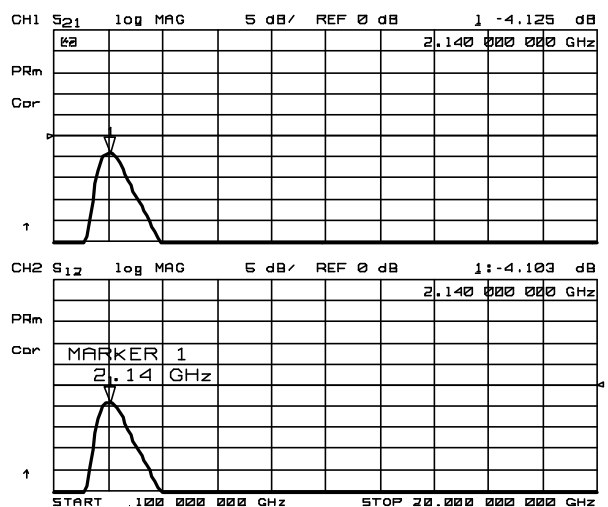
VSWR



Zin, Zout



S11, S22 (100MHz~20GHz)



S21, S12 (100MHz~20GHz)

The schematic diagram illustrates the internal architecture of a 1-bit programmable logic device (PLD). The device is represented as a central square block with eight pins, numbered 1 through 8, and a 1 Pin INDEX. The internal components include:

- Input Stage:** The RF IN pin (pin 5) is connected to an input buffer (pin 5) and a series inductor L2 (5.6nH). The input buffer is connected to a programmable logic element (pin 4) which is also connected to a series inductor L4 (8.2nH) and a series capacitor C1 (2pF).
- Output Stage:** The RF OUT pin (pin 3) is connected to an output buffer (pin 3) and a series inductor L3 (2.2nH). The output buffer is connected to a programmable logic element (pin 4) which is also connected to a series inductor L4 (8.2nH) and a series capacitor C1 (2pF).
- Control Logic:** The V_{CTL} pin (pin 7) is connected to a control logic block (pin 7) which is also connected to a series inductor L1 (3.9nH). The control logic block is connected to a programmable logic element (pin 4) which is also connected to a series inductor L4 (8.2nH) and a series capacitor C1 (2pF).
- Power and Ground:** The V_{DD}=2.7V pin (pin 2) is connected to a power supply (pin 2) and a series capacitor C2 (1000pF). The V_{INV}=2.7V pin (pin 1) is connected to an inverter (pin 1) and a series capacitor C2 (1000pF). The GND pin (pin 6) is connected to ground (pin 6).
- Internal Connections:** The internal connections between the pins and the programmable logic elements are shown as a network of lines and components, including a central programmable logic element (pin 4) and a series inductor L3 (2.2nH).

■RECOMMENDED PCB DESIGN

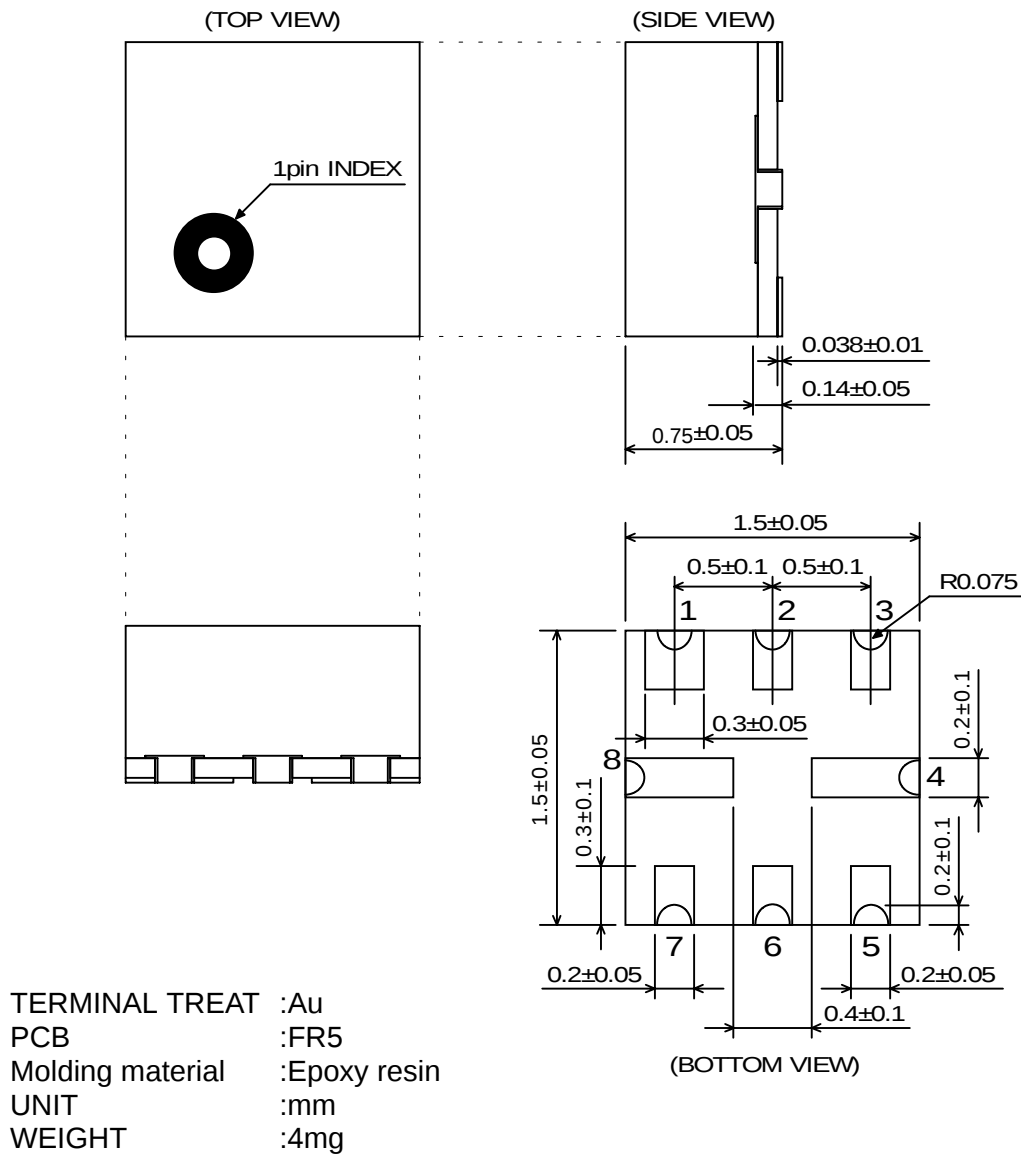
The micrograph shows the physical layout of the circuit board. The components are labeled as follows: V_{DD} (power supply), V_{CTL} (control voltage), V_{INV} (inverter voltage), $C1$, $C2$ (capacitors), $L1$, $L2$, $L3$, $L4$ (inductors), and $J0028$ (a specific component or test point). The RF input and output ports are labeled "RF IN" and "RF OUT". The layout includes a central area with a grid of small circles, likely representing a microstrip or a similar transmission line structure, and larger circular features that may be vias or pads.

Parts ID	Comment
L1, L3,	TAIYO-YUDEN (HK1005)
L2, L4	MATUSHITA (ELJRF)
C1, C2	MURATA (GRP15)

PCB (FR-4) :
t=0.2mm
MICROSTRIP LINE WIDTH
=0.4mm ($Z_0=50\Omega$)
PCB SIZE=17.0mmx17.0mm

NJG1116HB3

■PACKAGE OUTLINE (USB8-B3)



Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.