REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical change for I_{DDQ} test in table IA. - LTG	07-04-17	Thomas M. Hess
B	Change measurements, in case outline X in figure 1. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	11-01-27	Thomas M. Hess
C	Add subgroups to table IIA in groups C and D. - LTG	11-06-23	David J. Corbett
D	To correct switching waveforms input/output test limits to figure 4. Add test equivalent circuits and footnote 1 to figure 4. Delete class M requirements throughout.—MAA	13-01-25	Thomas M. Hess

REV																				
SHEET																				
REV	D	D																		
SHEET	15	16																		

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
06-12-21

REVISION LEVEL
D

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUIT, WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON

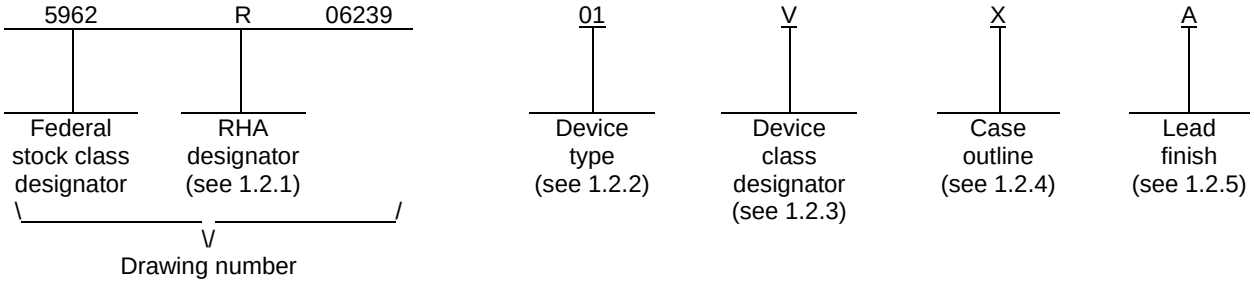
SIZE	CAGE CODE	
A	**67268**	**5962-06239**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACS630	16-bit parallel error detection and correction circuit with three-state outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	28	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DD})	-0.3 V dc to +6.0 V dc
Voltage on any pin during operation ($V_{I/O}$)	-0.3 V dc to V_{DD} + 0.3 V dc
DC input current (I_{IN})	±10 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum junction temperature (T_J)	+175°C
Thermal resistance junction-to-case (θ_{JC})	20°C/W
Maximum power dissipation (P_D)	350 mW

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Input voltage on any pin (V_{IN})	0.0 V dc to V_{DD}
Case operating temperature range (T_C)	-55°C to +125°C
Maximum input rise or fall time (t_r, t_f)	20 ns

1.5 Radiation features.

Maximum total dose available (dose rate = 50 to 300 rad(Si)/s)	1.0 x 10^5 rads (Si)
Single event phenomenon (SEP):	
No SEL occurs at effective LET (see 4.4.4.5)	≤108 MeV-mg/cm^2 4
No SEU occurs at effective LET (see 4.4.4.5)	≤108 MeV- mg/cm^2 4/
Neutron fluence	1X 10^{14} n/cm^2 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, all voltages are referenced to V_{SS}.

3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C unless otherwise specified.

4/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Function tables. The function tables shall be as specified on figure 3.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage 2/	V_{IH}		1, 2, 3	All	$0.7V_{DD}$		V
Low level input voltage 2/	V_{IL}		1, 2, 3	All		$0.3V_{DD}$	V
Positive input clamp voltage	$V_{IC}+$	For input under test I_{IN} = 18 mA, V_{DD} = 0.0 V	1, 2, 3	All	0.4	1.5	V
Negative input clamp voltage	$V_{IC}-$	For input under test I_{IN} = -18 mA, V_{DD} = open	1, 2, 3	All	-1.5	-0.4	V
High level output voltage (except DEF and SEF)	V_{OH1}	I_{OH} = -16 mA	1, 2, 3	All	V_{DD} – 0.8 V		V
		I_{OH} = -100 µA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 4.5 V to 5.5 V			V_{DD} – 0.2 V		
High level output voltage (DEF and SEF only)	V_{OH2}	I_{OH} = -8 mA	1, 2, 3	All	V_{DD} – 0.8 V		V
		I_{OH} = -100 µA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 4.5 V to 5.5 V			V_{DD} – 0.2 V		
Low level output voltage (except DEF and SEF)	V_{OL1}	I_{OL} = 16 mA	1, 2, 3	All		0.4	V
		I_{OL} = 100 µA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 4.5 V to 5.5 V				0.2	
Low level output voltage (DEF and SEF only)	V_{OL2}	I_{OL} = 8 mA	1, 2, 3	All		0.4	V
		I_{OL} = 100 µA $V_{IN} = 0.7V_{DD}$ or $0.3V_{DD}$ V_{DD} = 4.5 V to 5.5 V				0.2	
Three-state output leakage current	I_{OZ}	V_{DD} = 4.5 V to 5.5 V $V_{IN} = V_{DD}$ or V_{SS}	1, 2, 3	All	-10	10	µA
Input leakage current	I_{IN}	V_{DD} = 4.5 V to 5.5 V $V_{IN} = V_{DD}$ or V_{SS}	1, 2, 3	All	-5	+5	µA
Short circuit output current 3/ 4/	I_{OS}	$V_{OUT} = V_{DD}$ or V_{SS}	1, 2, 3	All	-300	300	mA
Power dissipation 5/ 6/ 7/	P_D	C_L = 20 pF	1, 2, 3	All		400	µW/ MHz
Quiescent supply current	I_{DDQ}	$V_{IN} = V_{DD}$ or V_{SS} V_{DD} = 5.5 V	1, 2, 3	All		100	µA
		M, D, P, L, R	1	All		100	
V_{DD} supply current, operating	$I_{DD\ (OP)}$	V_{IH} = 5.0 V, C_L = 20 pF V_{IL} = 0.0 V, V_{DD} = 5.0 V	1, 2, 3	All		2.0	mA/ MHz
Input capacitance	C_{IN}	f = 1 MHz at 0 V See 4.4.1c	4	All		24	pF
Output capacitance	C_{OUT}	f = 1 MHz at 0 V See 4.4.1c	4	All		24	pF
Functional tests		See 4.4.1d	7, 8	All			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, DBn to CBn	t_{PLH1}, t_{PHL1}	V_{DD} = 5.0 V ±10% V_{SS} = 0 V See figure 4	9, 10, 11	All	5.5	11.0	ns
Propagation delay time, S1 to DEF	t_{PLH2}		9, 10, 11	All	3.0	8.0	ns
Propagation delay time, S1 to SEF	t_{PLH3}		9, 10, 11	All	3.0	8.0	ns
Propagation delay time, output enable, S0 to DBn or CBn	t_{PZH}, t_{PZL}		9, 10, 11	All	2.0	9.5	ns
Propagation delay time, output disable, S0 to DBn or CBn	t_{PHZ}, t_{PLZ}		9, 10, 11	All	3.5	8.0	ns
Setup time, high or low, DBn or CBn to S1	t_s		9, 10, 11	All	0.5		ns
Hold time, high or low, DBn or CBn to S1	t_h		9, 10, 11	All	3.5		ns

1/ Devices supplied to this drawing are characterized at all levels M, D, P, L, and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Functional tests are conducted in accordance with the MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}$ (min) +20%, -0%; $V_{IL} = V_{IL}$ (max) +0%, -50%; as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH} (min) and V_{IL} (max).

3/ Not more than one output may be shorted at a time for a maximum duration of one second.

4/ Supplied as a design limit, but not guaranteed or tested.

5/ Guaranteed by characterization, but not tested.

6/ Power does not include power contribution of any CMOS output sink current.

7/ Power dissipation specified per switching output.

TABLE IB. SEP test limits . 1/ 2/ 3/

Device type	Bias V_{DD} = 4.5 V For SEU test	Bias V_{DD} = 5.5 V For SEL test
	Effective LET no SEU occurs [MeV/(mg/cm^2)]	Effective LET No SEL occurs [MeV/(mg/cm^2)]
All	LET ≤ 108	LET ≤ 108

1/ Devices that contain cross coupled resistance must be tested at the maximum rated T_A. For SEP test conditions, see 4.4.4.5 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature for latch-up test T_A = +125°C ±10°C. Test temperature for SEU test T_A = +25°C ±10°C.

Case outline X

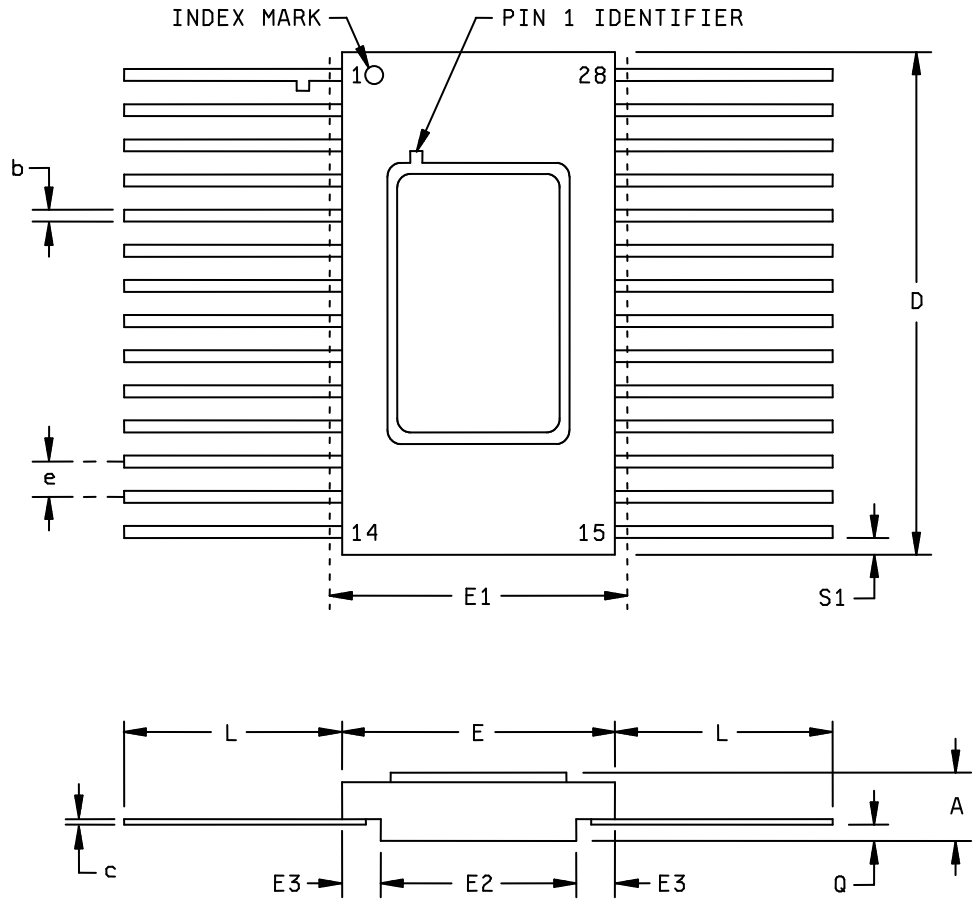


FIGURE 1. Case outline.

Case outline X

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.102	.122	2.59	3.09
b	.015	.020	.381	.508
c	.005	.008	.127	.203
D	.706	.720	17.9	18.3
E	.510	.520	12.9	13.2
E1	---	.550	---	13.9
E2	.395	.405	10.0	10.3
E3	.030	---	.762	---
e	.050 BSC		1.27 BSC	
L	.355	.375	9.01	9.52
Q	.026	.045	.660	1.14
S1	0.005	---	.127	---

FIGURE 1. Case outline – Continued.

Device type	All		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DEF	15	DB12
2	DB0	16	DB13
3	DB1	17	DB14
4	DB2	18	DB15
5	DB3	19	CB5
6	DB4	20	CB4
7	DB5	21	CB3
8	DB6	22	CB2
9	DB7	23	CB1
10	DB8	24	CB0
11	DB9	25	S0
12	DB10	26	S1
13	DB11	27	SEF
14	V_{SS}	28	V_{DD}

Pin names	Pin description
S0, S1	Mode control inputs
DBn	Bidirectional data bus
CBn	Bidirectional checkbit bus
SEF	Single error flag output
DEF	Double error flag output

FIGURE 2. Terminal connections.

CONTROL FUNCTIONS

Memory cycle	Control		EDAC function	Data I/O	Checkword	Error flags	
	S1	S0				SEF	DEF
WRITE	Low	Low	Generates checkword	Input data	Output checkword	Low	Low
READ	Low	High	Read data and checkword	Input data	Input checkword	Low	Low
READ	High	High	Latch and flag error	Latch data	Latch checkword	Enabled	Enabled
READ	High	Low	Correct data word and generate syndrome bits	Output correction data	Output syndrome bits	Enabled	Enabled

CHECKWORD GENERATION

Check word bit	16-bit data word															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

FIGURE 3. Function tables.

ERROR SYNDROME CODES

Syndrome error code	Error locations										
	DB										
	0	1	2	3	4	5	6	7	8	9	10
CB0	L	L	H	L	L	H	H	H	L	L	L
CB1	L	H	L	L	H	L	L	H	L	H	H
CB2	H	L	L	H	L	L	H	L	H	L	H
CB3	L	L	L	H	H	H	L	L	H	H	L
CB4	H	H	H	L	L	L	L	L	H	H	H
CB5	H	H	H	H	H	H	H	H	L	L	L

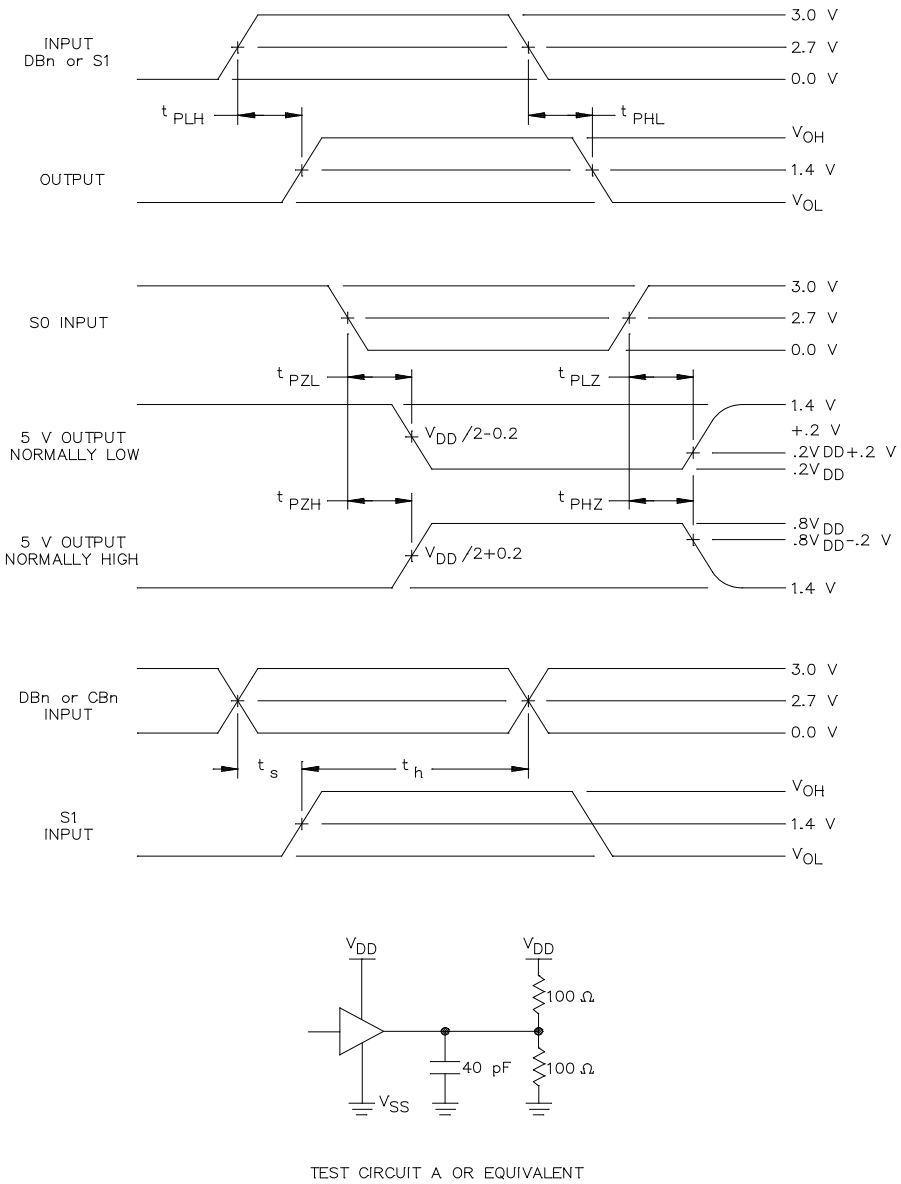
ERROR SYNDROME CODES – Continued.

Syndrome error code	Error locations											
	DB					CB						No error
	11	12	13	14	15	0	1	2	3	4	5	
CB0	H	H	L	H	H	L	H	H	H	H	H	H
CB1	L	H	H	L	H	H	L	H	H	H	H	H
CB2	H	L	H	H	L	H	H	L	H	H	H	H
CB3	L	L	H	H	H	H	H	H	L	H	H	H
CB4	H	H	L	L	L	H	H	H	H	L	H	H
CB5	L	L	L	L	L	H	H	H	H	H	L	H

ERROR FUNCTIONS

Total number of errors		Error flags		Data correction
16-bit data	6-bit check word	SEF	DEF	
0	0	L	L	Not applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

FIGURE 3. Function tables – Continued.



TEST CIRCUIT A OR EQUIVALENT

NOTE:

1. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on five devices with zero failures.

d. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8	1, 2, 3, 7, 8A, 8B, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 7, 8A	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits as specified in table IIB herein shall be required when specified and the delta values shall be completed with reference to the zero hour electrical parameter.

TABLE IIB. Burn-in delta parameters (+25°C).

Parameter 1/	Symbol	Condition	Delta limit 2/ 3/
Standby supply current	I_{DDQ}	T_A = 25°C	10 µA 4/

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.
2/ Devices having delta drift values in excess of the device specification or drawing limits shall be rejected.
3/ When expressed as a percentage value, it should be calculated as a proportion of the previous measured value.
4/ IDDQ limits were tightened from 100µA to 10µA for pre/post burn-in to determine the delta at 25°C. These tighter limits were implemented to more effectively screen out marginal parts upstream from group A and allow elimination of Deltas.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in Table IIA herein at T_A = +25°C ±5°C after an exposure of 2 x 10^{12} neutrons/cm^2 (minimum).

4.4.4.3 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test 4 devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA levels test conditions (SEP).

b. Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latch-up (SEL).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-01-25

Approved sources of supply for SMD 5962-06239 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0623901QXA	65342	UT54ACS630UCA
5962R0623901QXC	65342	UT54ACS630UCC
5962R0623901VXA	65342	UT54ACS630UCA
5962R0623901VXC	65342	UT54ACS630UCC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Boulevard Colorado Springs, Colorado 80907-3486