QuickScan™ 8-Bit Universal JTAG Access Port with Output Enable

QS3J245

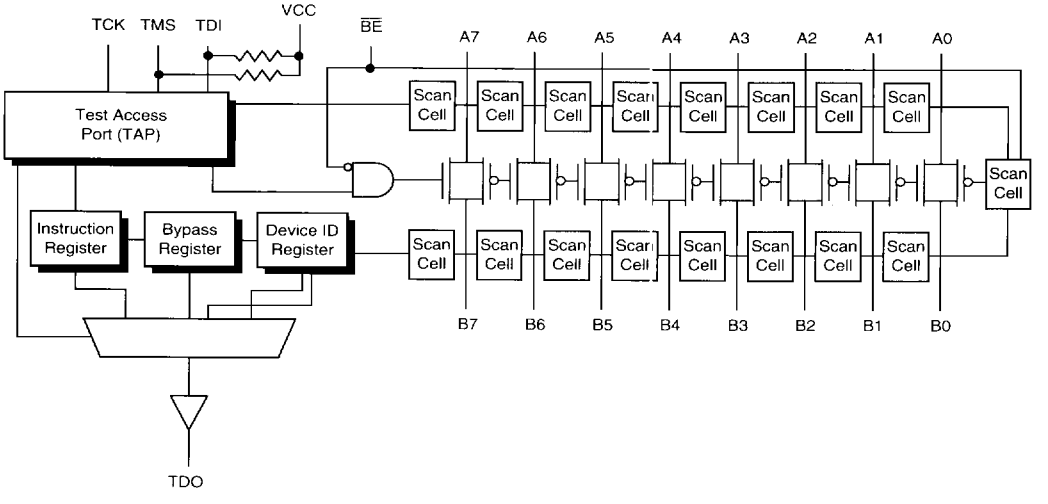
FEATURES/BENEFITS

- IEEE 1149.1 - 1993 compliant
- Direct bus connection when switches on
- Superset pinout of a '245
- Undershoot clamp diodes on all inputs
- Balanced ±12 mA drive in JTAG mode
- Low power QCMOS™ technology
- QuickSwitch® fast switch technology
- Zero added signal skew in non-JTAG mode
- Zero added ground bounce in non-JTAG mode
- TTL-compatible I/O
- Zero propagation delay in non-JTAG mode
- Available in 24-pin QSOP, HQSOP

DESCRIPTION

The QS3J245 JTAG QuickScan device is designed to provide JTAG access to a data bus, while being transparent to the system during normal (non-JTAG) operation. This is achieved by combining the "like-a-wire" characteristics of QSI's QuickSwitch devices with a JTAG boundary scan access port. The QS3J245 can provide scan coverage of system functional blocks without the cost overhead and performance penalties of individual scan components. When not in boundary scan mode, the QS3J245 QuickSwitch pass gates are turned on, allowing transparent, bi-directional data propagation. When in boundary scan mode, scan data can be captured from or loaded onto the data bus. The serial access port also can be used to monitor bus data while the device remains electrically transparent. This feature is useful for debugging or bus monitoring. The QS3J245 is IEEE1149.1-1990 compliant, with complete instruction register functionality, bypass and 32-bit device ID register.

FUNCTIONAL BLOCK DIAGRAM



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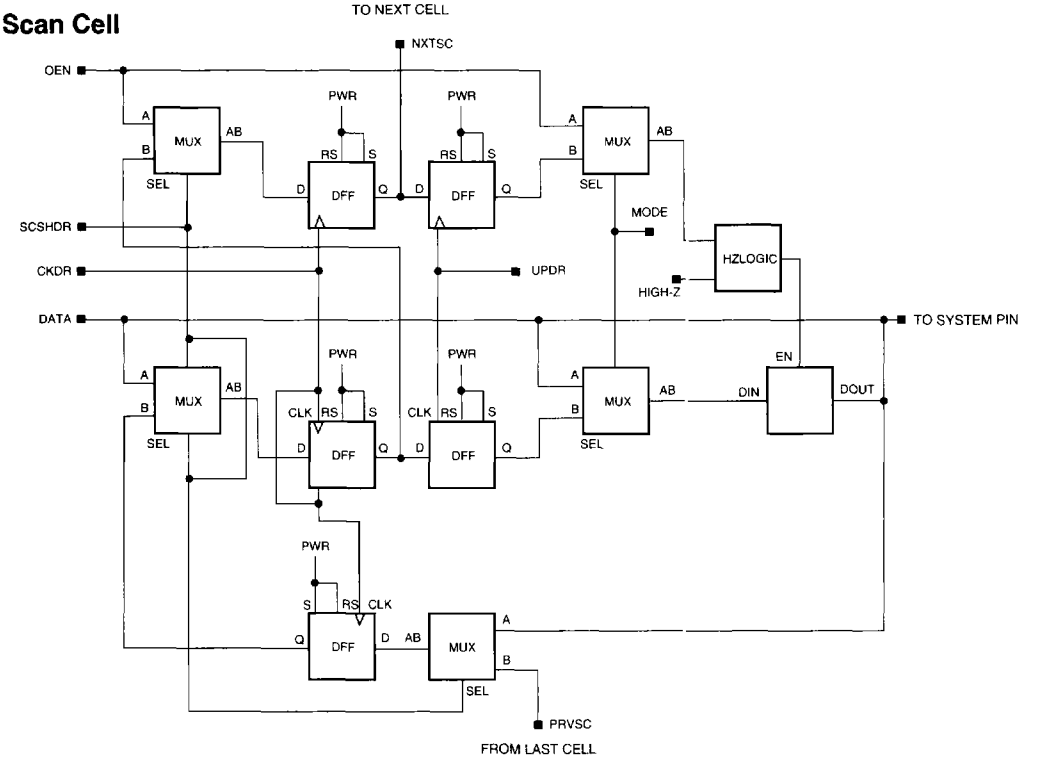
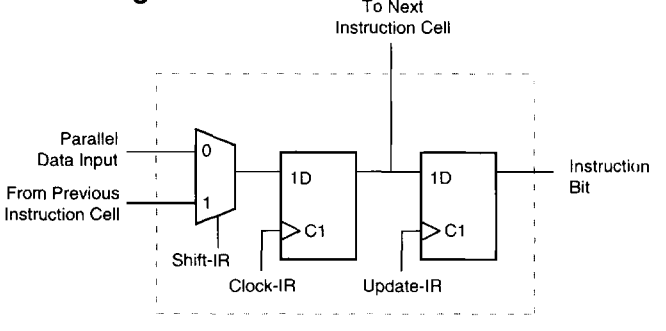
SUPPLEMENTAL BLOCK DIAGRAMS

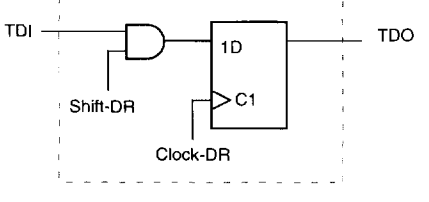
Scan Cell



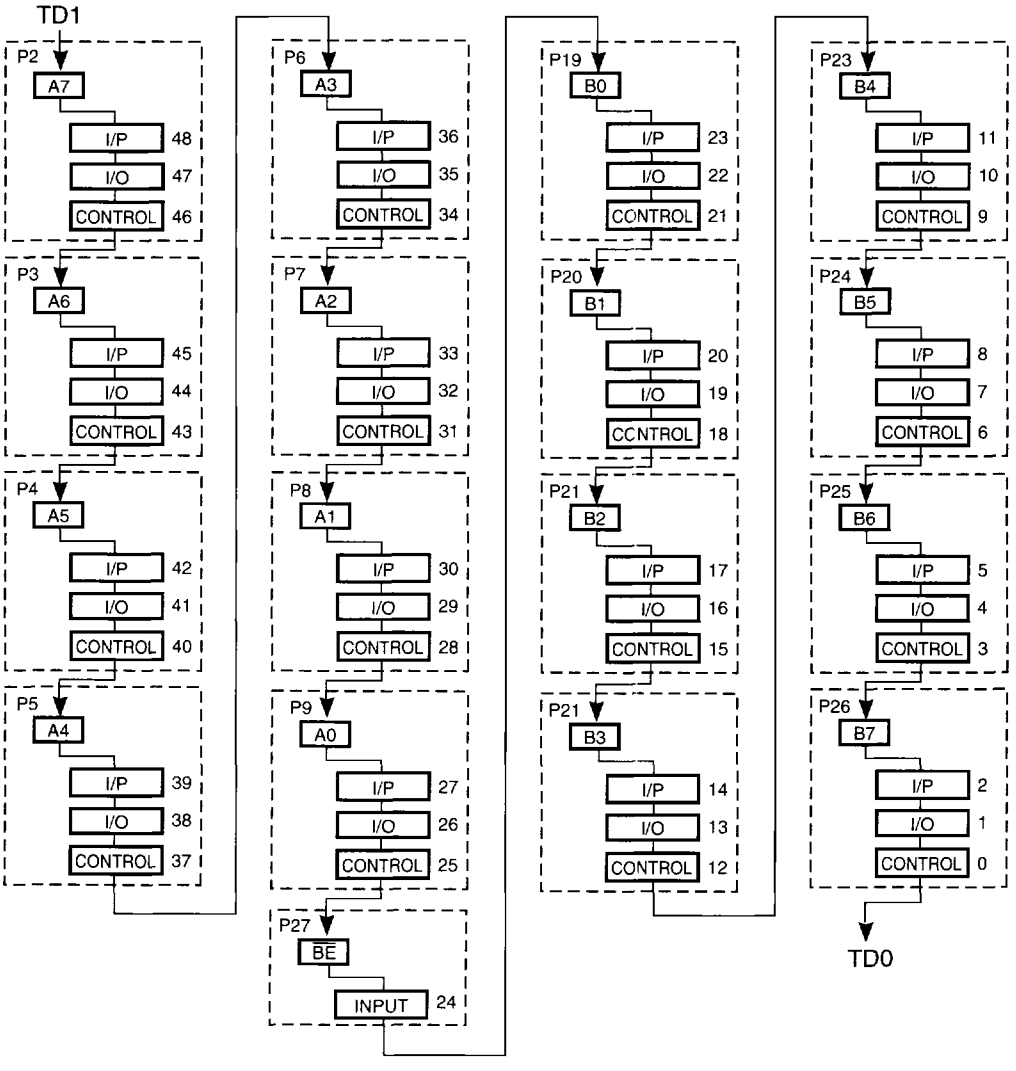
Instruction Register Cell



Bypass Register



Scan Chain Definition



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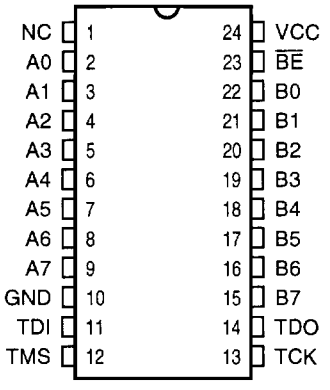
PIN CONFIGURATION
(All Pins Top View)

QSOP, HQSOP



PIN DESCRIPTION

Name	I/O	Function
A7-A0	I/O	Bus A
B7-B0	I/O	Bus B
$\overline{BE}$	I	Bus Enable
TDI	I	JTAG test data input: Provides for serial movement of test data into the device. Sampled at the rising edge of TCK.
TDO	O	JTAG test data input: Provides for serial movement of test data or instructions out of the device. Data is output on the falling edge of TCK.
TMS	I	JTAG test mode select.
TCK	I	JTAG test clock input.

INSTRUCTION REGISTER DEFINITIONS

Instruction Code	Instruction	Switch State
00000000	EXTEST	OFF
All others	BYPASS	ON
00000001	SAMPLE/PRELOAD	ON
00000010	IDCODE	ON
00000100	HIGH-Z	ON
00000101	CLAMP	OFF
00000110	BOUNDARY READ	ON

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	−0.5V to +7.0V
DC Switch Voltage V_S	−0.5V to +7.0V
DC Input Voltage V_{IN}	−0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	−3.0V
DC Input Diode Current with V_{IN} < 0	−20 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	−65° to +150°C

Note: Absolute Maximum Ratings are those conditions beyond which damage to the device may occur. Exposure to these conditions or beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rating conditions is not implied.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	QSOP Typ	QSOP Max	HQSOP Typ	HQSOP Max	Unit
Control/JTAG Pins	3	4	—	—	pF
QuickSwitch Channels (ON)	5	8	—	—	pF

Note: Capacitance is characterized but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military: T_A = –55°C to 125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions		Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
V_{OH}	Output HIGH Voltage (Scan mode)	Vcc = Min I_{OH} = –12 mA I_{OH} = –8 mA	COM MIL	—	2.4	—	V
V_{OL}	Output LOW Voltage (Scan mode)	Vcc = Min I_{OL} = 12 mA I_{OL} = 8 mA	COM MIL	—	—	0.55	V
$\lvert I_{IN} \rvert$	Input Leakage Current	0 ≤ V_{IN} ≤ Vcc		—	—	1	µA
$\lvert I_{OZ} \rvert$	Off-State Current (Hi-Z)	0 ≤ A, B ≤ Vcc		—	—	1	µA
R_{ON}	Switch ON Resistance(2)	Vcc = Min., V_{IN} = 0.0V I_{ON} = 30 mA	COM MIL	— —	5 10	7 15	Ω
R_{ON}	Switch ON Resistance(2)	Vcc = Min., V_{IN} = 2.4V I_{ON} = 15 mA	COM MIL	— —	10 15	15 20	Ω
R_{ON}	Switch ON Resistance(2)	Vcc = Min., V_{IN} = 4.0V I_{ON} = 15 mA	COM MIL	— —	17 25	20 30	Ω

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A,B) pins.

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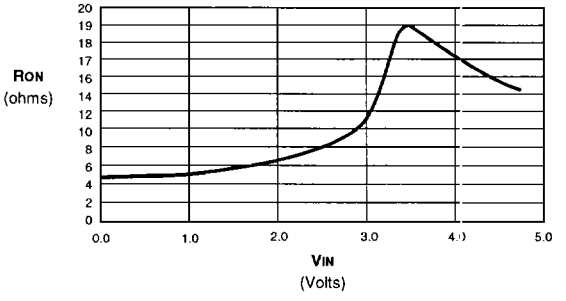
Switch ON Resistance Characteristics vs V_{IN} at 4.75 Vcc (Commercial Temperature Only)



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Max	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	30	µA
ΔI_{CC}	Power Supply Current per Input HIGH[2]	V_{CC} = Max., V_{IN} = 3.4V, F = 0 per Control Input	2.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz[3]	V_{CC} = Max., A & B Pins Open, Controls Toggling @ 50% Duty	0.5	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V, control inputs only). A and B pins do not contribute to Icc.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.

AC SWITCHING CHARACTERISTICS FOR NORMAL OPERATION

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military: T_A = –55°C to 125°C, V_{CC} = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description		QS3J245 Min	QS3J245 Typ	QS3J245 Max	Unit
t_{PLH}	Data Propagation Delay[2,3]	Com	—	0.25	—	ns
t_{PHL}	A ↔ B, Switch On	Mil	—	1.25	—	
t_{PZL}	Switch Turn-on Delay[1]	Com	1.5	—	6.5	ns
t_{PZH}	TCK → Switch On, or $\overline{BE}$ = H → On	Mil	1.5	—	7.5	
t_{PLZ}	Switch Turn-off Delay[1,2]	Com	1.5	—	5.5	ns
t_{PHZ}	TCK → Switch High-Z	Mil	1.5	—	5.5	
	or $\overline{BE}$ = H → High-Z					
$\lvert Q_{CI} \rvert$	Charge Injection, Typical[4,5]		—	1.5	—	pC

Notes:
1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagation delay other than the RC time constant delay of the switch resistance and the load capacitance. The propagation delay specified assumes a standard 50 pf external load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds negligible propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Measured at switch turn off, A to B, load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} at A = 0.0V.
5. Characterized parameter but not 100% tested.

SWITCHING CHARACTERISTICS FOR SCAN TEST OPERATION

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military: T_A = –55°C to 125°C, V_{CC} = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	State	Commercial Min	Commercial Max	Military Min	Military Max	Unit
t_{PLH} t_{PHL}	Data Propagation Delay TCK to TDO		3.5	13	3.5	16	ns
t_{PLZ} t_{PHZ}	Disable Time TCK to TDO		2.5	12	2.5	13	ns
t_{PZL} t_{PZH}	Enable Time TCK to TDO		3	15	3	17	ns
t_{PLH} t_{PHL}	Data Propagation Delay TCK to TDO Data Out	Update-DR Update-IR Test Logic Reset	5	18	5	22	ns
t_{PLZ} t_{PHZ}	Disable Delay TCK to Data Out High-Z	Update-DR Update-IR Test Logic Reset	4	17	4	22	ns
t_{PZL} t_{PZH}	Enable Delay TCK to Data Out High-Z	Update-DR Update-IR Test Logic Reset	5	19	5	25	ns
t_S	Setup Time, TDI to TCK		4.0	—	4.0	—	ns
t_H	Hold Time, TDI to TCK		4.5	—	4.5	—	ns
t_S	Setup Time, TMS to TCK		8.0	—	8.0	—	ns
t_H	Hold Time, TMS to TCK		2.0	—	2.0	—	ns
t_W	Pulse Width, TCK	HIGH	12	—	12	—	ns
		LOW	5	—	5	—	ns
f_{MAX}	Maximum Frequency TCK		25	—	25	—	MHz
t_{PU}	Power Up to TCK		100	—	100	—	ns
t_{PD}	Power Down Time		100	—	100	—	ns

Note:
1. All propagation delays measured from the falling edge of TCK.

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TEST ACCESS PORT (TAP) DESCRIPTION
The Test Access Port (TAP) consists of four pins dedicated solely to the operation of the test logic. The four pins include TMS (Test Mode Select), TDI (Test Data In), TDO (Test Data Out), and TCK (Test Clock). These pins are required by IEEE1149.1a.

TCK: (TEST CLOCK) This input provides the test clock for the test circuits. Data (TDI and TMS) is captured on the rising edge of TCK and outputs change on the falling edge.

TMS: (TEST MODE SELECT) This input controls test logic operation modes by directing the device through TAP controller states. This input has a pull-up resistor which guarantees that an undriven TMS input can put the TAP Controller into the Test Logic Reset state. The requirement that an unforced TMS input produce a logic high ensures that the normal operation of the design can continue without interference from the test logic.

TDI: (TEST DATA IN) This input is for serial data input of instructions and data to the test logic. Test data will arrive at TDO without inversion after the appropriate number of clock cycles as determined by the length of the register currently connected between TDI and TDO. This input has a pull-up resistor to implement a logic high for an undriven input. The requirement that an unforced TDI input produce a logic high is to assist in the determination of manufacturing defects in the test scan chain interconnect. A repeating field of 1's can indicate where a break in the scan chain interconnect occurred.

TDO: (TEST DATA OUT) This output provides the serial data output of test instructions and data from the test logic. Changes in the logic state and drive activity for this output occur upon the falling edge of TCK. This is to avoid a race condition when TDO is connected to TDI of the next chip in the scan chain which is sampled on the rising edge. This output shall remain inactive except when the scanning of data is in progress. This is to permit the ability to multiplex scan chains on the board without causing signal contention between multiple TDO outputs connected together to form parallel scan chains.

$\overline{BE}$: (Bus Enable) This pin is a overriding bus disable which when high disables all the switches.

TAP STATE DESCRIPTION

The main feature of the TAP controller is a state machine which is defined by the IEEE 1149.1 JTAG specification. These states change in response to the value of TMS (upon the rising edge of TCK), or upon power-up. In any given state, actions of the test logic occur on the falling or rising edge of TCK following the rising edge of TCK which caused the TAP Controller to enter the state initially.

NOTE: It may happen that actions to occur in one state happen on the same rising edge of TCK that causes the TAP Controller to enter the next state.

TEST LOGIC RESET: The test logic is disabled during this state so that normal operation of the system logic may proceed uninhibited. Following entry into the Test Logic Reset state, the IDCODE instruction is latched onto the instruction register output on the falling edge of TCK.

Two features of the state diagram are realized in this state. First it can be noted that independent of what state the TAP Controller is currently in, the QS3J245 will enter the Test Logic Reset state after, at most, five cycles of TCK with the TMS input high. Secondly, if a temporary glitch should occur on the TMS input during a rising edge of TCK, the TAP Controller will enter the Run-Test/Idle state then return to the Test Logic Reset state via the Select-DR state and Select-IR state provided that TMS returns to its logic high value for rising edge clocks following the glitch. The QS3J245 TAP Controller will also be forced into the Test Logic Reset state upon power-up.

RUN-TEST/IDLE: In this state, activity in the test logic occurs according to the instruction present. None of the mandatory instructions undertake any test logic activity during this state. During the description above regarding recovery from a glitch on the TMS input the current instruction is the BYPASS instruction and as a result no activity occurs in this state with that instruction preser t. This state is designed to provide the capability of performing built-in test functions during optional instructions. For instructions that do not activate test logic during this state, all test data registers retain their current state, i.e., remain idle.

SELECT-DR Scan: This is a temporary state in which all test data registers retain their previous values.

CAPTURE-DR: In this controller state, data may be parallel loaded into the data register selected by the current instruction; otherwise, it retains its previous values.

SHIFT-DR: In this state the test data register selected between TDI and TDO by the current instruction will shift one stage at each rising edge of TCK. TDO is active during this state. Test data registers not selected by the current instruction maintain their previous values.

PAUSE-DR: This is a temporary state in which all data registers retain their previous values. This state is intended to temporarily halt the shifting of test data into the data register selected while retaining the ability to keep TCK running; TCK may be a free-running clock.

EXIT1-DR: This is a temporary state in which all test data registers retain their previous values.

EXIT2-DR: This is a temporary state in which all test data registers retain their previous values.

UPDATE-DR: The parallel output register of the selected test data register may be updated on the falling edge of TCK in this state, provided the test data register has such a parallel output register. The intent of the parallel output register is to provide the ability to apply the contents of the test data.

SELECT-IR Scan: This is a temporary state in which the instruction register retains its previous value.

CAPTURE-IR: In this controller state data may be parallel loaded into the instruction register. The only restriction on what data may be is that its least significant bit must be a logic high, or 1, and its second least significant bit must be a logic low, or 0. These opposite state bits can be used to check the correct operation of the scan chain on the board by forcing a bit toggle when the instructions are shifted.

SHIFT-IR: In this state the instruction register selected between TDI and TDO will shift one stage at each rising edge of TCK. TDO is active during this state.

EXIT1-IR: This is a temporary state in which the instruction registers retains its previous values.

PAUSE-IR: This is a temporary state in which the instruction register retains its previous value. This state is intended to temporarily halt the shifting of test data into the instruction register while retaining the ability to keep TCK running.

EXIT2-IR: This is a temporary state in which the instruction register retains its previous value.

UPDATE-IR: The current instruction is updated on the falling edge of TCK following entry into the Update-IR state.

FEATURES OF THE TAP CONTROLLER

The TAP Controller will not be initialized by the operation of any system pin such as a system reset. The TAP controller will be initialized into the Test Logic Reset state upon power-up. This requirement is intended to avoid bus signal contention upon power-up by disabling the test logic which allows the system logic to operate normally and hence be controlled to avoid any contention. (The TAP Controller will return to the Test Logic Reset state after, at most, five clock cycles of TCK with TMS high; but the time required to enact that operation may not be sufficient to avoid contention).

Note that the TAP Controller has been defined such that six of the sixteen states have the ability to maintain their state provided that TMS remains at the same value it had when entering the state: **Test Logic Reset** to hold off the test logic during normal system operation, **Run Test/Idle** to undertake multi-cycle self tests, **SHIFT-DR** and **SHIFT-IR** to maintain the data shifting process for an extended period, and the **PAUSE-DR** and **PAUSE-IR** to halt the shifting process while some other activity is performed such as retrieving test data from additional memory. This feature is available in any/all states where multiple clock cycles may be required to achieve the desired outcome or where activity is to be halted but still provide the ability to make TCK a free-running clock.

REGISTER OVERVIEW

With the exception of the Bypass register, any test register may be thought of as a serial shift register with a parallel latch on each bit. The bypass register only contains a single bit shift register. As detailed above, there are 3 main instructions for controlling these registers:
Capture: causes the shift register to be parallel loaded from a specific source
Shift: causes shift register contents to shift from TDI to TDO
Update: causes shift register data to latch into the parallel register on the falling edge of TCK.

INSTRUCTION REGISTER

The ***Instruction*** register permits 8-bit instructions to be serially loaded which select a particular test data register and/or a specific test function. Each instruction will identify a particular test data register to be connected between TDI and TDO when in the Shift-DR state along with defining any particular test actions to occur to that test data register and/or any others. The order of scan through the instruction register must be least-to-most; that is, the least significant bit is closest to TDO for a loaded instruction. During the SHIFT-IR state the instruction shifts one bit between TDI and TDO upon each rising edge of TCK and appears without inversion at TDO.

During CAPTURE-IR, the ***Instruction*** register LSB's are set to "001". The bit value "001" in the least significant locations can be used to check the connectivity of the scan chain by forcing a bit toggle at each instruction during a scan of the instruction registers. The technique not only assists in determining the correct connectivity of the scan chain about the board, but also assists in pinpointing the location of any break in the scan chain. During UPDATE-IR, the value data that has been shifted into the ***Instruction*** register is loaded into the parallel latches. At this time, the current instruction is updated and relevant mode changes are initiated.

INSTRUCTION DEFINITIONS

The instructions required by IEEE1149.1 include the BYPASS, EXTEST and SAMPLE/PRELOAD instructions. The additional IDCODE, CLAMP and HIGH-Z has also been incorporated into this QuickScan device. In the following descriptions, each instruction will identify the test data register to be connected between TDI and TDO during the SHIFT-DR state, any restrictions on the binary codes used to implement the instruction, and what test data registers are used in undertaking the actions of the instruction.

1. EXTEST. This instruction allows circuitry external to the component package, typically the board interconnect, to be tested. ***Boundary Scan*** register cells at the QuickSwitch I/O pins are used to apply test and capture stimuli. When this instruction is selected, the states of all signals on the system input pins will be loaded into the ***Boundary Scan*** register upon the rising edge of TCK in the Capture-DR state and the contents of the ***Boundary Scan*** register will solely define the state of the system outputs upon the falling edge of TCK in the UPDATE-DR state. The 00000000 instruction binary code invokes the EXTEST instruction. During this instruction the ***Boundary Scan*** register is connected between TDI and TDO in the SHIFT-DR state. Additional binary codes for this instruction are permitted.

2. SAMPLE/PRELOAD. This instruction allows a "snapshot" of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the ***Boundary Scan*** shift register prior to selection of another boundary scan test instruction. During this instruction the ***Boundary Scan*** register is connected between TDI and TDO in the SHIFT-DR state. When this instruction is selected, the states of all signals on the system pins will be loaded into the ***Boundary Scan*** register upon the rising edge of TCK in the CAPTURE-DR state and the contents of the ***Boundary Scan*** register will be loaded into the parallel output register included with the ***Boundary Scan*** register bits upon the falling edge of TCK in the UPDATE-DR state.

Note that by interfacing these two actions through the Exit1-DR state, the current state of the system pins can be captured into the ***Boundary Scan*** register and stored into its parallel output registers for later application back onto those same pins. When the SAMPLE/PRELOAD instruction is selected, the test logic shall have no impact upon the system logic in performing its system function. The binary code may be device specific.

3. BYPASS. This instruction allows rapid movement of test data to and from other components on a board that are required to perform test operations by selecting the ***Bypass*** register, a single-bit shift-register stage, between TDI and TDO in the SHIFT-DR state to provide a minimum-length serial scan path. The "all others" opcode, along with the requirement that an undriven TDI input produce a logic high value, loads the BYPASS instruction if the scan chain is broken. In such a case all instructions following the break in the scan chain will be loaded with the BYPASS instruction and hence have no impact upon the system's normal functional operation. During CAPTURE-DR, the bypass register captures a logic 0.

4. IDCODE. The IDCODE instruction instructs the device to output an internal ID code from the device ***Identification*** register. This code is locked into the device ***Identification*** register on the rising edge of TCK following entry into the capture-DR state. The device ***Identification*** register contains an encoded part number, as well as Quality Semiconductor's manufacturer identity as defined by JEDEC. The full ID code for the QS3J245 is listed below. Note that the LSB is fixed at "1". This allows differentiation from the ***Bypass*** register output that would begin with logic 0. The ***Bypass*** register is output in the absence of ***Instruction*** register.

Version (bits 31-28)	Part Number (27-12)	QSI I.D. (11-1)	LSB(0)
0000	1011111010101110 (BEAE$_H$)	00011101001 (E9$_H$)	1

Each of the previously defined instructions fully indicates which data registers may operate or interact with the system logic while the instruction is current. Test data registers that are not selected by the current instruction do not interfere with the system logic or the operation of the test data registers currently selected. While a given instruction may lead to operation of more than one test data register, only one test data register may be connected between TDI and TDO during the SHIFT-DR state for the given instruction.

5. HIGH-Z. This instruction places all I/O cells (A0-A7 and B0-B7) in a high-impedence state and selects the bypass register to be connected for serial access between TDI and TDO in the ***Shift-DR*** state. When leaving the HIGH-Z instruction and selecting the EXTEST instruction for example , the data held in the boundary scan register prior to the selection of the HIGH-Z instruction will be applied to the device output pins.

6. CLAMP. This instruction allows the state of the signals driven from the component pins to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the device pins will not change while the CLAMP instruction is selected.

7. BOUNDARY READ. The boundary scan register is selected in the scan path. The value in the boundary scan register remains unchanged during Capture-DR.

BOUNDARY-SCAN REGISTER

The ***Boundary Scan*** register permits testing of printed circuit board interconnects such as opens and shorts while also providing access to the components inputs and outputs when testing or monitoring its system logic. In the QS3J245, the ***Boundary Scan*** register is 18 bits long, with one boundary scan cell for each QuickSwitch I/O. The Boundary-Scan cells facilitate both observation and control of the QuickSwitch gate I/Os'.

Each boundary scan cell can be configured to be an input, output, or tri-state depending on the input data at TDI.

Data applied to the TDI input appears without inversion at TDO during the SHIFT-DR state following 49 TCK cycles. In the CAPTURE-DR state, data will be parallel loaded into the ***Boundary Scan*** register upon the rising edge of TCK. Contents of the ***Boundary Scan*** register will be latched into its shadow register upon the falling edge of TCK in the UPDATE-DR state provided that it is selected by the current instruction. At power-up, the contents of each boundary scan cell is reset to logic 0.

BYPASS REGISTER

The ***Bypass*** register provides a minimum length serial path for the movement of test data between TDI and TDO. Use of this register speeds access to test data registers in other components on the board-level test data path. The ***Bypass*** register consists of a single shift register.

The ***Bypass*** register must set to a logic low value upon the rising edge of ¯CK in the SHIFT-DR state provided that it is selected by the current instruction. Upon an initial scan of the data registers connected across the board, all devices will connect the device ***Identification*** register while in the SHIFT-DR state. This condition is a result of power-up to initialize each JTAG device on board. The first logic high will be the framing bit of a device ***Identification*** register which would then indicate that the following thirty-one bits are identifiers to the specific device at that location of the scan chain.