

Am9580

Hard Disk Controller (HDC)

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Linked list command and data structure
- Controls up to 4 drives, any combination of hard or floppy disk drives
- ST506/412 and user-defined disk interface options supported
- Two on-chip sector buffers are programmable for sector sizes of 128, 256, and 512 bytes
- Error checking algorithms supported include
 - CRC/CCITT
 - Single burst Reed-Solomon
 - Double burst Reed-Solomon
 - External ECC (Error Correcting Code)
- On-chip DMA capability supports 32-bit addressing in 8/16-bit systems

GENERAL DESCRIPTION

The Am9580 Hard Disk Controller (HDC) is single chip solution to the problems encountered in designing Data Formatters and Disk System Controllers. Together with its companion part, the Am9581 Disk Data Separator (DDS), the Am9580 provides all the functions which until now have been found only on sophisticated board-level products.

The Am9580 has been designed with the necessary flexibility to cope with the differing requirements of today's broad marketplace while still retaining the advanced technology and innovative features that tomorrow's market will demand.

The Am9580 supports both Rigid and Flexible Disk Drives and their accompanying Data Formats. The Am9580 can control up to four drives, allowing any mix of Rigid and Flexible drives. As the characteristics of each drive are independently user-programmable, the system designer is provided with the flexibility needed to control any disk drive.

A sophisticated on-chip DMA Controller fetches the commands, writes status information, fetches data to be written on disk and writes data read from disk. The DMA operation is programmable to adjust the bus occupancy, data bus width (8-bit or 16-bit), and wait state insertion. Two sector buffers allow zero sector interleaving to access data on physically contiguous sectors, improving both file access

time and system throughput. The buffers are programmable for sector sizes of 128, 256, and 512 bytes.

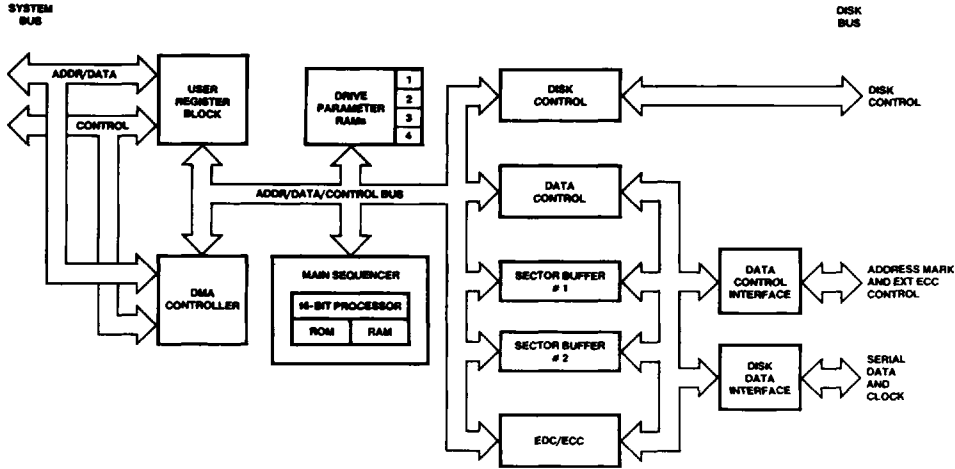
The Am9580 insures data integrity by selecting one error detecting code (CRC-CCITT) or one of two error correcting codes (single and double burst Reed-Solomon). Additionally, the HDC provides handshake signals to control external ECC circuitry to implement any ECC algorithm.

The Am9580 provides signals which are necessary to control external Encode/Decode and Address Mark circuitry such as found on the Am9581. By partitioning the Disk Control System in this way, future developments in the field of Data Encoding can still take advantage of the HDC's advanced Data Formatting and Control capabilities.

The flexible, user-programmable disk interface can be configured to control ST506/412 or standard Floppy Disk interfaces with only a few buffers required and can easily be adapted to other interface standards.

The Am9580 provides a comprehensive, high level command set for multi-sector disk I/O, marginal data recovery, diagnostics and error recovery. Commands may be linked together to be executed sequentially by the Am9580 without any host intervention. This linked list command structure also simplifies command insertion, deletion, or rearrangement.

BLOCK DIAGRAM



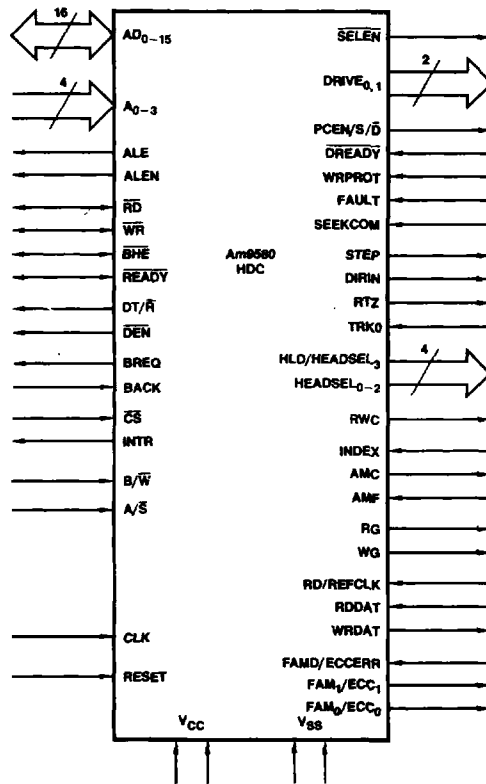
BD004030

Function	PGA Pin Number	LCC Pin Number
AD15	B1	1
AD14	B2	2
AD13	C1	3
AD12	C2	4
AD11	D1	5
AD10	D2	6
AD9	E1	7
VCC	E2	8
AD8	F1	9
AD7	F2	10
AD6	G1	11
AD5	G2	12
AD4	H1	13
AD3	H2	14
AD2	J1	15
AD1	J2	16
AD0	K1	17
READY	L2	18
CLK	K2	19
RESET	L3	20
ALEN	K3	21
ALE	L4	22
CS	K4	23

Function	PGA Pin Number	LCC Pin Number
WR	L5	24
RD	K5	25
VSS	L6	26
DT/ \bar{R}	K6	27
DE \bar{N}	L7	28
BHE	K7	29
A0	L8	30
A1	K8	31
A2	L9	32
A3	K9	33
BREQ	L10	34
BACK	K11	35
INTR	K10	36
A/ \bar{S}	J11	37
B/ \bar{W}	J10	38
INDEX	H11	39
FAMD/ECCERR	H10	40
RDDAT	G11	41
WRDAT	G10	42
VCC	F11	43
RD/REFCLK	F10	44
FAM0/ECC0	E11	45
FAM1/ECC1	E10	46

Function	PGA Pin Number	LCC Pin Number
RG	D11	47
WG	D10	48
AMC	C11	49
AMF	C10	50
RWC	B11	51
HLD/HEADSEL3	A10	52
HEADSEL2	B10	53
HEADSEL1	A9	54
HEADSEL0	B9	55
PCEN/S/ \bar{D}	A8	56
RTZ	B8	57
DIRIN	A7	58
STEP	B7	59
VSS	A6	60
SEEKCOMB	B6	61
FAULT	A5	62
WRPROT	B5	63
DREADY	A4	64
TRK0	B4	65
DRIVESEL1	A3	66
DRIVESEL0	B3	67
SELEN	A2	68

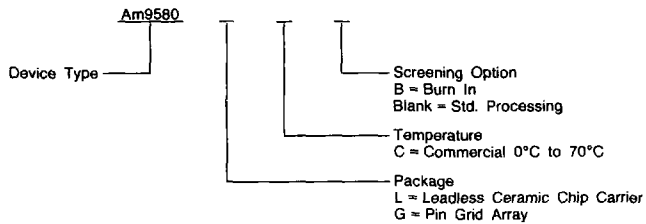
LOGIC SYMBOL



LS001351

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations

Am9580	GC (68 leads PGA) LC (68 LCC)
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Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

PIN DESCRIPTION

LCC Pin No.	Name	I/O	Description															
SYSTEM INTERFACE LINES																		
8, 43	VCC1, VCC2		+5V Power Supply.															
26, 60	VSS1, VSS2		Ground.															
19	CLK	I	System Clock. CLK is a TTL-compatible clock input to time DMA transfers and disk control operations (seeks).															
25	RD	I/O	Read (Active-Low). Read is a bidirectional, active-low, three-state signal. A LOW on this line indicates that the CPU or HDC is performing an I/O or memory read cycle. When the HDC is in Slave Mode, this is an input signal used by the CPU to read the internal registers of the HDC. When the HDC is the bus master, this signal is an output used by the HDC to access data from memory. RD and WR must not be active simultaneously.															
24	WR	I/O	Write (Active-Low). Write is a bidirectional, active-low, three-state signal. A LOW indicates that the CPU or HDC is performing an I/O or memory write cycle. When the HDC is in Slave Mode, it is an input signal used by the CPU to load the internal registers of the HDC. When the HDC is Bus Master, this signal is an output used by the HDC to write data into system memory. RD and WR must not be active simultaneously.															
22	ALE	O	Address Latch Enable (Active-High). The trailing edge of ALE latches the lower address word (A ₀ to A ₁₅) into the external address latch.															
21	ALEN	O	Upper Address Latch Enable (Active-High). The trailing edge of ALEN latches the upper address word (A ₁₆ to A ₃₁) into the external address latch. The HDC executes Upper Address latch cycles as necessary to minimize bus occupancy. The address is updated when a new command is executing or whenever the upper address for the current bus cycle differs from the address of the previous bus cycle.															
27	DT/R	O	Data Transmit/Receive (Three-State). When the HDC is bus master, a HIGH on this output indicates that data is being transmitted from the HDC. A LOW on this output indicates that data is being transferred into the HDC. This output is three-stated when the HDC is not in control of the system bus.															
28	DEN	O	Data Enable (Active-Low, Three-State). When the HDC is bus master, a LOW on this output indicates that data is driven on the Address/Data bus or the Address/Data bus is three-stated for receiving data. This output is three-stated when the HDC is not in control of the system bus.															
29	BHE	I/O	Byte High Enable (Active-Low). BHE is a bidirectional, active-low signal to enable data onto the most significant byte of the data bus (AD ₁₅ - AD ₈). BHE is LOW when data is to be accessed on the high portion of the bus. <table border="1" data-bbox="537 838 1201 994"> <thead> <tr> <th>BHE</th> <th>A₀</th> <th>Size</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>Whole word</td> </tr> <tr> <td>L</td> <td>H</td> <td>Upper byte</td> </tr> <tr> <td>H</td> <td>L</td> <td>Lower byte</td> </tr> <tr> <td>H</td> <td>H</td> <td>Reserved</td> </tr> </tbody> </table> <p>When the HDC is a bus master, this pin is an output. It is an input when the HDC is in Slave Mode. BHE is disabled and ignored when the HDC is strapped to a byte interface.</p>	BHE	A ₀	Size	L	L	Whole word	L	H	Upper byte	H	L	Lower byte	H	H	Reserved
BHE	A ₀	Size																
L	L	Whole word																
L	H	Upper byte																
H	L	Lower byte																
H	H	Reserved																
1, 2, 3, 4, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15, 16, 17	AD < 15:0 >	I/O	Address/Data Bus (Active-High). The Address/Data Bus is a time-multiplexed, bidirectional, three-state, 16-bit bus used for all system transactions. A logic HIGH on the bus corresponds to a "1" and a logic LOW corresponds to a "0." AD ₀ is the least significant bit. The presence of an address is defined by ALE or ALEN. When ALE is HIGH, the bus contains the Lower Address bits A ₀ to A ₁₅ . When ALEN is HIGH, the bus contains Upper Address bits A ₁₆ to A ₃₁ . The 32-bit address allows the HDC to direct linear addressing of 4 GBytes. The presence of data is indicated by RD and WR. When the HDC is in Slave Mode, RD and WR may be asynchronous to the system clock (CLK). In Master Mode the Address/Data Bus is driven asynchronously using a four-cycle bus transfer.															
30	A ₀	I	Address Line 0 (Active-High). This pin selects between the odd byte (HIGH) and the even byte (LOW) of the internal registers. It is used only when the HDC is in Slave Mode.															
33, 21, 31	A < 3:1 >	I	Address Line 1 to 3 (Active-High). When the HDC is in Slave Mode, these lines are the address inputs selecting one of the internal registers. These lines are ignored when the HDC is bus master.															
18	READY	I/O	Ready (Open Drain, Active-Low). When the HDC is bus master, this is an input to extend the bus cycle for slow memories and peripheral devices. When the HDC is in Slave Mode, this is an output indicating that the HDC is ready to complete the bus transfer. The READY input may be synchronous or asynchronous depending on the programming of the A/S strap.															
34	BREQ	O	Bus Request (Active-High). The HDC activates BREQ to request the control of the system bus.															
35	BACK	I	Bus Acknowledge (Active-High). BACK acknowledges the bus request of the HDC, indicating that the CPU has relinquished the system bus to the HDC. Since BACK is internally synchronized, transactions on BACK do not have to be synchronous with the HDC clock. BACK may be removed at any time to make the HDC release the bus. If the HDC DMA is preempted by removing BACK, the HDC will release BREQ for two clock cycles so that external devices may gain the mastership on the system bus.															
36	INTR	O	Interrupt Request (Active-High). INTR is activated when the HDC requires service by the CPU. Interrupt Request is reset whenever the status half of the Status/Command Register (SCR) is accessed.															

PIN DESCRIPTION (Cont.)

LCC Pin No.	Name	I/O	Description															
23	\overline{CS}	I	Chip Select (Active-Low). The host processor activates \overline{CS} to enable a Slave Mode access to read or write the internal registers of the HDC. This pin is ignored when the HDC is bus master.															
38	B/W	I	Byte/Word Strap. This pin selects either a byte (8-bit) or word (16-bit) interface. When a byte interface is selected, only AD < 7,0 > are used for data transfers and all operations are then byte operations. This pin must be strapped to either V_{CC} or V_{SS} . V_{CC} = byte interface V_{SS} = word interface															
37	A/ \overline{S}	I	Asynchronous/Synchronous Ready Strap. This line determines whether the \overline{READY} input is asynchronous or synchronous. When this line is strapped HIGH, the HDC internally synchronizes the \overline{READY} line to the system clock. When the line is strapped LOW, the HDC does not synchronize \overline{READY} . It must be synchronized to the system clock externally. V_{CC} = asynchronous \overline{READY} V_{SS} = synchronous \overline{READY}															
20	RESET	I	Reset (Active-High). When RESET is active, all outputs lines are inactive. Three-state outputs are floating. Inputs are ignored. A RESET pulse makes the chip enter the initialization procedure. Upon completion of initialization, an interrupt request will be issued. INTR will go High. If the user attempts to read from or write to the HDC prior to completion of reset, the ready line will remain inactive until the reset is completed, causing the CPU to wait.															
DISK INTERFACE LINES																		
68	SELEN	O	Select Enable (Active-Low). SELEN enables the drive specified by DRIVE < 1:0 >. When LOW, DRIVE < 1:0 > are valid. When HIGH, no drive is selected. A selected drive should respond with \overline{DREADY} .															
66, 67	DRIVE < 1:0 >	O	Drive Address (Active-High). These two lines in conjunction with SELEN determine the drive to be selected. The drive numbers are encoded as follows:															
<table border="1"> <thead> <tr> <th>DRIVE < 1 ></th> <th>DRIVE < 0 ></th> <th>Drive Selected</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>Drive 0</td> </tr> <tr> <td>L</td> <td>H</td> <td>Drive 1</td> </tr> <tr> <td>H</td> <td>L</td> <td>Drive 2</td> </tr> <tr> <td>H</td> <td>H</td> <td>Drive 3</td> </tr> </tbody> </table>				DRIVE < 1 >	DRIVE < 0 >	Drive Selected	L	L	Drive 0	L	H	Drive 1	H	L	Drive 2	H	H	Drive 3
DRIVE < 1 >	DRIVE < 0 >	Drive Selected																
L	L	Drive 0																
L	H	Drive 1																
H	L	Drive 2																
H	H	Drive 3																
56	PCEN/S/ \overline{D}	O	Precompensation Enable/Single/Double (Active-High). For all drive formats, this line signals when precompensation should be used. It enables precompensation if HIGH and disables precompensation if LOW. In addition, for floppy formats, it selects either the single- or double-density recording formats. The falling edge of SELEN may be used to latch Single/Double. A latched LOW indicates double-density and a latched HIGH single-density.															
64	\overline{DREADY}	I	Drive Ready (Active-Low) Drive Ready indicates that the currently selected drive is ready to Read, Write, or Seek. It must be asserted within 217 clocks after SELEN is asserted by the HDC. Once asserted by the selected drive, any negation of this line causes the current IOPB to be aborted. \overline{DREADY} is ignored while SELEN is HIGH.															
62	FAULT	I	Fault (Active-High). FAULT indicates a fault of the selected drive. Fault must be inactive as long as \overline{DREADY} is active. If it is ever asserted by the selected drive, the current IOPB is aborted and the drive deselected.															
63	WRPROT	I	Write Protect (Active-High). WRPROT is sampled after receipt of \overline{DREADY} during any IOPB command which involves a write to the disk. It is ignored during "Read Only"-type commands.															
61	SEEKCOM	I	Seek Complete (Active-High). SEEKCOM indicates that the drive is on track and that the heads have settled (head settling applies only to floppy disk drives). This line is sampled and verified High before any seek is issued. A HIGH indicates "Seek Complete." It is also used as an indication of head load completion for floppy drives.															
59	STEP	O	Step (Active-High). The HDC pulses the STEP line to move the head from one track to the next track. The width and spacing of pulses is programmable. This allows easy upgrades to higher performance drives.															
58	DIRIN	O	Direction In (Active-High). DIRIN indicates the direction the head should move on STEP pulses. When HIGH, the head should move toward higher track numbers (In, or towards the disk spindle). When LOW, it should move towards lower track numbers (Out).															
57	RTZ	O	Return to Zero (Active-High). A pulse on the RTZ output should recalibrate the head to track 0. Optionally, the HDC may recalibrate the drive by issuing STEP pulses until track 0 is reached (TRK0 becomes active). The RTZ pulse has the same width as the STEP pulse. The drive should assert SEEKCOM as an indication of the completion of the requested recalibration.															
65	TRK0	I	Track 0 (Active-High). The selected drive should assert TRK0 whenever the head is positioned over track 0.															
52	HLD/ HEADSEL < 3 >	O	Head Load/Head Select < 3 > (Active-High). For floppy drives, this line functions as a head load signal. It is active as long as the head should be loaded. SEEKCOM is sampled eight clocks after the assertion of HLD. If LOW, the HDC will then wait for it to go HIGH. If HIGH, the HDC assumes that the heads are already loaded. For hard disk drives, this line is the most significant bit of the head number.															
53, 54, 55	HEADSEL < 2:0 >	O	Head Select (Active-High). These lines output the lower three bits of the head number. The encoding is standard binary.															
51	RWC	O	Reduced Write Current (Active-High). When the drive currently selected is configured for a floppy disk or ST506/412 interface, this line indicates that the head is positioned over an inner track where the Write Current should be reduced.															

PIN DESCRIPTION (Cont.)

LCC Pin No.	Name	I/O	Description																				
39	INDEX	I	Index (Active-High). INDEX marks each revolution of the disk. The HDC only notes the LOW-to-HIGH transition. INDEX should be valid as long as DREADY is asserted.																				
49	AMC	O	Address Mark Control (Active-High). The HDC asserts AMC in conjunction with RG or WG to command the data separator to write or detect address marks. When RG is asserted, the HDC wants the data separator to search for the next address/data mark. When WG is asserted, the HDC wants the data separator to write an address mark. In both cases, the data separator should acknowledge completion by asserting AMF.																				
50	AMF	I	Address Mark Found (Active-High). The data separator asserts AMF in response to AMC.																				
47	RG	O	Read Gate (Active-High). RG indicates that a disk read is in progress. It commands the Phase Locked Loop (PLL) of the data separator to lock the RD/REF CLK to the serial data from disk. This output changes synchronously with the RD/REF CLK.																				
48	WG	O	Write Gate (Active-High). WG indicates that the HDC is writing to the disk. When WG is asserted disk data is strobed out synchronously with RD/REF CLK.																				
44	RD/REFCLK	I	Read/Reference Clock. RD/REFCLK is the data clock for sampling read data and strobing out write data. It is assumed valid if the following conditions are met: SELEN = LOW, DREADY = LOW, SEEKCOM = HIGH, and FAULT = LOW. While valid, this clock should be free from any glitches.																				
41	RDDAT	I	Read Data. RDDAT is the NRZ data input from the disk. The HDC samples RDDAT with the rising edges of RD/REF CLK. Therefore, the data should be set up by the data separator at the falling edge of RD/REF CLK.																				
42	WRDAT	O	Write Data. WRDAT is the NRZ data output to the disk. Transitions occur on the falling edge of RD/REF CLK.																				
40	FAMD/ECCERR	I	Floppy Address Mark Detect/ECC Error (Active-High). This signal indicates a data read error when external ECC is used. For single-density floppy formats, it indicates detection of a deleted data mark.																				
46, 45	FAM < 1:0 > / ECC < 1:0 >	O	<p>Floppy Address Mark/ECC Control (Active-High). These dual-function lines either control external ECC (hard disk format, external ECC enabled) or indicate the type of address/data mark to be used (single- and double-density floppy formats, AMC High).</p> <p>ECC Control:</p> <table> <tr> <td>00 = Idle</td> <td>No operation in the external ECC.</td> </tr> <tr> <td>01 = Reset</td> <td>External ECC should reset and prepare itself for an operation.</td> </tr> <tr> <td>11 = Generate</td> <td>Whether reading or writing, the external ECC should strobe data in and generate a check sum.</td> </tr> <tr> <td>10 = Check</td> <td>When reading, this state indicates that the ECC should accept the check sum from the disk. When writing, it should gate the check sum to the disk.</td> </tr> </table> <p>These states always proceed in the Gray code progression shown above: 00-01-11-10-00. The nominal state of the HDC is 00:Idle.</p> <p>Floppy Address Mark:</p> <table> <tr> <td>Double-Density</td> <td>00 = Index Address Mark (IAM)</td> </tr> <tr> <td></td> <td>XX = Data or Header Address Mark (DAM, IDA)</td> </tr> <tr> <td>Single Density</td> <td>00 = Index Address Mark (IAM)</td> </tr> <tr> <td></td> <td>01 = ID Address Mark (IDAM)</td> </tr> <tr> <td></td> <td>10 = Data Address Mark (DAM)</td> </tr> <tr> <td></td> <td>11 = Deleted Data Address Mark (DDAM)</td> </tr> </table> <p>Floppy Address Mark takes precedence over ECC Control.</p>	00 = Idle	No operation in the external ECC.	01 = Reset	External ECC should reset and prepare itself for an operation.	11 = Generate	Whether reading or writing, the external ECC should strobe data in and generate a check sum.	10 = Check	When reading, this state indicates that the ECC should accept the check sum from the disk. When writing, it should gate the check sum to the disk.	Double-Density	00 = Index Address Mark (IAM)		XX = Data or Header Address Mark (DAM, IDA)	Single Density	00 = Index Address Mark (IAM)		01 = ID Address Mark (IDAM)		10 = Data Address Mark (DAM)		11 = Deleted Data Address Mark (DDAM)
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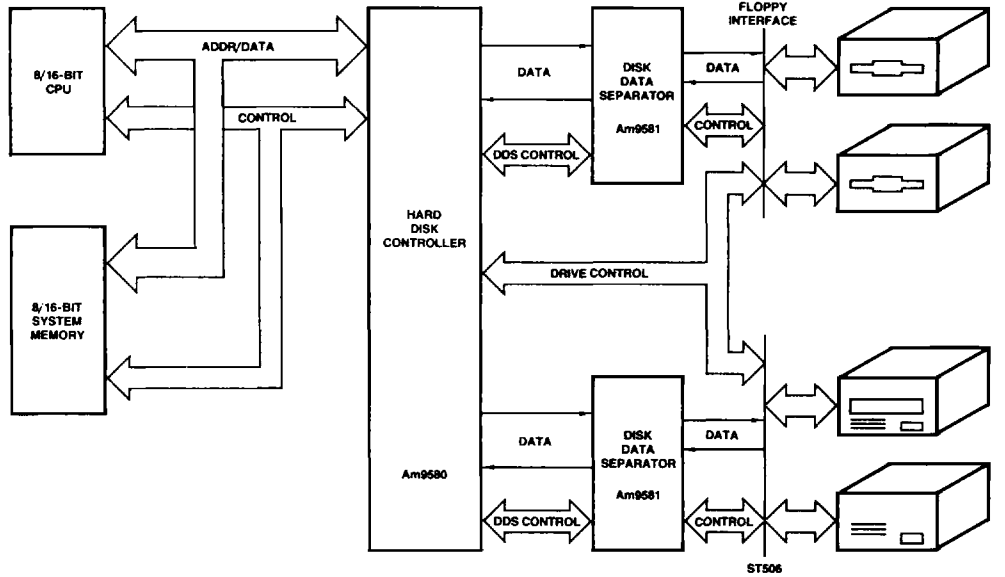


Figure 1. Disk Controller System

PRODUCT OVERVIEW

Hardware Architecture

The HDC supports two interfaces as shown in the block diagram in Figure 2; the system interface communicates with the host CPU and system memory, and the disk interface controls the data separator and the disk drives.

System Interface

The HDC is designed for easy interfacing to most 8-bit or 16-bit, multiplexed or demultiplexed, synchronous or asynchronous microprocessor buses. A strap pin programs the system interface for either byte (8-bit) or word (16-bit) mode. In Slave Mode, the host CPU can access the internal registers of the HDC. In Master Mode, the on-chip DMA controller controls the system bus.

DMA Controller

The on-chip DMA controller provides the HDC with the ability to execute complex disk I/O operations without intervention by the host CPU. The DMA controller scans the command chain stored in system memory, updates the Status Result Area when errors occur, and transfers the data between the internal sector buffers and system memory. Data may optionally be stored in noncontiguous memory to support linked-list data storage in word processing systems.

The DMA controller generates 32-bit linear addresses to access system memory of up to 4 GBytes directly. For multiple bus master systems, the DMA transfers can be throttled to dedicate only a certain share of the system bus bandwidth to the HDC. The Mode Register specifies the DMA burst length and dwell time. DMA bursts can be preempted by removing Bus Acknowledge (BACK). The HDC can insert a programmable number of software Wait States into DMA bus cycles. Additionally, hardware Wait States can be added via the READY input. The HDC updates the upper address word (A₁₆

to A₃₁) when a carry out of the lower 16 bits indicates it is necessary.

User Registers

The Mode Register defines the operation of the DMA controller. The Status/Command Register controls the basic operation of the HDC itself. The Next Block Pointer (NBP) Register links to the first Input/Output Parameter Block (IOPB) of the command chain. The Status Result Pointer Register and the Status Result Length Register define the Status Result Area.

Main Sequencer

The main sequencer translates the high-level system commands into the control signals for the various independent functional sections of the HDC. The power of this 16-bit processor is used to ease the complex data manipulation burden of the system CPU.

Drive Parameter RAMs

The Drive Parameter RAMs store the specification parameters for individual drives that adapt the HDC to any combination of disk recording schemes. The contents can be altered at any time with a single IOPB. Once loaded these parameters allow disk commands to be independent of the drive format. For example, the write command is the same whether it is for a single-density floppy disk drive or a Winchester hard disk drive.

Error Checking

The HDC features two powerful Reed-Solomon error-correcting codes, as well as the industry-standard error-detection code, CRC-CCITT. It also supports user-definable, external error-correction schemes. These, along with the programmable retry and correction attempt policy, allow maximum control of data integrity.

Sector Buffers

The HDC transfers data to or from disk without adding time constraints on the system bus bandwidth. The two internal sector buffers can be filled or emptied at any speed without interfering with the data transfer between the sector buffers and the disk. The two internal sector buffers can be toggled for zero sector interleave disk data operations. While one sector buffer is filled with data from disk, the other buffer is emptied by the DMA controller. Physically contiguous sectors on a track can thus be read or written on the fly.

Disk Control Interface

The lines of the Disk Control Interface conform to the ST506/412 disk drive interface standard. Other drive interface standards can be supported with some external circuitry. The ST506/412 interface selects one of the four disk drives and one of up to 16 heads. Any combination of floppy disk and hard disk drives can be connected. The Drive Parameter Blocks specify the seek dwell, seek pulse width, and head settle timing.

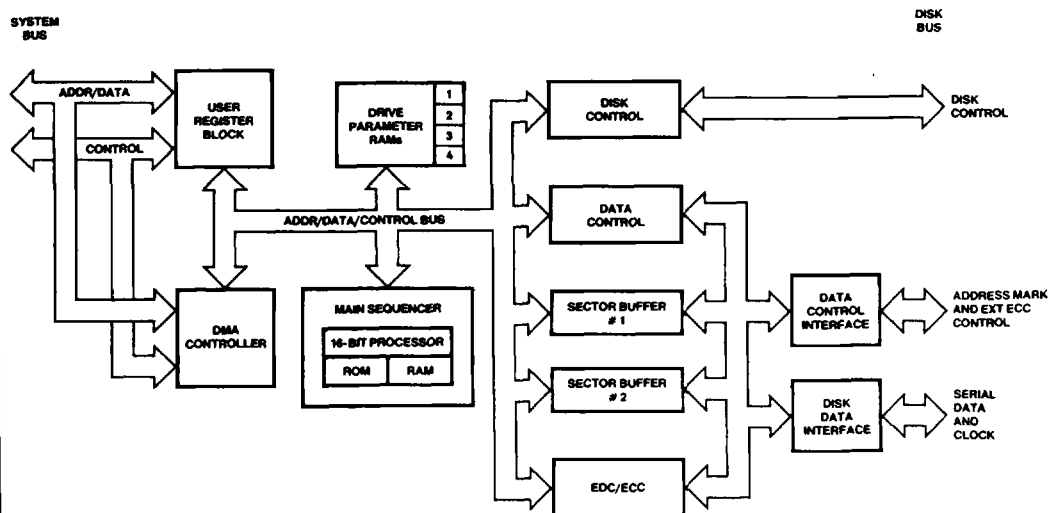
The HDC can perform implied and overlapped seeks. When the implied seek option is selected, the HDC automatically causes the appropriate seeks when issuing a read or write command. If this option is disabled, then the HDC should be

issued separate seek commands before executing read or write commands.

When the overlapped seek option is selected, drives can seek in parallel, thus minimizing the seek overhead in multiple disk drive systems. After the HDC has issued a seek command to one drive and while this drive performs the seek, the HDC scans subsequent IOPBs for commands requiring seeks on other drives. If the HDC finds such commands, it issues seek commands to these drives to make them seek in parallel. On receiving a "Seek Complete" from the first drive, the HDC resumes execution of the command chain.

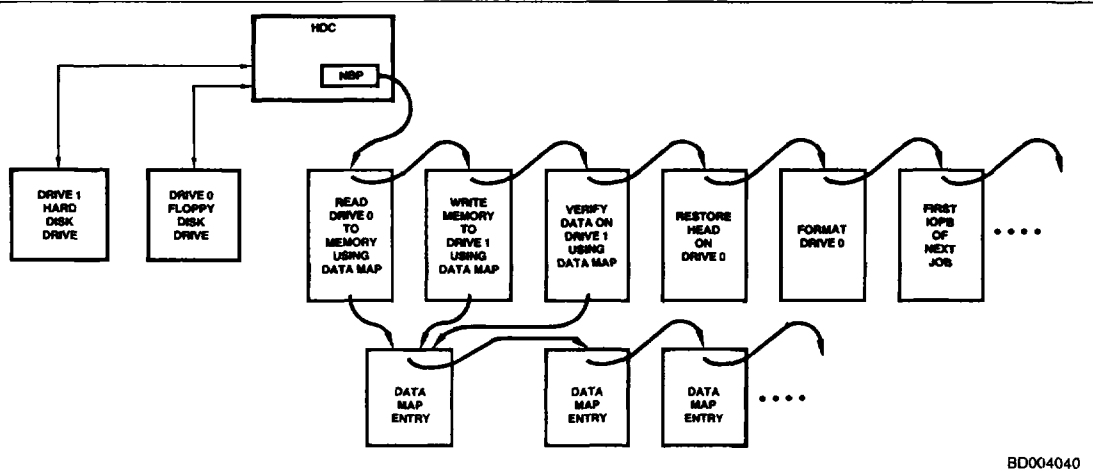
Disk Data Interface

The Disk Data Interface controls the Address Mark handshake with the data separator, controls the optional external ECC logic, and handles the serial data input and output. Operating asynchronously to the other blocks of the device, the Disk Data Interface is driven by the Read/Reference Clock (RD/REF CLK) generated by the data separator. The Disk Data Interface converts the data stored in the sector buffer into a serial bit stream for the disk or it deserializes the incoming bit stream to be loaded into one of the sector buffers. Non-data information, such as the header, pads, gaps, preambles, and postambles, is conditioned according to the parameters stored in the Drive Parameter RAMs to meet the defined recording standard.



BD004030

Figure 2. HDC Block Diagram



BD004040

Figure 3. IOPB Linked-List

Software Architecture

IOPB Command Structure

The HDC features a high-level data and command structure. The basic unit of a command structure is the Input/Output Parameter Block (IOPB). The host CPU creates IOPBs in system memory to pass control and status information to the HDC. The HDC fetches these IOPBs using its on-chip DMA controller. Each IOPB specifies one disk command and contains all parameters needed to execute it. To start execution of an IOPB, the host CPU loads the address of the first IOPB into the Next Block Pointer Register and issues the command "Start Chain" by programming the Status/Command Register. After the IOPB is executed, the HDC reports the status information and waits for further instructions. The host CPU can examine the Status/Command Register for information about the command termination. The CPU can also get status from the Status Result Block in memory if an error occurs.

Optionally, IOPBs may be connected in a linked-list format which the HDC can interpret sequentially. With this structure, a complex list of disk commands can be set up and executed by the HDC without CPU intervention. The CPU is then totally free from any processing for disk control. For example, the host CPU can set up a list of commands to copy an entire floppy disk to a hard disk, verify that the data was copied correctly, and, if so, reformat the floppy disk—all without host CPU intervention. This is shown in Figure 3.

First, the HDC reads the data from the floppy disk into a temporary buffer in system memory. The data-mapping option lets the system use any free memory space. The subsequent write command uses the same data map to transfer data to the hard disk. The verify command ensures that data was written correctly by performing a byte-by-byte comparison of the data on the hard disk with the data in the temporary buffer. Optionally, the chain execution may be stopped in the event of an error in the write or verify command. If there was no problem with the data transfer, the HDC will perform the restore and format commands. Optionally, the system can be informed that the disk copy has been completed and that the memory space allocated for the temporary buffer of the disk data is free to be reused.

The seek-lookahead mechanism of the HDC will move forward through the IOPB chain to see where it can overlap head seeks. In this example, the HDC will move the head on the hard disk into position for the write command while the read command is still executing. When the HDC starts executing the write command, it will look ahead in the chain and start executing the restore command on the floppy drive to move the head back to track zero. If possible, the HDC will do additional head positioning for commands further down the IOPB chain.

An IOPB command chain is basically a queue of jobs waiting for execution by the HDC. This offers a pre-defined and efficient structure for the operating system to handle its disk I/O. The ID field of the IOPB allows the operating system to link a particular disk command to the user process that made the disk request. The jobs can thus be placed in the HDC job queue and then forgotten by the operating system unless an error occurs. All the information required to retrace an error is provided by the HDC Status Result Block.

Since the HDC manages the disk job queue, it can look ahead in the queue to overlap some time-consuming operations. Head movement (seeking) can require a major portion of the disk access time. Since the HDC controls up to four drives, it can perform an IOPB operation on one drive while it is executing seeks for future IOPBs on the other drives. This can eliminate the seek-time overhead when those subsequent IOPBs are finally executed.

Data Mapping

Sector data to be transferred to or from the disk may be stored in noncontiguous system memory using the data mapping option. Definable portions of a disk file can be written to or read from separate areas of memory on a byte-by-byte basis. Word processing systems can employ this feature to save text arranged in a linked-list directly on disk and eliminate the time-consuming task of converting the linked-list into a linear list. The Data Map defines the linked-list data structure. The Data Map option is processed by the HDC while the disk is in operation, so that data maps can be handled without affecting data transfer rate.

Status Result Blocks

When the HDC finds that an IOPB has caused an error, it writes a Status Result Block (SRB). Errors can be caused by invalid command codes, disk read and write errors, and seek or memory time-outs. Since the SRB contains the ID number for the IOPB which caused the error, the operating system can determine which disk I/O job caused the error and report this to the user. Depending upon the type of error and what policy has been selected, the HDC may continue with the IOPB chain automatically or wait for the host processor to tell it whether to start over or continue. The SRBs contain all the specific information required to find the exact location of the error and to make recovery as complete as possible.

Registers

When the IOPB command chain has been set up, the Next Block Pointer Register of the HDC should be set to point to the first IOPB in the chain. Writing a Start Chain command to the Status/Command Register causes the HDC to copy the first IOPB into its internal memory. It starts executing the IOPB after updating the Next Block Pointer to the next command in the IOPB chain. The Status/Command Register also reports HDC error and status codes (such as memory time-outs, IOPB option results, and other information related to the internal operation of the HDC).

The Status Result Pointer points to an area of contiguous memory reserved for Status Result Blocks (SRBs). The length

of this memory block is defined by the Status Result Length Register, which specifies the number of SRBs. (Each SRB is 10 bytes.) The error-handling scheme of the operating system can manipulate this as needed to coordinate disk use.

The Mode Register controls the HDC's share of the system bus bandwidth to adapt the HDC to the system performance requirements.

Register Description

Four registers control the operation of the HDC. These registers can be accessed directly by the host CPU. The addresses are shown in Figure 4.

Mode Register

Bit assignments of this 16-bit read/write register are shown in Figure 6. This register may be read or written at any time. A hardware or software reset initializes all bits in this register to zero. DMA Burst Length and DMA Dwell Time control the share of the system bus bandwidth allocated to the HDC. DMA Burst Length defines the maximum length of a DMA burst in bytes, and DMA Dwell Time specifies the minimum time between DMA bursts that the HDC must stay off the system bus.

Wait Select (WS) defines the number of software Wait States that are inserted into bus transactions. The HDC inserts this number of Wait States and then waits until the **READY** line is activated (hardware Wait States). If no acknowledge is received within 2^{16} clock periods, a time-out error is generated.

\overline{CS}	A ₃	A ₂	A ₁	Register Accessed
L	L	L	L	Status/Command Register
L	L	L	H	Mode Register
L	L	H	L	Next Block Pointer (low word)
L	L	H	H	Next Block Pointer (high word)
L	H	L	L	Status Result Pointer (low word)
L	H	L	H	Status Result Pointer (high word)
L	H	H	L	Status Result Length
L	H	H	H	Reserved
H	X	X	X	No Register Accessed

Figure 4. Register Addresses

MODE	B/W	BHE	A ₀	AD<15:8>	AD<7:0>
Word Access	L	L	L	HIGH	LOW
	L	H	L	—	LOW
	L	L	H	HIGH	—
Byte Access	H	X	L	—	LOW
	H	X	H	—	HIGH

Figure 5. Data Bus Assignment for Byte/Word Transfers

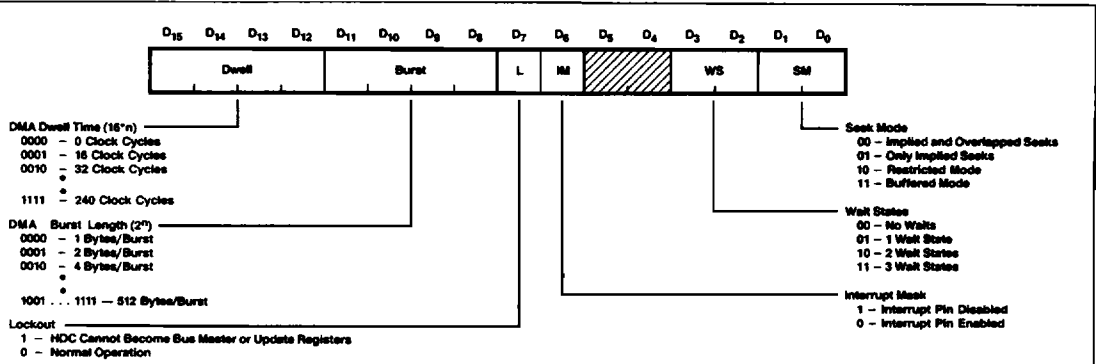


Figure 6. Mode Register

DF003790

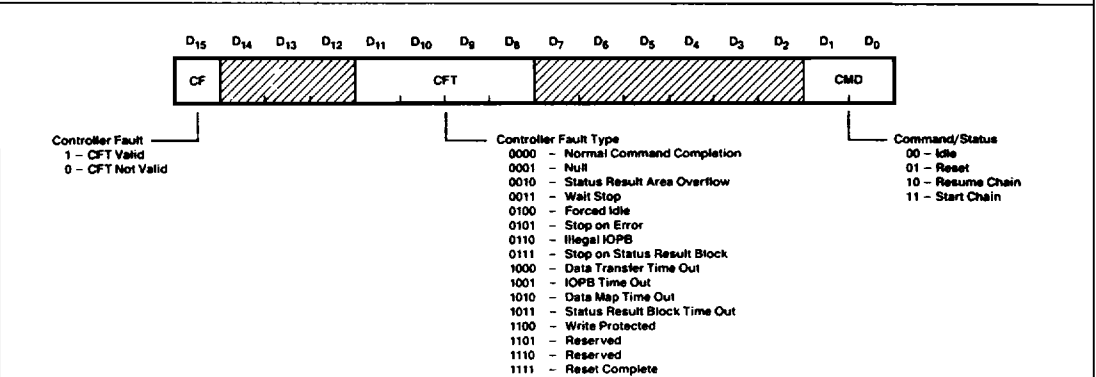


Figure 7. Status/Command Register

DF003800

The two seek bits control the seek mode. When the Implied Seek option is enabled, the HDC automatically positions the head to the desired track when executing disk commands. This means that explicit seek commands need not precede disk read and write commands. Overlapped seeks are seeks on multiple drives in parallel. In Restricted Mode, seek operations are controlled by external logic. Therefore, STEP, DIRIN, and RTZ should not be connected. In Buffered Mode, seek operations and drive selection are handled externally. Therefore, all disk control lines should not be connected. In Buffered Mode, the HDC controls only the data transfer (RDDAT, WRDAT, RD/REF CLK and WG), the data separator handshake and ECC operation (AMC, AMF, INDEX, FAM/ECC(1:0), and FAMD/ECCERR).

When the Lock-out bit is set, the HDC does not read or modify internal registers. It also keeps the DMA off the system bus. However, dependent on the time this bit is being set, it may execute further DMA bursts to finish the current sector transfer.

The Interrupt Mask enables and disables the Interrupt output pin.

Status/Command Register

The host CPU can access the Status/Command Register any

time (Figure 7). The execution of some commands modify the content of this register. A hardware or software reset initializes all bits of the Status/Command Register to zero.

Command

When the command field is written by the host CPU, it causes the HDC to enter the programmed state. By reading this field, the host CPU can determine the state of the HDC.

Idle The HDC is not performing any action. If CF (Controller Fault) is asserted, then CFT (Controller Fault Type) gives the result of the last known action performed. Any command might be written to this command field while the HDC is idle.

Reset The software reset is immediately executed. On completion of reset, the HDC goes to the idle state. Any access of a register while in the reset state holds READY inactive until the reset is completed, causing the CPU to wait. A software reset is equivalent to a hardware reset.

Resume Chain The HDC resumes execution of the IOPB chain where it was interrupted due to a Status Result Area overflow. When receiving the Idle command, the HDC completes the current IOPB and then enters the Idle state.

Start The IOPB chain pointed to by the Next Block Pointer is executed. When receiving the Idle command, the HDC completes the current IOPB and then enters the Idle state.

Controller Fault

When this bit is set, the Controller Fault Type field is valid. The CF-bit is set by the HDC when entering the Idle state and reset when leaving the Idle state.

Controller Fault Type

The Controller Fault Type indicates the status of the HDC upon entering the Idle state. Whenever the Controller Fault Type is updated, the HDC issues an interrupt.

- Normal Complete** — Execution of the IOPB chain terminated without fault.
- Null NBP** — A Resume or Start Chain command was given with NBP zero.
- SRA Overflow** — The HDC filled the Status Result Area (SRA).
- Wait Stop** — An IOPB was completed with the option Wait Stop set.
- Forced Idle** — An Idle command was given while executing the Resume or Start Chain command.
- Stop on Error** — Nonrecoverable disk error in conjunction with the SE-bit set caused the HDC to terminate chain execution.
- Illegal IOPB** — The HDC attempted to execute an undefined IOPB.
- SRB Error** — A Status Result Block (SRB) was written when executing an IOPB with the Stop on SRB (SSRB) option set.
- Data Time Out** — Memory Time Out when transferring data.
- IOPB Time Out** — Memory Time Out when reading an IOPB.
- DM Time Out** — Memory Time Out when reading the Data Map.
- SRB Time Out** — Memory Time Out when writing a Status Result Block.
- Write Protected** — WRPROT line was asserted when executing a Disk Write command.
- Reset** — Hardware or software reset has been executed.

Next Block Pointer

The Next Block Pointer Register is a 32-bit register pointing to the IOPB currently being executed. The HDC updates it on IOPB completion.

Status Result Pointer

The 32-bit Status Result Pointer Register points to the system memory location where the next Status Result Block can be written. This pointer is updated after adding a new Status Result Block to the Status Result Area.

Status Result Length

The 16-bit Status Result Length Register defines the size of the Status Result Area in terms of the number of Status Result Blocks. Therefore, the maximum size of the Status Result Area is 65536 Status Result Blocks.

The Next Block Pointer, the Status Result Pointer, and the Status Result Length should only be updated while the HDC is in the Idle state.

COMMAND DESCRIPTION

All operations of the HDC result from commands. Commands are set up in system memory in IOPBs (I/O Parameter Blocks) (Figures 8 and 9). The HDC starts interpreting the command list after receiving the "Resume Chain" or "Start Chain" command from the host CPU (see Status/Command Register description). *Errors and warnings on command execution are reported by adding Status Result Blocks (SRB) to the Status Result Area.*

Normal Disk I/O Commands

The HDC supports three normal disk I/O commands: READ, WRITE, and VERIFY. The multi-sector operation is performed on DRIVE starting at the desired TRACK, HEAD and SECTOR. RECORD COUNT defines the number of sectors. The General Select Byte in the Drive Parameter Block specifies whether the track number or the head number is to be incremented on sector overflow. SOURCE/DESTINATION ADDRESS is the starting address of the data block in system memory (DME Low) or the address of the first Data Map Entry (DME High). These commands verify the head position before attempting the data transfer. The Data Mark option allows the DATA MARK parameter to be used instead of FBH. On single-density floppy disks, the Data Mark option also causes the search for a deleted data mark.

READ

READ performs a multi-sector data transfer from disk to system memory.

WRITE

WRITE performs a multi-sector data transfer from system memory to the disk.

VERIFY

VERIFY compares multi-sector data on disk with data stored in system memory. It reports any mismatches or data read errors by updating the Status Result Area.

Initialization Commands

FORMAT

The HDC formats the number of tracks specified by TRACK COUNT starting at HEAD and TRACK. The head and track number are incremented according to the General Select Byte in the Drive Parameter Block. The sectors are numbered like the order given in the sector map, which is sequentially loaded from system memory starting at MAP POINTER. The number of sectors per track is specified in the Drive Parameter Block of this DRIVE. The data field of each sector is filled with PATTERN.

RELOCATE TRACK

A relocation vector is written to all data fields of a bad track. The relocation vector consists of the new track number (ALTERNATE TRACK) and the new head number (ALTERNATE HEAD) (i.e., the track's relocated location). Also, the address mark is changed from FEH to FDH to mark that this track is relocated. Thus, when the HDC encounters three consecutive sectors with an FDH data mark, it assumes the track has been relocated. This command is illegal for single-density floppy disk drives.

LOAD DRIVE PARAMETER BLOCK

This command loads the Drive Parameter Block (DPB) for the selected DRIVE into the internal Drive Parameter RAM (see "Drive Parameters").

DUMP DRIVE PARAMETER BLOCK

The Drive Parameter Block for the selected DRIVE is transferred from the internal Drive Parameter RAM to the DESTINATION ADDRESS.

Marginal Data Recovery Commands**READ PHYSICAL SECTOR**

This command lets the user recover a marginal data field which is unrecoverable by normal disk error recovery procedures. First it seeks to the desired track. If TRACK VERIFY is selected, the HDC reads ID fields until three consecutive sector headers show the right track number. This verifies it is

on the right track. Beginning with the next index mark, the HDC starts counting the PHYSICAL SECTOR number of IDs specified by "PHYSICAL SECTOR" to locate the desired sector. It reads the data field while disregarding the ID field. The user can thus possibly recover data where headers and/or data marks have been rendered unreadable. PHYSICAL SECTOR specifies the absolute location of the sector. No retries are performed.

READ ID

READ ID attempts to recover the header ID information of a marginal sector. If LOCATOR DUMP is selected, then the first valid ID read is transferred to the DESTINATION ADDRESS. If LOCATOR DUMP is not selected, then the ID of the absolute sector specified by PHYSICAL SECTOR is transferred to DESTINATION ADDRESS. If this command is successfully executed, it updates the HDC's track position.

LOAD BUFFER

The data pointed to by the SOURCE ADDRESS is transferred to the internal sector buffer. The number of bytes transferred is determined by the sector size for the selected DRIVE.

DUMP BUFFER

The data in the internal sector buffer is transferred to system memory starting at DESTINATION ADDRESS. The number of bytes transferred is specified by the sector size for the selected DRIVE.

D ₁₅	NEXT IOPB POINTER <15:0>		D ₀
	NEXT IOPB POINTER <31:16>		
	ID		
	COMMAND CODE ⁽¹⁾	OPTIONS	
	BYTE 9	BYTE 8	
	BYTE 11	BYTE 10	
	BYTE 13	BYTE 12	
	BYTE 15	BYTE 14	
	BYTE 17	BYTE 16	
	BYTE 19	BYTE 18	

(1) Not yet defined.

Figure 8. IOPB Structure

Command	Code	Options								Byte 9	Byte 8	Byte 11	Byte 10	Byte 13	Byte 12	Byte 15	Byte 14	Byte 17	Byte 16	Byte 19	Byte 18
		7	6	5	4	3	2	1	0												
Read	0C	W	SE	SSRB	DME	DM				Drive	Track	Head	Sector	Data Mark	Record Count	Destination <15:0>	Destination <31:16>				
Write	0D	W	SE	SSRB	DME	DM				Drive	Track	Head	Sector	Data Mark	Record Count	Source <15:0>	Source <31:16>				
Verify	0F	W	SE	SSRB	DME	DM				Drive	Track	Head	Sector	Data Mark	Record Count	Source <15:0>	Source <31:16>				
Format	07	W	SE	SSRB					Pat-tern	Drive	Track	Head			Track Count	Map Pointer <15:0>	Map Pointer <31:16>				
Relocate Track	0B	W	SE	SSRB						Drive	Track	Head			Alternate Track	Alternate Head					
Load Drive Parameter Block	00	W	SE	SSRB						Drive						Source <15:0>	Source <31:16>				
Dump Drive Parameter Block	03	W	SE	SSRB						Drive						Destination <15:0>	Destination <31:16>				
Read Physical Sector	0A	W	SE	SSRB	TV					Drive	Track	Head	Physical Sector			Destination <15:0>	Destination <31:16>				
Read ID	09	W	SE	SSRB	L					Drive	Track	Head	Physical Sector			Destination <15:0>	Destination <31:16>				
Load Buffer	01	W	SE	SSRB	DME					Drive						Source <15:0>	Source <31:16>				
Dump Buffer	02	W	SE	SSRB	DME					Drive						Destination <15:0>	Destination <31:16>				
Load Syndrome	04	W	SE	SSRB						Drive						Source <15:0>	Source <31:16>				
Dump Syndrome	05	W	SE	SSRB						Drive						Destination <15:0>	Destination <31:16>				
Correct Buffer	06	W	SE	SSRB	LD					Drive						Destination <15:0>	Destination <31:16>				
Seek	0E	W	SE	SSRB	TV					Drive	Track	Head									
Restore	08	W	SE	SSRB	TV					Drive											

Figure 9. IOPB Parameters

LOAD SYNDROME

The Reed-Solomon check bytes are transferred from SOURCE ADDRESS to the internal Syndrome RAM. This command generates an error if the Drive Parameter Block of the selected DRIVE specifies CRC or external ECC error-checking.

DUMP SYNDROME

The Reed-Solomon check bytes are dumped to the DESTINATION ADDRESS.

CORRECT BUFFER

This command uses the contents of the Syndrome RAM to correct the data in the internal sector buffer. It generates an error if the Drive Parameter Block of the selected DRIVE specifies CRC or external ECC error-checking. If the LOCATOR DUMP option is selected, the HDC additionally writes the location and values of errors sequentially to DESTINATION ADDRESS. If the buffer address is greater than the sector size and the error pattern is non-zero, then the error is uncorrectable for that locator. If the error pattern and the buffer address both are zero, then no error was detected by that locator. If the error pattern is zero and the buffer address is greater than the sector size, then the error occurred in the check bytes.

Head Movement Commands**SEEK**

The HEAD of the selected DRIVE is moved to the desired TRACK. If TRACK VERIFY is selected, the HDC looks at the first encountered header to determine whether it is on the right track. If the track numbers mismatch, the HDC reports an error. Usually, this command is issued only if implied and overlapped seeks are disabled.

RESTORE

RESTORE moves the heads of the selected DRIVE to track 0. This command synchronizes the HDC and the drives or recovers seek errors. The HDC supports two restore options. It can restore drives by issuing step-out pulses until the drive reaches track 0 and asserts TRK0. Optionally, drives with built-in restore logic may be restored by a pulse on the RTZ (Return To Zero) line. If TRACK VERIFY is selected, the HDC will also scan the header IDs to verify that the restore was successful.

Option Byte

One byte in each IOPB contains a set of options applicable to the particular command.

- W — WAIT
- 0 — After execution of current IOPB, continue with next IOPB.
 - 1 — Stop IOPB execution after terminating current IOPB.
- SE — STOP ON ERROR
- 0 — Option disabled.
 - 1 — Stop IOPB chain execution if current IOPB causes a Status Result block to be written.

SSRB — STOP ON STATUS RESULT BLOCK

- 0 — Option disabled.
- 1 — Stop IOPB chain execution if current IOPB causes a Status Result block to be written.

DME — DATA MAP ENABLE

- 0 — Data Mapping disabled.
- 1 — Data Mapping enabled. Source/Destination Address links to first Data Map Entry.

DM — DATA MARK

- 0 — Data Mark disabled.
- 1 — Data Mark enabled (see Normal Disk I/O Commands).

TV — TRACK VERIFY

- 0 — Track Verify disabled.
- 1 — Track Verify enabled (see Read Physical Sector and Seek).

L — LOCATOR DUMP

- 0 — Locator Dump disabled.
- 1 — Locator Dump enabled (see Read ID).

DATA MAPPING OPTIONS

The Data Mapping option lets the HDC process data stored in noncontiguous system memory. This option is available to five commands: Read, Write, Verify, Load Buffer, and Dump Buffer. It is enabled by setting the Data Map Enable bit (DME-bit) in the IOPB.

The last two words of the IOPB (Source/Destination Address) link to the first Data Map Entry (Figures 10 and 11). If this pointer is zero, then the Data Map does not exist and the HDC does not transfer data. Data Map Entries are linked together via the Data Map Pointer. The Data Map linked-list is terminated if the Data Map Pointer is set to zero. Each Data Map Entry defines a data buffer in system memory starting at the address defined by Data Source/Destination Address. The size of this buffer is defined by Byte Count. When Byte Count is set to zero, the HDC assumes a size of 2^{15} bytes. When the Load Enable (LE-bit) is reset to zero, the HDC masks off a data block with the size specified by Byte Count (Figure 12).

STATUS RESULT BLOCK (SRB)

The host CPU reserves a Status Result Area defined by the 32-bit Status Result Pointer register and the 16-bit Status Result Length Register. Whenever the HDC terminates a command and an error occurred, it adds a Status Result Block (Figures 13 and 14) to the Status Result Area. A Status Result Block carries the same unique ID number of the IOPB where the error occurred.

Multi-record Command Terminated

This SRB indicates that a Multi-record command has been terminated due to an error condition at the specified TRACK, HEAD, SECTOR, and RECORD COUNT.

No IDs Found On Track

A given Track was searched for an ID and none was found.

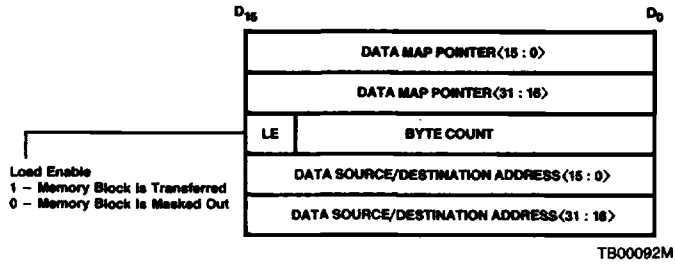


Figure 10. Data Map Entry

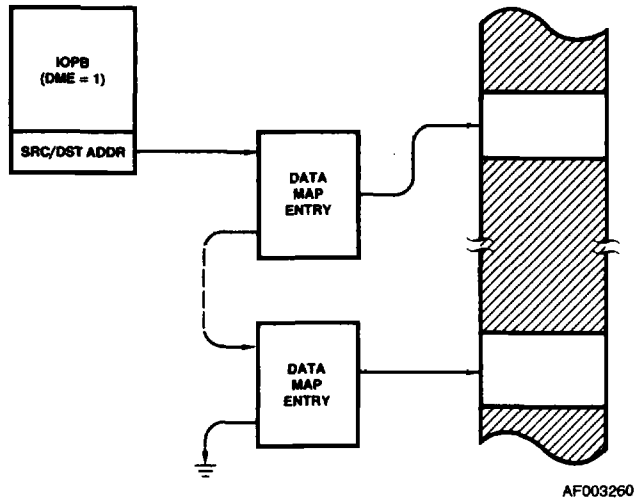


Figure 11. Data Map Entry Linked List

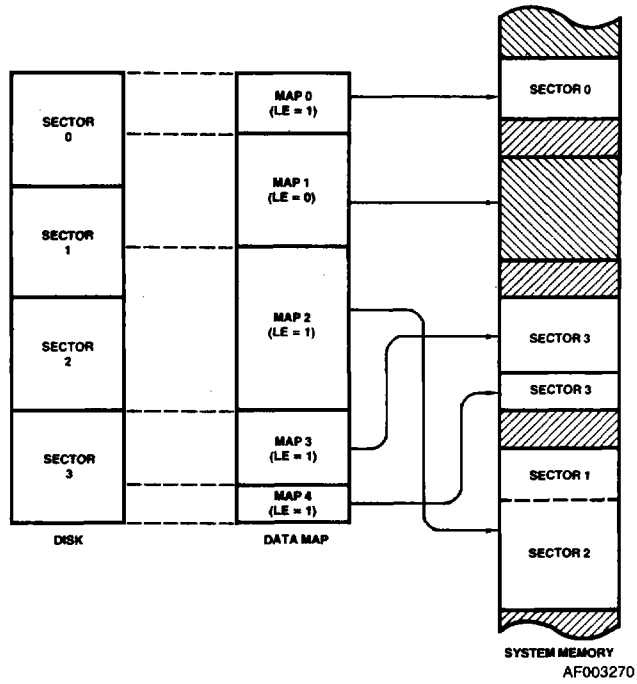


Figure 12. Data Mapping

D ₁₅	D ₀
Byte 1	Byte 0
Byte 3	Byte 2
Byte 5	Byte 4
Byte 7	Byte 6
Byte 9	Byte 8

Figure 13. Layout of Status Result Blocks

Status Result Block	Byte 1	Byte 0	Byte 3	Byte 2	Byte 5	Byte 4	Byte 7	Byte 6	Byte 9	Byte 8
Multirecord Command Terminated	ID		Record Count	Code ⁽¹⁾	Track		Head	Sector		
No IDs Found on Track	ID			01	Track		Head			
Format Error	ID			00	Track		Head			
Seek Error	ID			02	Current Track		Desired Track	Current Head	Desired Head	
Fatal Seek Error	ID			08	Current Track		Desired Track	Current Head	Desired Head	
Relocated Track	ID			05	Current Track		New Track	Current Head	New Head	
Relocated Track (No Vector)	ID			06	Track		Head			
Record Not Found	ID			09	Track		Head	Sector		
Record Not Found (ID Errors)	ID			07	Track		Head	Sector		
Multirecord Overflow	ID			0D	Track		Head	Sector		
Data Not Recovered	ID			17	Track		Head	Sector		
Data Recovered with Retries	ID		Retry Count	0A	Track		Head	Sector		
Data Recovered with ECC	ID		Retry Count	03	Track		Head	Sector		
Data SYNC Fault	ID			04	Track		Head	Sector		
Data Mark Error	ID		Data Mark	0E	Track		Head	Sector		
Sector Size Mismatch	ID		Sector Size	0F						
Data Non-Verify	ID			0B	Track		Head	Sector		
Physical Data Recovered with ECC	ID			Code ⁽¹⁾						
ECC Error Not Corrected	ID			Code ⁽¹⁾						
ECC Not Selected	ID			10						
ECC Error in Data Field	ID			18						
Data Mark Physical Error	ID		Data Mark	Code ⁽¹⁾						
ID CRC Error	ID			Code ⁽¹⁾						
Fault While Seeking	ID			12	Track					
Restore Fault	ID		Drive Status	16	Track					
Fault While Head Select	ID			13			Head			
Drive Selection Fault	ID		Drive Status	11						
Drive Status Trap	ID		Drive Status	Code ⁽¹⁾						
Data Timeout	ID			0C	Byte Count		Block Address <15:0>	Block Address <31:16>		
No Single Density Floppy Relocation	ID			14						
End of Data Map	ID			15						

(1) Note yet defined.

Figure 14. Status Result Blocks

Format Error

When reading or writing, it indicates that an Index Pulse occurred when not expected. When formatting, it indicates that the Index Pulse occurred before the format was completed. This means the number of sectors times the sector size is too large for the track.

Seek Error

The HDC has read a valid ID showing that the current TRACK/HEAD differs from the expected TRACK/HEAD.

Fatal Seek Error

After a seek error, the HDC has performed a restore and a second seek, but the seek error still persists. The IOPB is aborted.

Relocated Track

A track was read as relocated and the HDC auto-vectored to the new track.

Relocated Track (No Vector)

A track was read as relocated, but the HDC could not find a valid data field to read the vector. The IOPB is aborted.

Record Not Found

No ID was found corresponding to the desired sector number.

Record Not Found (ID Errors)

Sector was not found, but one or more IDs had CRC errors.

Multi-record Overflow

The HDC aborted a Multi-record command because the last sector of a track was read and the programmed Multi-Record Policy prohibits a track/head increment.

Data Not Recovered

The HDC could not recover a sector requested by a read command.

Data Recovered with Retries

Data was recovered using read retries (RETRY COUNT).

Data Recovered with ECC

The Reed-Solomon successfully corrected a read error. Retry Count specifies the number of retries performed before the error was corrected.

Data Sync Fault

The HDC successfully read the ID for the desired sector, but could not find an Address Mark for the data field.

Data Mark Error

The Data Mark read did not correspond to the Data Mark specified by the Drive Parameter Block.

Sector Size Mismatch

Sector Size read from the Header field does not match the Sector Size defined in the Drive Parameter Block (floppy formats only).

Data Non-Verify

The Verify command detected a mismatch between disk and memory data.

Physical Data Recovered with ECC

The Read Physical Sector command had to use ECC to correct the data field.

ECC Error Not Corrected

The data transferred to system memory by Read Physical Sector contained uncorrected errors.

ECC Not Selected

Error correction attempted when ECC was not selected internally.

ECC Error in Data Field

An error was detected in the data field of a sector.

Data Mark Physical Error

The Data Mark read by Read Physical Sector did not correspond to programmed Data Mark.

ID CRC Error

A CRC error was detected when reading the ID field by the Read ID command.

Fault While Seeking

While seeking, the FAULT line was asserted or the SEEKCOM line was not asserted.

Restore Fault

The HDC could not restore the drive.

Fault While Head Select

The HDC could not select the specified head. The FAULT line was asserted or SEEKCOM was not asserted (for floppy disk drives only).

Drive Selection Fault

A fault occurred when selecting a drive. The Drive Status byte latches the levels of the status lines when the fault occurred:

D₉ = DREADY
 D₁₀ = FAULT
 D₁₁ = SEEKCOM
 D₁₂ = WRPROT
 D₁₃ = TRK0

Drive Status Trap

An unexpected change in state of one or more drive status lines occurred while the drive was selected. The Drive Status byte latches the status lines. The IOPB is aborted.

Data Time-out

A memory time-out occurred while accessing the system memory. The Block Address defines the starting location of a block of system memory where the time-out occurred. Byte Count defines the length of the block.

No Single-Density Floppy Relocation

A Relocate Track command was attempted on a single-density floppy disk drive.

End Of Data Map

Unexpected end of Data Map encountered.

DISK DATA I/O**Sector Formats**

Data is stored on the disk in sectors. Each sector consists of two fundamental parts: the header and the data field. The sizes of all pads, gaps, preambles, postambles, and data fields are programmable in the Drive Parameter Block. Floppy disk formats also have an Index field at the beginning of each track.

Header

The header contains the Address Mark, the track number, the head number, and the sector number (Figure 16). Two trailing CRC check bytes protect the header. The beginning of the header is marked by an ID Address Mark (IDAM). The single-density floppy format requires a single-byte address mark while the double-density floppy and hard disk formats use a two-byte address mark. The first byte (the only byte for single-density floppy formats) of the address mark is a unique clock/data pattern written and detected by the data separator. Since the unique clock/data pattern is written by the disk data separator, its length and layout are transparent to the HDC. The second byte, which is processed by the HDC, specifies that this is a normal (FEH) or a relocated (FDH) track. This byte is not present for single-density floppy formats. A preamble and a postamble compensate for speed and mechanical variations of the disk system. The length of both fields is user-programmable.

Data Field

A Data Mark similar to the header's ID Address Mark marks the beginning of the data field (Figure 17). The single-density floppy format uses a single-byte Data Mark which is different from the Address Mark. The data field can be marked by two types of data marks to specify either a normal data field or a deleted data field. The double-density floppy and the hard disk

formats have a two-byte Data Mark consisting of a unique clock/data pattern similar to the Address Mark and a user-programmable Data Mark byte.

The data field has a user-programmable length of 128, 256, or 512 bytes. It is protected by one of three user-selectable data protection algorithms: CRC-CCITT (error detection), Single-Burst or Double-Burst Reed-Solomon (error detection and correction). Optionally, external error processing logic can be interfaced for hard disk format to implement any user-designed algorithm. The check bytes are stored in the ECC field. For external error processing, the user-designed external error processing logic reads and writes the ECC field. The number of ECC bytes appended varies from 2 to 15 bytes for the internal ECC options and 1 to 256 bytes (determined by the drive parameter block) for external ECC.

Data Separator Interface Signals

The data lines (RDDAT and WRDAT) transfer the data to and from the disk. The transfer is controlled by five signals: INDEX, AMC, AMF, RG, and WG. The FAM/ECC<1:0> and FAMD/ECCERR lines interface with external hardware to allow user-definable error-detection/correction. For floppy formats, these lines interface with the data separator to allow address/data mark detection and generation.

Header Search Mechanism

The unique clock/data patterns of the address/data marks are written and detected by the data separator only. When the HDC attempts to read a header or to access a data field, it activates Address Mark Control (AMC).

For floppy formats, the FAM/ECC<1:0> outputs differentiate between the various index, address, and data marks defined by the IBM Single- and Double-density Format. Whenever the HDC activates the AMC line to read or write a special mark from a floppy disk, the data separator should use the FAM/ECC<1:0> to determine the unique clock/data pattern to read or write. Additionally, for single-density floppy formats, the

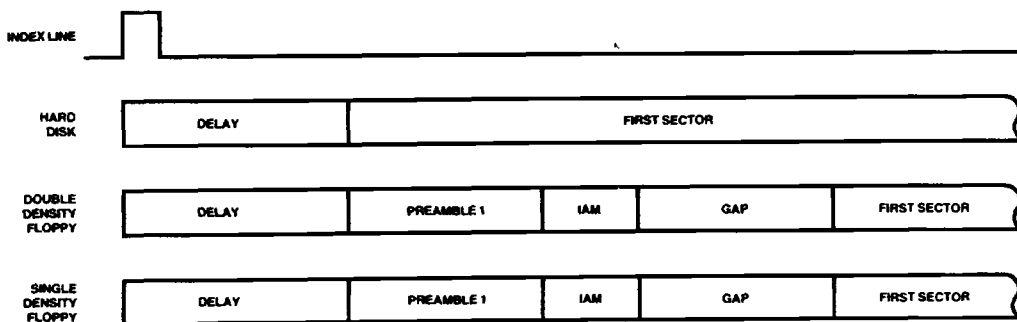
FAMD/ECCERR pin indicates that a deleted data address mark should be written or read.

Next, the HDC activates Read Gate (RG) and waits for the data separator acknowledge. The data separator should assert Address Mark Found (AMF) when it detects an address/data mark. The rising edge of AMF indicates that valid data will be on the RDDAT pin on the next rising edge of the RD/REF CLK (see Figure 23). For double-density floppy and hard disk formats, the HDC checks the next eight bits for an FDH or FEH. If the check fails, a data address mark was found; the HDC deactivates AMC and RG. After AMF becomes inactive, AMC is reasserted then followed by RG, and the whole procedure is repeated until a header is found or it is determined that no header can be found (indicated by three index pulses). For single-density floppy formats, the rising edge of AMF indicates that a header address mark has been found.

After finding a valid header address mark, the HDC compares the next 48 bits (6 bytes) of serial data with the track, head, and sector number of the desired sector (and sector size for floppy formats) to determine if the right header has been found. A CRC check ensures the correctness of the header information. If the track or the head numbers recovered from the header do not match the desired track or head number, an error is flagged and the command is aborted. For floppy formats, sector size is also checked against the sector size defined for the current drive. The sector number is checked to see if this is the desired sector.

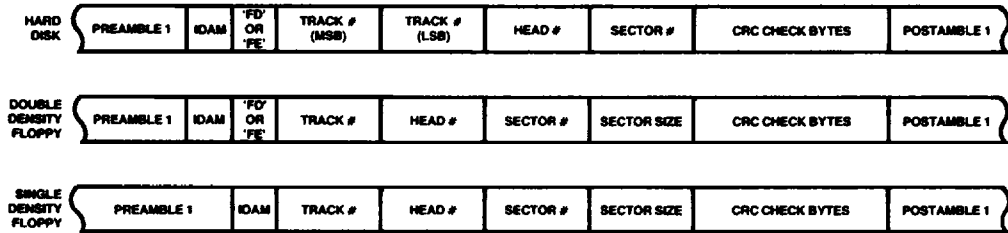
If the correct sector number was not found, then the process is started all over again until either the desired sector is found or the HDC determines that the sector cannot be found on the current track. If three index pulses are detected (indicating two or more disk revolutions), the Sector Not Found error is flagged.

If the correct sector number was found, the search for the data mark begins.



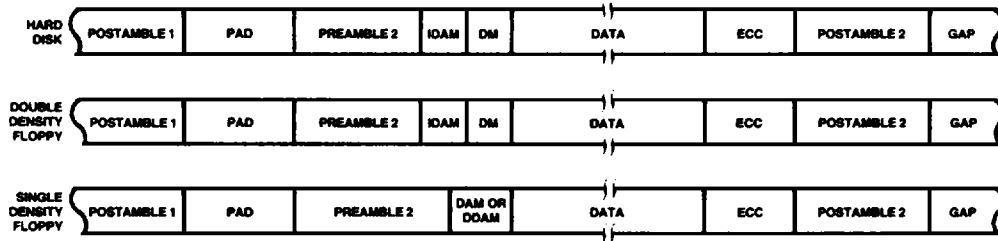
DF003810

Figure 15. Track Initialization Field



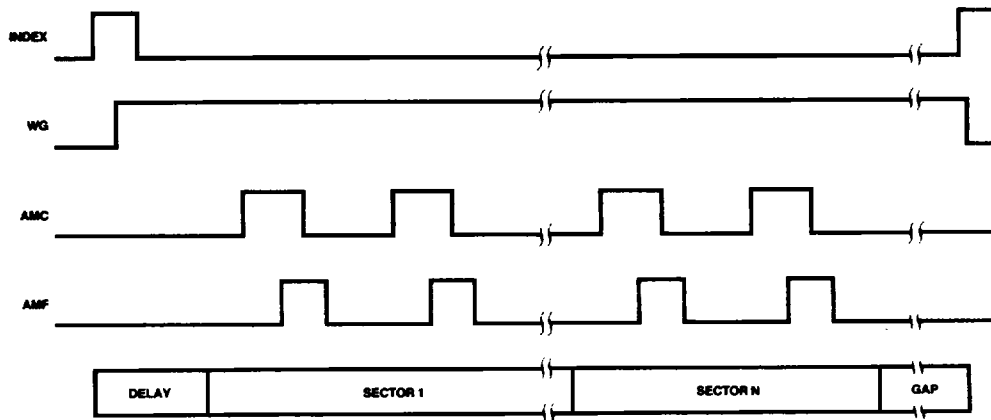
DF003820

Figure 16. Sector Header Formats



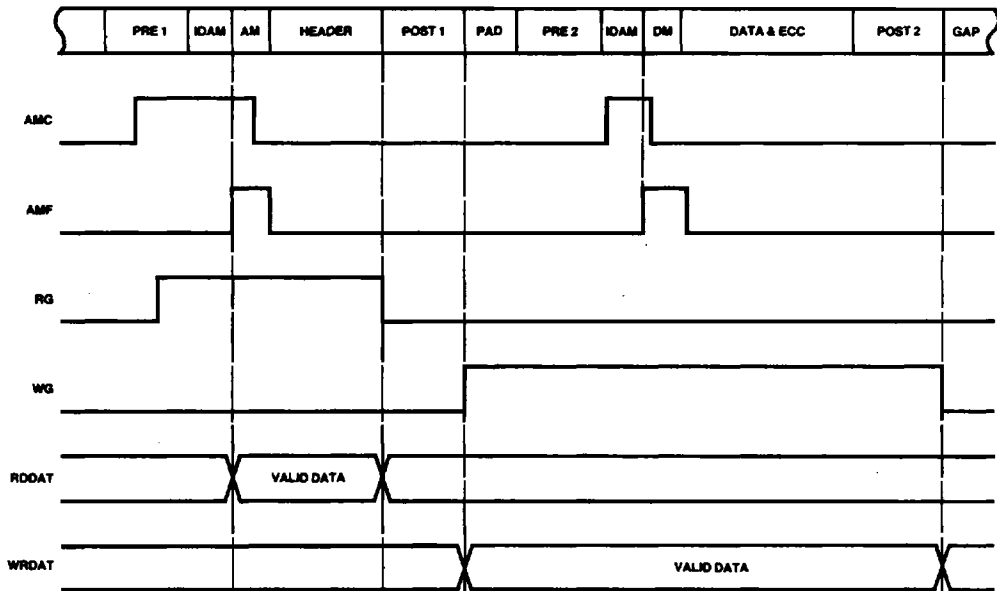
DF003830

Figure 17. Sector Data Fields Format



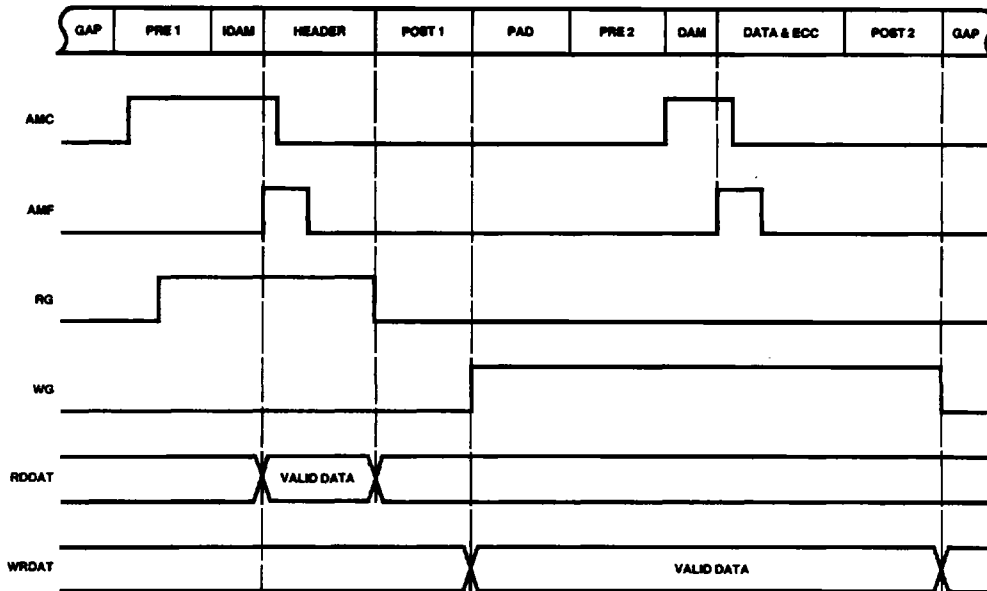
DF003840

Figure 18. Write Track Sequence



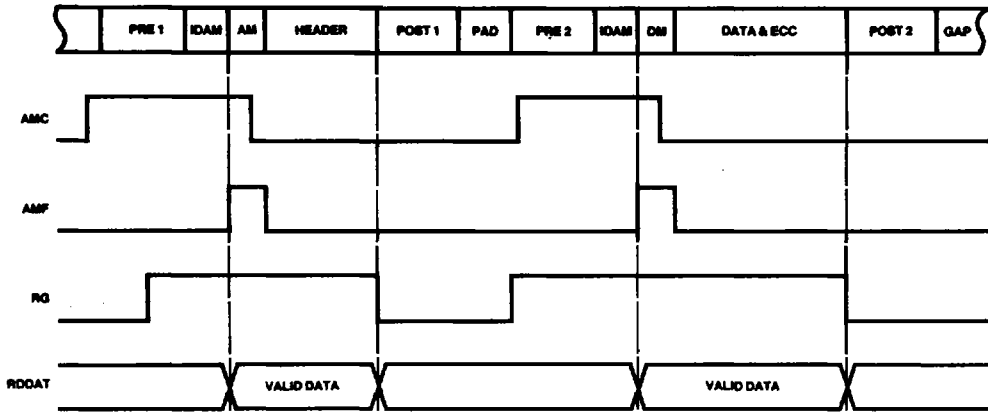
WF008161

Figure 19. Write Sector Control Sequence
(For Hard Disk and Double-Density Floppies)



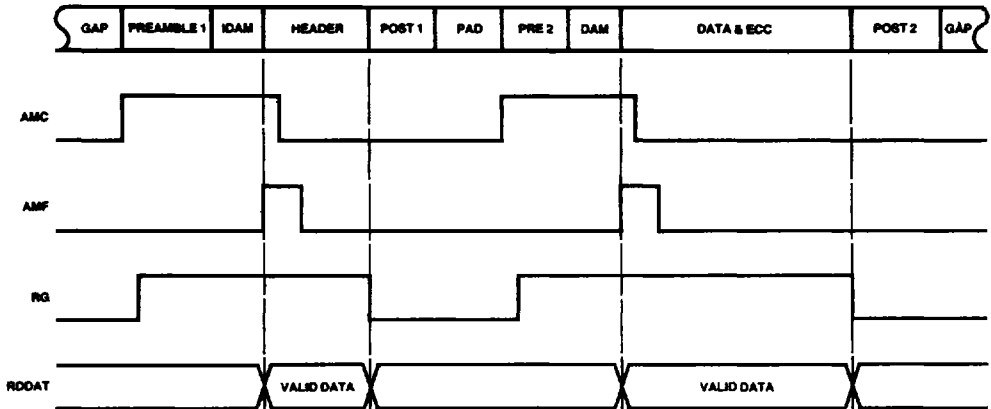
WF008170

Figure 20. Write Sector Control Sequence
(For Single-Density Floppies)



WF008181

**Figure 21. Read Sector Control Sequence
(For Hard Disks and Double-Density Floppies)**



WF008190

**Figure 22. Read Sector Control Sequence
(For Single-Density Floppies)**

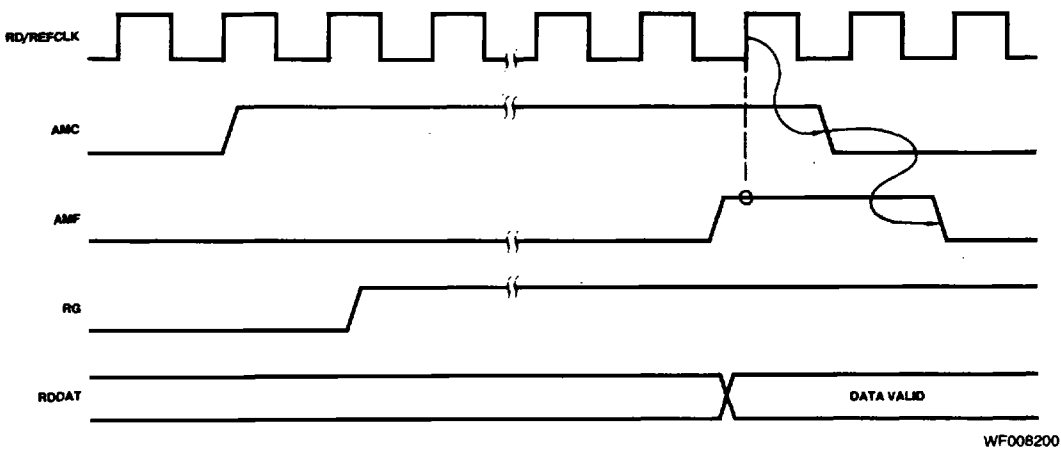


Figure 23. Address Mark Control/Address Mark Found Handshake (Read Data)

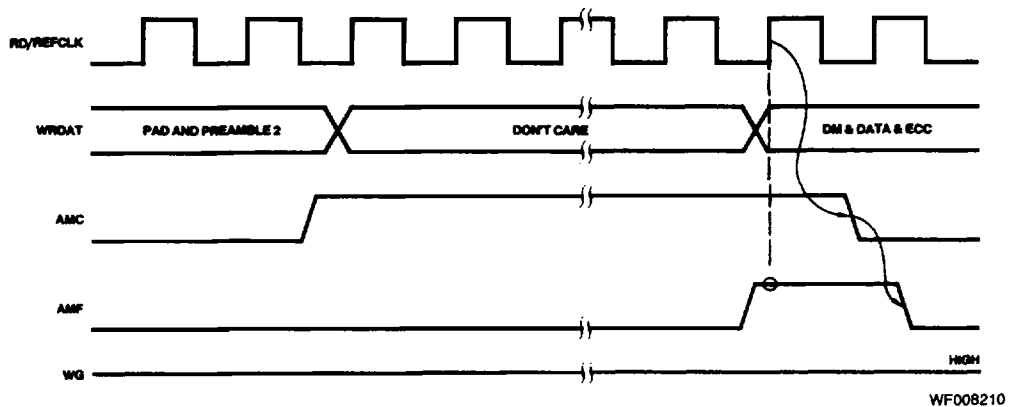


Figure 24. Address Mark Control/Address Mark Found Handshake (Write Data)

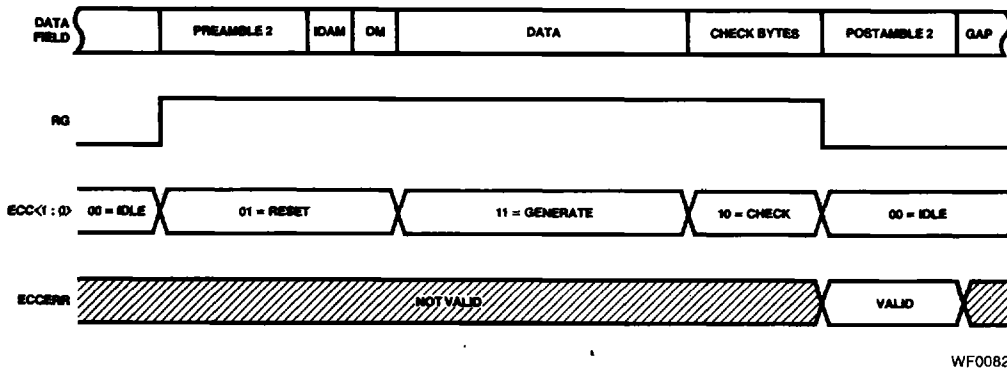


Figure 25. External ECC Handshake
(Read Data)

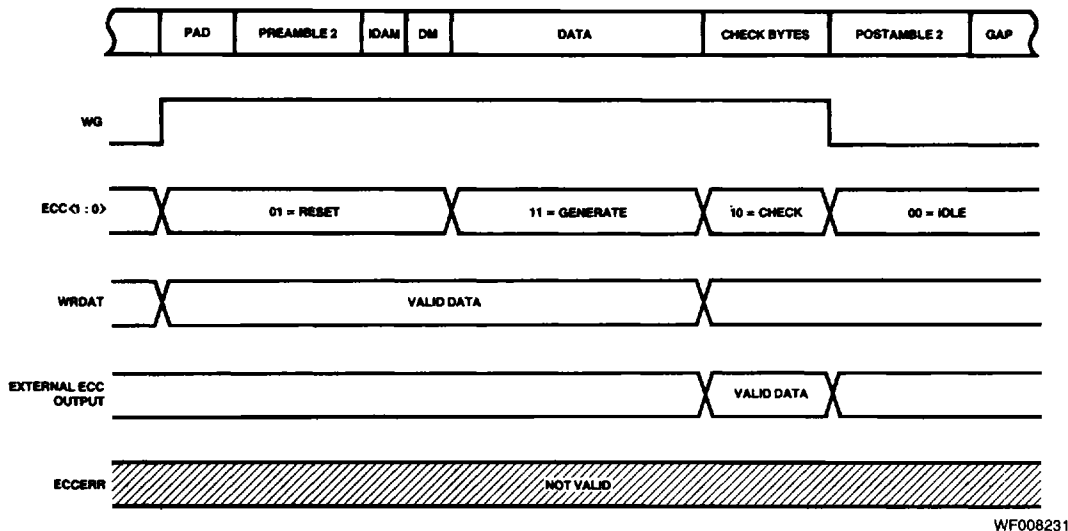


Figure 26. External ECC Handshake
(Write Data)

Data Field Read

The HDC uses the same handshake procedure outlined above to search for the data address mark. For double-density floppy and hard disk formats, the HDC compares the byte following the data address mark to the programmed data mark to confirm that the data field has been found. The HDC reads the data field into the sector buffer and the ECC bytes into the error logic. For hard disk formats, the HDC ignores the ECC field if external ECC is selected. The external error processing logic should read the ECC field to verify the integrity of the data field. FAM/ECC<1:0> and FAMD/ECCERR control the external error logic handshake. Immediately after the ECC field has been read, RG is turned off and the sector-read operation is terminated.

Data Field Write

Sector-write commands proceed similarly to sector-reads while searching for the desired sector. After finding the desired sector header, the subsequent data field and ECC field, including pad, preamble2, data address mark and postamble2 are overwritten. The HDC activates Write Gate (WG) at the beginning of the pad. Write Data on WRDAT line is valid with the next rising edge of the clock. First, the HDC writes the pad and preamble2 fields. On completion of preamble2, AMC is activated. For floppy formats, FAM/ECC<1:0> indicates to the data separator the data address mark to write. The data separator should assert AMF after writing the last data address mark bit. The HDC resumes data output with the next clock. For double-density floppy and hard disk formats, the HDC writes a user-programmable data mark first. Next the

data field is output on the WRDAT line. Depending on the selected ECC mode, either the HDC or the external error logic appends the check bytes to the data field. FAM/ECC<1:0> and FAMD/ECCERR control the external error logic handshake. WG is turned off after the postamble2 field is written. This completes the write-sector sequence.

Format Track

Format Track always writes the entire track. It is the only command that writes the sector header. Beginning with the rising edge of the INDEX pulse, the HDC asserts WG and outputs the pattern for the delay field (Figure 18). Note that disk drives require that the delay field be wider than the INDEX pulse width. For floppy formats, an Index Address Mark (IAM) field follows the delay field. Then the HDC starts writing sectors.

For writing the headers, the HDC uses the track, head and sector size information supplied by the format IOPB. A sector map in the system memory supplies the logical sector number sequence. The first byte of the sector map is written in the sector number field of the first physical sector. The second byte is written in the second physical sector. This process continues until the required number of sectors have been formatted. For multiple track format commands, the sector maps for the tracks to be formatted are organized in a linear list in the system memory. The Map Pointer of format IOPB points to the beginning of this sector map list.

For writing address/data marks, the HDC proceeds as described in the section "Data Field Write." The data field is filled with the user-supplied pattern byte in the format IOPB. The gap between the end of the last sector and the rising edge of the index pulse is filled by the gap pattern. The length of this gap field depends on the track capacity and the number of sectors/track. It is different from the intersector gap which has a user-definable length. The patterns written for all fields are shown in the table below.

Field	Single-density floppy formats	Double-density floppy and hard disk formats
Delay	FFH	4EH
Preamble1	00H	00H
Postamble1	FFH	4EH
Pad	00H	00H
Preamble2	00H	00H
Postamble2	FFH	4EH
Gap	FFH	4EH

DRIVE PARAMETER PROGRAMMING (Figure 27)

The HDC contains one set of Drive Parameter Registers for each drive. The system can only access this register set indirectly by either of the following commands: Load Drive Parameter Block and Dump Drive Parameter Block. The block is set up in contiguous system memory. Byte values in this table, when set to zero, represent the value 256.

General Select Byte (Figure 28)

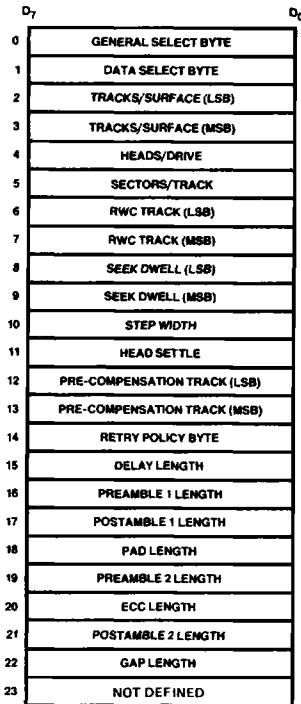
The EDCP field determines which of the error-checking algorithms the HDC should use to recover marginal data. The Auto Vector Enable bit (AVE) allows the HDC to vector automatically to the new track if a given track is found to be relocated. This bit is ignored for single-density floppy formats. The Multi-Record Policy (MRP) field determines the policy followed for multiple sector transfers. Multi-record commands may require that the HDC select a new track to access subsequent sectors. One option is to increment the head number. If the head number overflows, the HDC resets it to zero and increments the track number. If the track number overflows, it is reset to zero. The second option allows the track number to be incremented first. On overflow, the head number is incremented. The RTZEN bit defines the recalibration mode (move head to track 0). The HDC can either assert the RTZ pin (16 clock cycles active) or issue STEP pulses until TRK0 becomes active. The maximum number of STEP pulses for recalibration is 65535.

Data Select Byte (Figure 29)

The DSZE field defines the size of the data field for a particular drive.

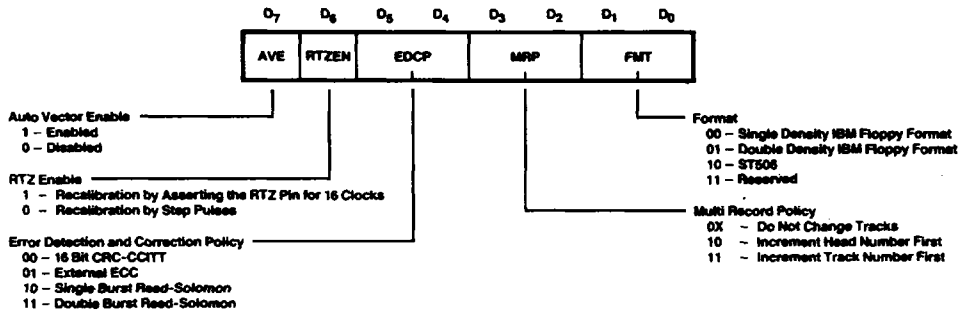
Retry Policy Byte (Figure 30)

The most significant three bits define the error-checking policy. These bits are ignored if CRC or external ECC is used. If ECC Before Retry is selected, the HDC uses ECC even when retry attempts are disabled. The RE-bit enables the number of retry attempts defined by Retry Count (RC).



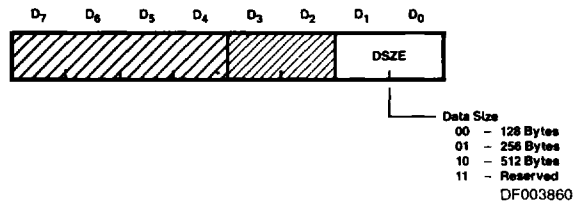
DF003851

Figure 27. Drive Parameter Block



DF003870

Figure 28. General Select Byte



DF003860

Figure 29. Data Select Byte

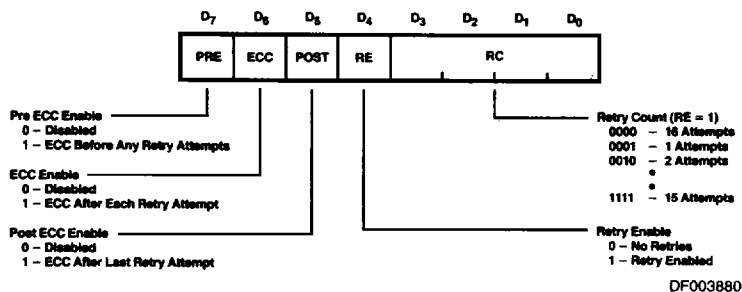


Figure 30. Retry Policy Byte

Drive Parameters

Tracks/Surface specifies the number of cylinders (tracks) in the range from 0 to 65536. Head/Drive specifies the number of moving heads (1 to 256). However, only the four least significant bits are output at the head select pins. Sectors/Track defines the number of sectors per track (1 to 256). RWC Track specifies the track number where the Reduced Write Current pin should be activated (only for ST506 and floppy formats). If the current track number is greater than RWC Track, the pin (RWC) is activated. Pre-Compensation Track specifies the track where the pre-compensation starts.

Seek Timing

Step Width (8-bit) determines the width of step pulses. Seek Dwell (16-bit) sets the delay between the falling edge and the rising edge of step pulses. If either Step Width or Seek Dwell is set to 1, then the step cycle is equal to 18 system clocks (50% duty cycle). If neither of these values is 1, then the Step Width is equal to $13 \times (\text{Step Width} + 8)$ and the dwell time is equal to $17 + (\text{Seek Dwell} \times 8)$. Head Settle defines the time to allow the heads of the selected drive to settle, after the head select lines change, in increments of 4 clock cycles.

Sector Format

The sector format parameters specify the sizes of particular sector header and data fields.

DISK DATA PROTECTION

All data stored on disk is protected by error-checking algorithms. The HDC supports four modes:

- 16-bit CRC-CCITT (error detection)
- Single-Burst Reed-Solomon (single-burst correction)
- Double-Burst Reed-Solomon (double-burst correction)
- External ECC

The error-checking scheme for each drive is defined by the EDCP field in the General Select Byte of the Drive Parameter Block. It is possible to use a different ECC for each sector or track provided that the Drive Parameter Block is constantly changed. However, this is not a recommended procedure.

CRC-CCITT

The CRC-CCITT code is a cyclic-based, error-detecting/non-correcting code. It is the industry standard error checking code for magnetic disk systems. CRC-CCITT is mandatory for the

protection of the sector ID field, but the data field can be protected by any of the four modes mentioned above. The CRC generator polynomial is:

$$x^{16} + x^{12} + x^5 + 1$$

The guaranteed capabilities of the code are listed below:

- Detects all odd number bit errors
- Detects all single-burst errors of 16 bits or less
- Detects all single, double, and triple bit errors

Single-Burst Reed-Solomon

The HDC supports two error correction codes, Single-Burst Reed-Solomon and Double-Burst Reed-Solomon. Single-Burst Reed-Solomon corrects single-burst errors and detects double-burst and some triple-burst errors. A single burst of errors is defined as any number of bit errors (contiguous or noncontiguous) where the distance between the first and the last bit error does not exceed the burst length given in the table below. The ECC code protects the check bytes as well as the data. The guaranteed performance of the Single-Burst Reed-Solomon code is shown below.

Sector Size (# of bytes)	Detection Capability (# of bits)		Correction Capability (# of bits)		# of Check Bytes
	Single Bursts	Double Bursts	Single Bursts	Double Bursts	
128	33	9	9	0	6
256	33	9	9	0	6
512	57	17	18	0	9

This table shows, for instance, that in a sector of 256 bytes any single burst of errors with a length of up to 33 bits will be detected. Note, that two single bit errors separated by more than 32 bits will count as a double-burst error. Alternatively, any two random single-bursts (double-burst) of up to 9 bits each will be detected also. In this example, this code can correct a single burst of errors up to 9 bits and cannot correct double-burst errors. The table presents the guaranteed capabilities of this code. Under certain circumstances the code is capable of detecting longer bursts or even triple-burst errors.

Double-Burst Reed-Solomon

Double-Burst Reed-Solomon is an enhanced version of Single-Burst Reed-Solomon. This code can detect and correct single- and double-burst errors of the maximum size listed in the following table.

2

Sector Size (# of bytes)	Detection Capability (# of bits)		Correction Capability (# of bits)		# of Check Bytes
	Single Bursts	Double Bursts	Single Bursts	Double Bursts	
128	49	16	25	9	10
256	49	16	25	9	10
512	81	24	41	17	15

External ECC

The HDC features external ECC to allow schemes other than CRC-CCITT or Reed-Solomon. External ECC can only be used for the protection of data fields. Three lines (ECC < 1:0 > and ECCERR) simplify interfacing the external ECC hardware. ECC < 1:0 > present the status of the HDC to allow the external ECC to run synchronously. The status is coded in Gray code; only one bit changes when going from one state to the next (Figure 26).

In the IDLE state, no data field of a sector is written or read. The external ECC should be inactive.

RESET should reset the external ECC to prepare itself for an ECC process. At the end of the data mark, while reading or writing the last bit, the status lines change into the GENERATE state.

On the next rising edge of the RD/REF CLK, the external ECC must be prepared to receive valid data on either the RDDAT or WTDAT lines (depending on whether RG or WG is asserted). The external ECC must generate the check bytes. When reading or writing the last bit of the data field, the lines change to the CHECK state.

CHECK enables the external ECC to either multiplex the check bytes on WRDAT (WG active) or to compare the generated check bytes with the bytes read from RDDAT (RG active). With the external ECC, a programmable number of check bytes can be added to the data field of a sector (1 to 256 bytes).

On completion of the check byte field, at the last bit of the last check byte, the status lines change back to the IDLE state. On the next rising edge of the RD/REF CLK, the IDLE state will be in effect. During the last byte of the Postamble2 field following the check bytes, the ECCERR pin will be sampled by the HDC for an "Error Found" signal from the external ECC. If the ECCERR pin is not asserted (LOW), then the HDC assumes that the data is valid. If the ECCERR line is asserted (HIGH), then the HDC assumes that an error occurred in the data field.

INTERFACING

System Interface

For both Slave Mode and Master Mode, the system bus interface can be programmed for byte (B/W High) or word (B/W Low) transfers as shown in Figure 5.

Slave Mode

In Slave Mode, the host CPU can access the five internal registers of the HDC. A₀ to A₃ indicate the address of the internal register (Figure 4). In Byte Mode, the High byte is accessed if A₀ is HIGH and the Low byte is accessed if A₀ is LOW. In Byte Mode, BHE is ignored. The HDC asserts READY to indicate that it is ready to complete the access.

Master Mode

The HDC is in Master Mode when it controls the system bus. To request the mastership on the system bus, the HDC asserts Bus Request (BREQ). The bus is granted to the HDC when Bus Acknowledge (BACK) is active. The HDC keeps BREQ asserted until it releases the bus after finishing a DMA burst of programmable length or when the burst is preempted by removing BACK.

A byte transfer occurs in Word Mode when only one byte remains to be transferred or when the system address is odd. The throttling of DMA transfers on the system bus is controlled by the Mode Register. The HDC inserts a programmable number of software Wait States into the DMA bus cycle. Additionally, it inserts hardware Wait States until the memory asserts READY.

Upper Address Latch Enable (ALEN) may latch the upper address word (A₁₆ to A₃₁) in an external address latch. The upper address is only updated if a change demands this update.

Interrupts

The HDC interrupts the host CPU when it has completed the initialization procedure executed after a hardware or software reset or when it has completed a command chain. The initialization interrupt cannot be disabled. The interrupt on command chain completion can be enabled or disabled by the Interrupt Mask bit in the Mode Register.

Disk Control Interface

The Disk Control Interface selects drives and heads and controls the head positioning. It is programmable either to provide a floppy disk type of interface or to conform with the ST506/412 drive interface standard.

Drive Selection

Drives are deselected when SELEN is HIGH. The two bits DRIVE < 1:0 > select one of up to four drives. DRIVE < 1:0 > are valid when SELEN is LOW. SELEN remains LOW as long as the drive is selected. The selected drive acknowledges the selection by activating DREADY. If SELEN is not acknowledged within 2¹⁶ clocks, then the HDC assumes that the selected drive is not present and generates a time-out error. If FAULT is asserted after activating DREADY, then the HDC deselects the drive and generates a fault error.

Head Positioning

Seek operations are performed via the lines STEP, DIRIN, SEEKCOM, RTZ, and TRK0. Normal seeks pulse the STEP line to move the head to the desired track. Restore may pulse the STEP or RTZ line to move the head to track 0. DIRIN specifies the direction in which the head should move on SEEK pulses.

SEEKCOM is asserted by the drive to indicate that the head has moved to the desired track. Once the drive has acknowledged the completion of a seek by activating SEEKCOM, it must keep SEEKCOM active as long as it is selected or until it receives another seek command; otherwise the HDC issues a drive fault error. When executing the restore or seek commands, the drive must acknowledge the first STEP pulse or the RTZ pulse (SEEKCOM pulsed LOW) within 2¹⁶ clocks or the HDC will generate a seek error.

Write Protect

The Write Protect line is sampled just prior to execution of a WRITE or FORMAT command. If the line is HIGH, the command is aborted.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Supply Voltage to Ground	
Potential Continuous	-0.5 to +7.0V
DC Voltage Applied to Outputs	
for High Output State	-0.5V to +V _{CC}
DC Input Voltage	-0.5 to +7.0V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

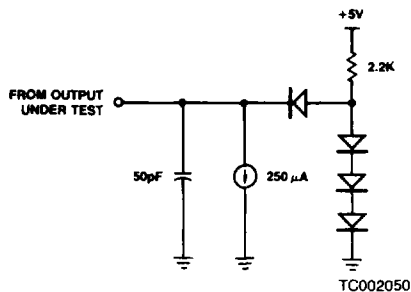
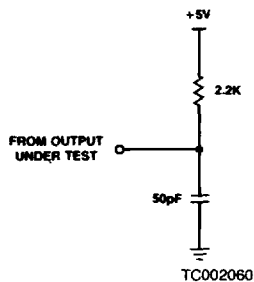
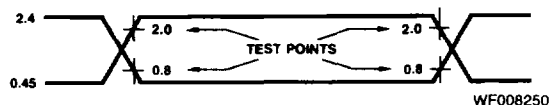
Part Number	T _A	V _{CC}	V _{SS}
Am9580 PG	0°C to 70°C	5V ±5%	0V
Am9580 LC			

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

Parameters	Description	Test Conditions	Min	Max	Units
V _{IL}	Input Low Voltage		-0.5	0.8	V
V _{IH}	Input High Voltage		2.0	V _{CC} + 0.5	V
V _{OL}	Output Low Voltage	I _{OL} = 3.2mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -250µA	2.4		V
I _I	Input Leakage Current	V _{SS} ≤ V _I ≤ V _{CC} ± 1.0		±10	µA
I _O	Output Leakage Current	V _{CC} ≤ V _O ≤ V _{SS} ± 1.0		±10	µA
I _{CC}	Supply Current				mA
C _{IN}	Input Capacitance	Unmeasured Pins Returned to Ground. f = 1MHz Over Specified Temperature Range			pF
C _{OUT}	Output Capacitance				pF
C _{I/O}	Bidirectional Capacitance				pF

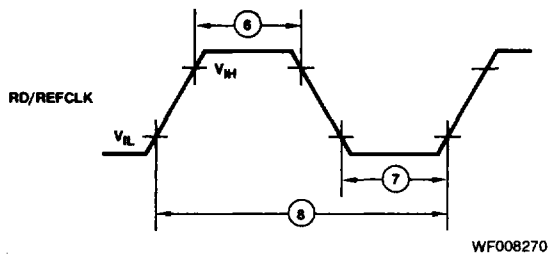
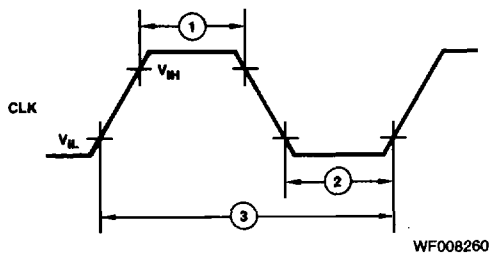
2

Standard Test Conditions**Standard Test Load****Open Drain Test Load****Switching Test Input Waveform**

SYSTEM CLOCK AND RD/REFCLK

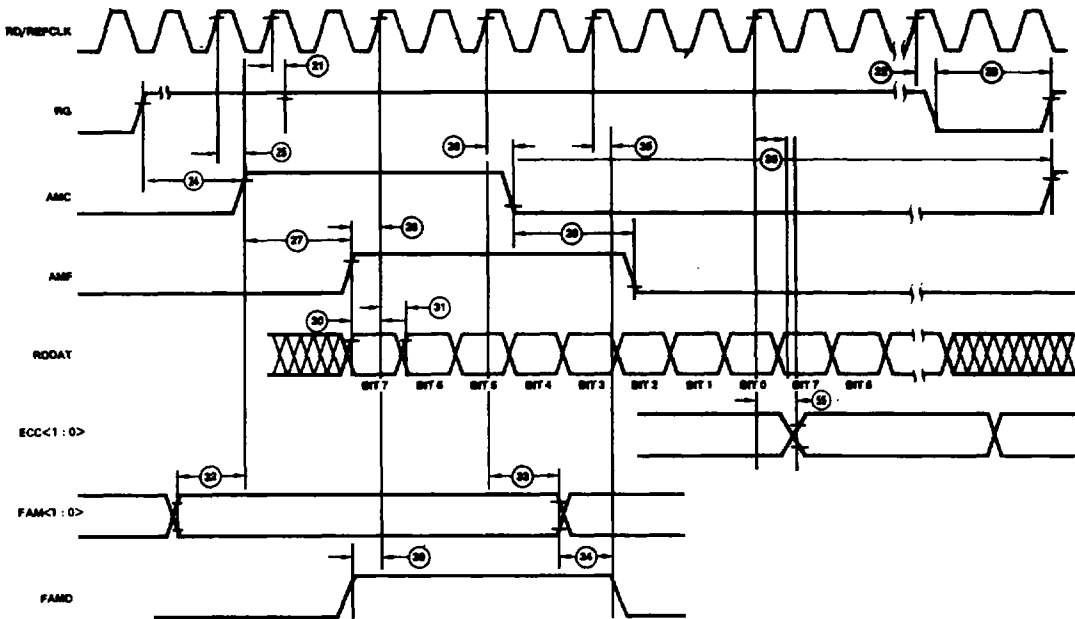
Number	Parameters	Description	Min	Max	Units
1	t _{CPH}	System Clock High Time	3		ns
2	t _{CPL}	System Clock Low Time	3		ns
3	t _{CPC}	System Clock Cycle Time	100	1000	ns
6	t _{DCPH}	Disk Clock High Time	30		ns
7	t _{DCPL}	Disk Clock Low Time	30		ns
8	t _{DCPC}	Disk Clock Cycle Time	83	1000†	ns

† Can be static if no drive selected.



DISK DATA READ

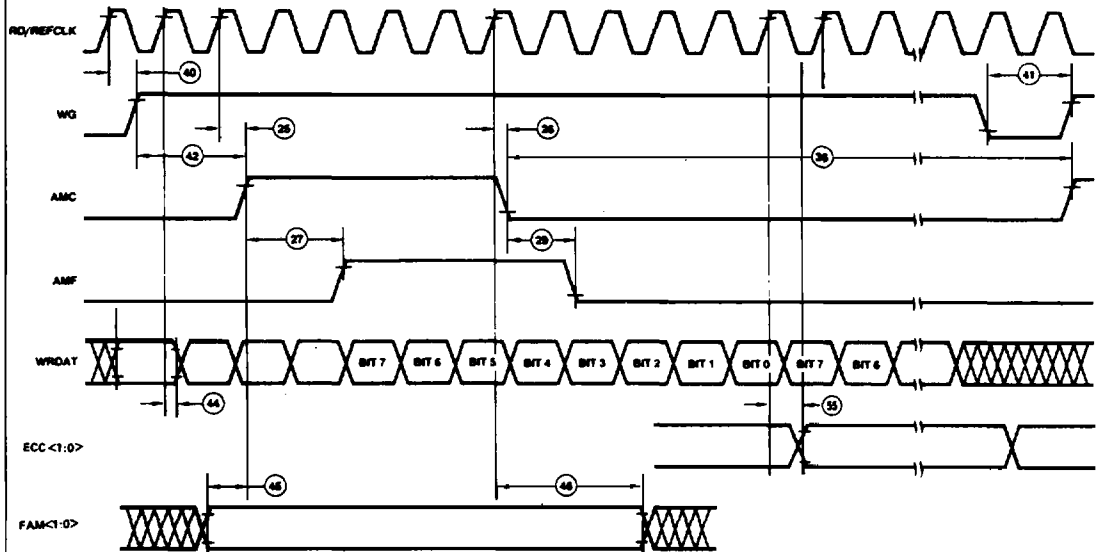
Number	Parameters	Description	Min	Max	Units
21	tDRGA	RD/REFCLK to RG Active	0	50	ns
22	tDRGI	RD/REFCLK to RG Inactive	0	50	ns
23	tRGDW	RG Dwell	8 tDCPC		ns
24	tAMCRG	RG to AMC	8 tDCPC		ns
25	tDAMCA	RD/REFCLK to AMC Active	0	50	ns
26	tDAMCI	RD/REFCLK to AMC Inactive	0	50	ns
27	tAMCAMF	AMC Active to AMF Active	tDCPC		ns
28	tSUAMF	AMF Setup to RD/REFCLK	30		ns
29	tDAMCAMF	AMC Active to AMF Inactive	0	16 tDCPC	ns
30	tDATSCC	Data Setup to RD/REFCLK	30		ns
31	tDAMH	Data Hold to RD/REFCLK	0		ns
32	tUFAMF	FAM <1:0> Setup to AMC Active	30		ns
33	tUFAM	FAM <1:0> Hold to RD/REFCLK	0		ns
34	tUFAMD	FAM <1:0> Change to FAMD Inactive	0		ns
35	tDFAMDI	RD/REFCLK to FAMD Inactive	0		ns
36	tAMCDW	AMC Dwell	8 tDCPC		ns
39	tSUFAMD	FAMD Setup to RD/REFCLK	30		ns



WF008281

DISK DATA WRITE

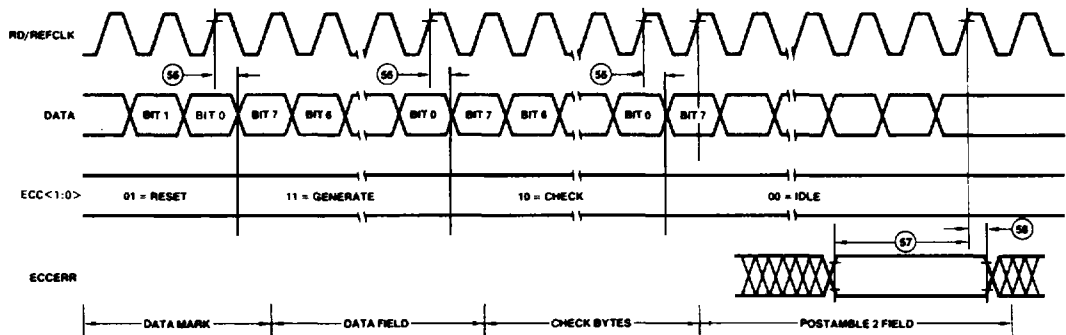
Number	Parameters	Description	Min	Max	Units
40	t _{DWG}	RD/REFCLK to WG Active		50	ns
41	t _{WDW}	WG Dwell		80	ns
42	t _{DWGAMC}	WG to AMC Active		80	ns
44	t _{HDWD}	RD/REFCLK WRDAT	0	50	ns
45	t _{SUFAM}	FAM <1:0> Set-up to AMC	t _{DCPC} - 50		ns
46	t _{HDFAM}	FAM <1:0> Hold to AMC Inactive	0		ns



WF008291

EXTERNAL ECC INTERFACE

Number	Parameters	Description	Min	Max	Units
55	t _{DECC}	RD/REFCLK to ECC<1:0>		50	ns
57	t _{ERRSU}	ECC<1:0> to Last RD/REFCLK		t _{DCPC}	ns
58	t _{ERRHD}	ERR Hold to Last RD/REFCLK (In Post 2)	0		ns



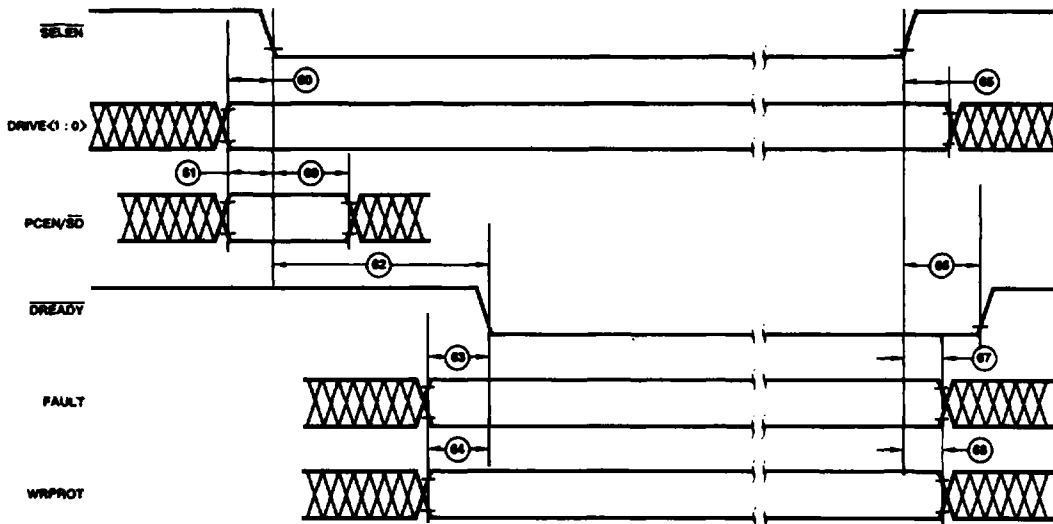
WF008841

DISK INTERFACE

Number	Parameters	Description	Min	Max	Units
60	tDRSU	DRIVESEL <1 : 0> Set-up to SELEN Active	0		ns
61	tPCSU	PCEN/SD Set-up to SELEN Active	0		ns
62	tSELDRDY	SELEN Active to DREADY Active	0	12.8	ms
63	tFLTSU	Fault to DREADY Set-up	0		ns
64	tWPSU	WRITEPROT to DREADY Set-up	0		ns
65	tDSHD	SELEN Inactive to DRIVESEL <1 : 0> Hold	400		ns
66	tDRDYHD	SELEN Inactive to DREADY Hold	0		ns
67	tFLTHD	SELEN Inactive to FAULT Hold	0		ns
68	tWPHD	SELEN Inactive to WRITEPROT Hold	0		ns
69	tPCHD	PCEN/SD Hold	400		ns

PRELIMINARY

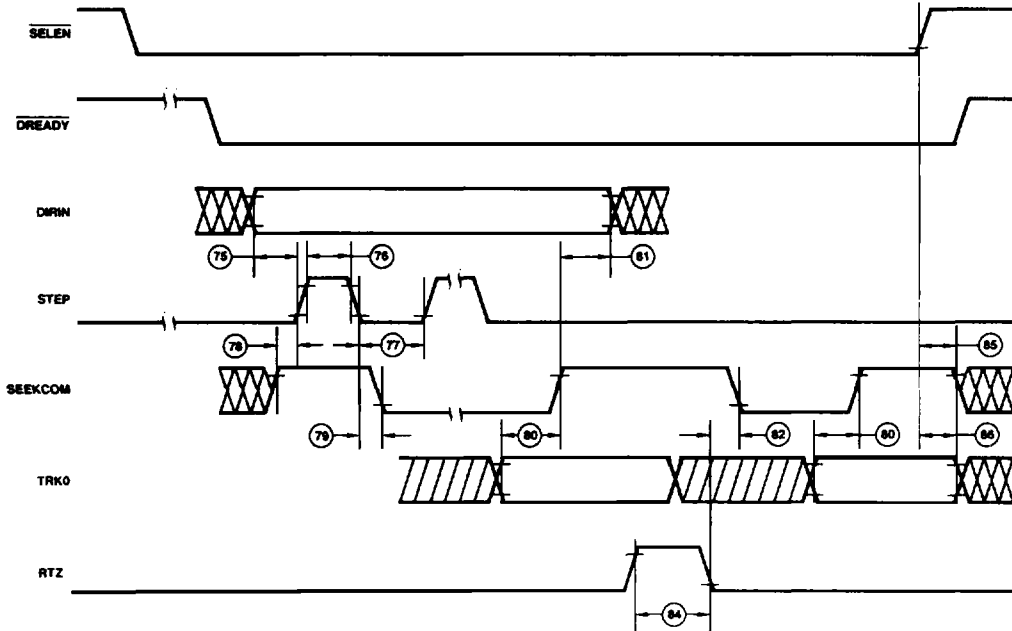
2



WF008301

DISK INTERFACE

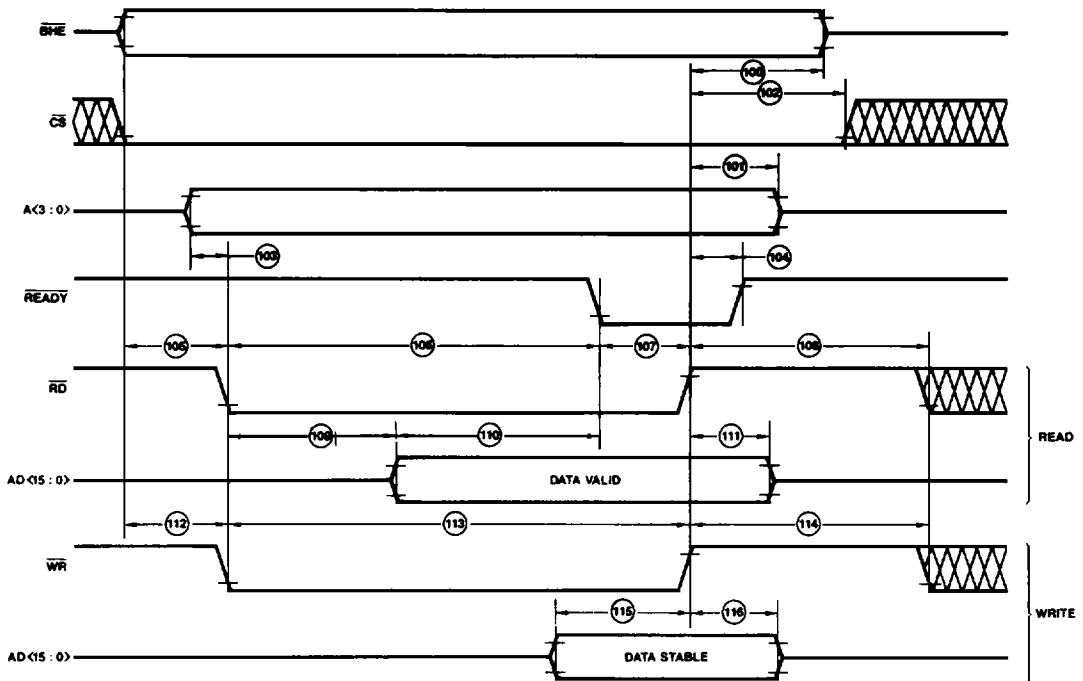
Number	Parameters	Description	Min	Max	Unit
75	tDIRSU	DIRIN Set-up	400		ns
76	tSTPWD	STEP High Width		User Programmable	ns
77	tSTLW	STEP Low Width		User Programmable	ns
78	tSKSU	SEEKCOM Set-up to STEP	400		ns
79	tSTPSK	STEP Low to SEEKCOM Low		10	ns
80	tTRKSK	TRK0 to SEEKCOM Set-up	0		
81	tSKDIRI	SEEKCOM to DIRIN Inactive Hold	400		
82	tRTZSK	RTZ Low to SEEKCOM Low		10	ns
84	tRTZWD	RTZ Pulse Width		User Programmable	ns
85	tSELSKI	SELEN Invalid to SEEKCOM Invalid	0		ns
86	tSELTRKI	SELEN Invalid to TRK0 Invalid	0		ns



WF008311

BUS SLAVE READ/WRITE

Number	Parameters	Description	Min	Max	Units
100	t _{HRW}	BHE to RD, WR Hold	0		ns
101	t _{HADD}	Address Hold	0		ns
102	t _{HCS}	CS Hold Time	0		ns
103	t _{SUADD}	Address Set-up	0		ns
104	t _{NRDY}	READY Negate Time	0	50	ns
105	t _{CSRd}	CS, BHE, to RD Set-up	0		ns
106	t _{RRDY}	READY Response Time	2 t _{CPC}	16 t _{CPC}	ns
107	t _{HSTB}	Strobe Hold	10		ns
108	t _{RRCV}	Read Recovery	t _{CPC} + 10		ns
109	t _{DATON}	Data Turn On	t _{CPC}	15 t _{CPC}	ns
110	t _{SUDAT}	Data Set-up	t _{CPC} - 30		ns
111	t _{DATOFF}	Data Turn-Off	0	50	ns
112	t _{CSWR}	CS, BHE, to WR Set-up	0		ns
113	t _{STBWR}	WR Strobe Width	t _{CPC}		ns
114	t _{WRCV}	Write Recovery	t _{CPC} + 10		ns
115	t _{SUDATW}	Data Write Set-up	40		ns
116	t _{HDDATW}	Data Write Hold	0		ns

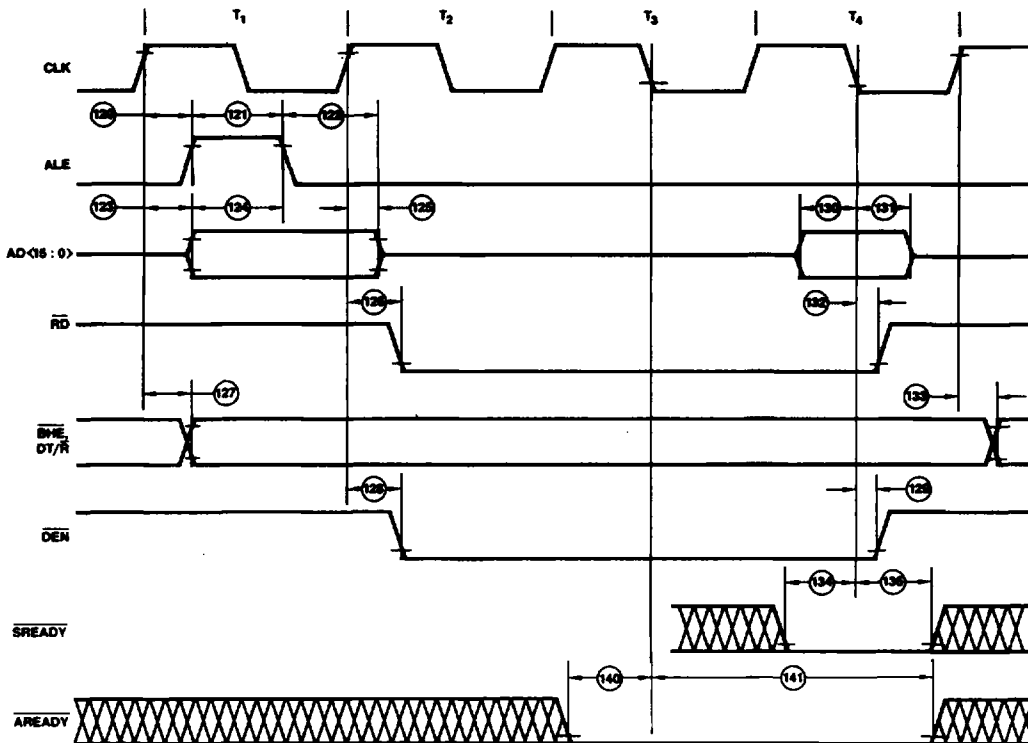


WF008321

BUS MASTER READ

Number	Parameters	Description	Min	Max	Units
120	t _{DALE}	CLK to ALE Active	0	50	ns
121	t _{WALE}	ALE Pulse Width	40		ns
122	t _{ADDHD}	Address <15 : 0> Hold Time	40		ns
123	t _{DADD}	CLK to Address <15 : 0> Valid	0	50	ns
124	t _{SUADD}	Address <15 : 0> Set-up	40		ns
125	t _{IADD}	CLK to Address <15 : 0> Invalid	0	50	ns
126	t _{DRD}	CLK to RD Active	0	50	ns
127	t _{VCNTL}	CLK to BHE, DT/R Valid	0	50	ns
128	t _{DDEN}	CLK to DEN Active	0	50	ns
129	t _{IDEN}	DEN to RD Inactive	0	50	ns
130	t _{SUDA}	RD In Setup	15		ns
131	t _{HDDA}	Data In Hold	0		ns
132	t _{IRD}	CLK to RD Negate	0	50	ns
133	t _{VCNTL}	BHE, DT/R Negate (if changing)	0	50	ns
134	t _{SURBY}	SREADY Set-up	15		ns
135	t _{HDRDY}	SREADY Hold	0		ns

BUS MASTER READ



WF008331

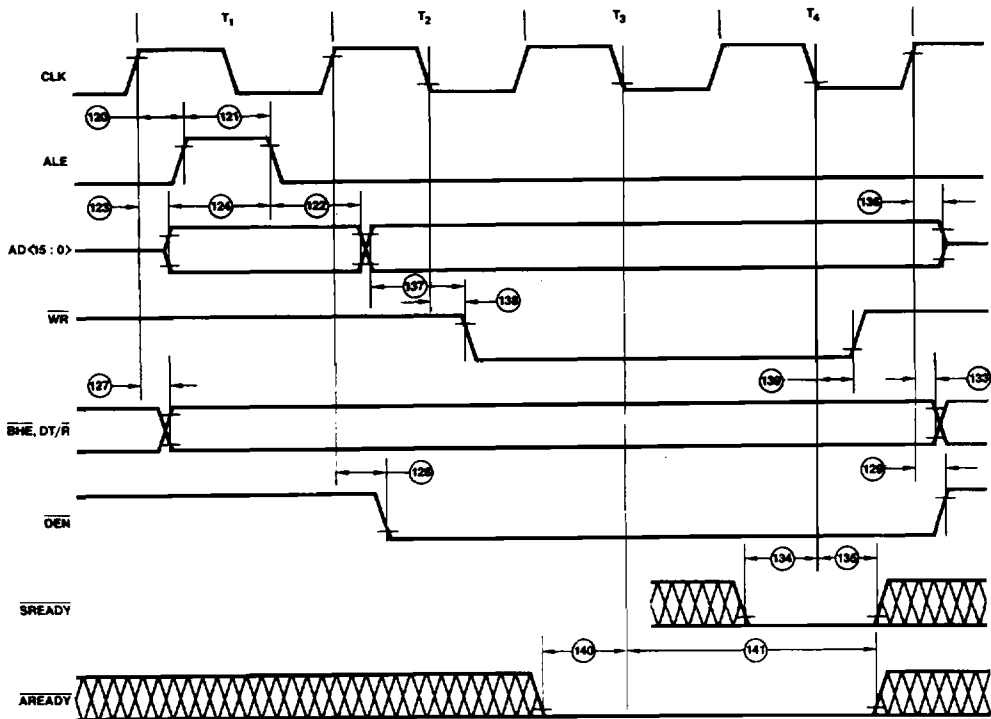
BUS MASTER WRITE

Number	Parameters	Description	Min	Max	Units
136	t_{DO}	Data Out Invalid		50	ns
137	t_{SUDT}	Data Out Set-up	40		ns
138	t_{DWR}	CLK to WR Active	0	50	ns
139	t_{HDWR}	CLK to WR Inactive	0	50	ns

AREADY

Number	Parameters	Description	Min	Max	Units
140	t_{ARSU}	$\overline{\text{AREADY}}$ Set-up to CLK Low	15		ns
141	t_{ARHD}	$\overline{\text{AREADY}}$ Hold to CLK Low	0		ns

BUS MASTER WRITE

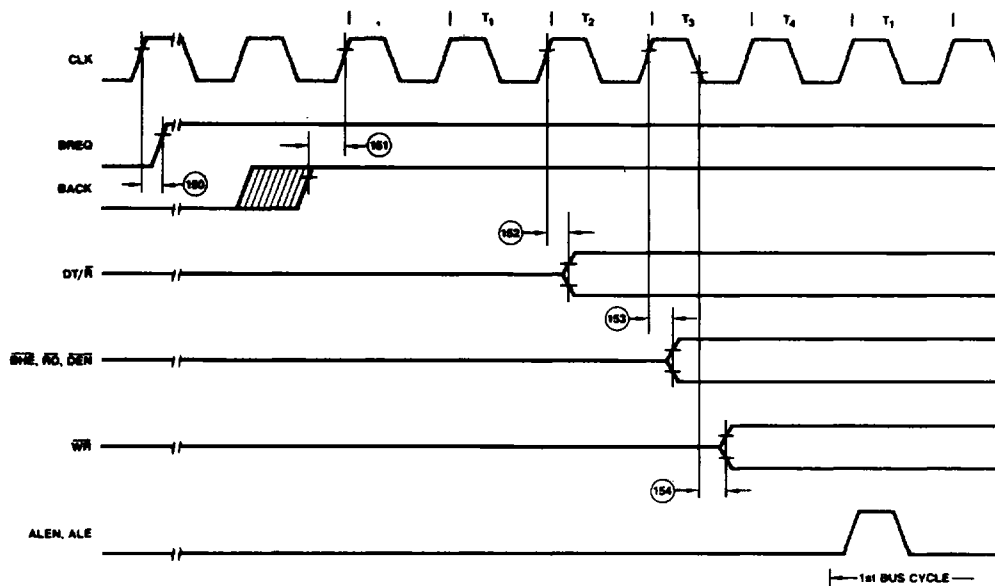


WF008341

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BUS REQUEST

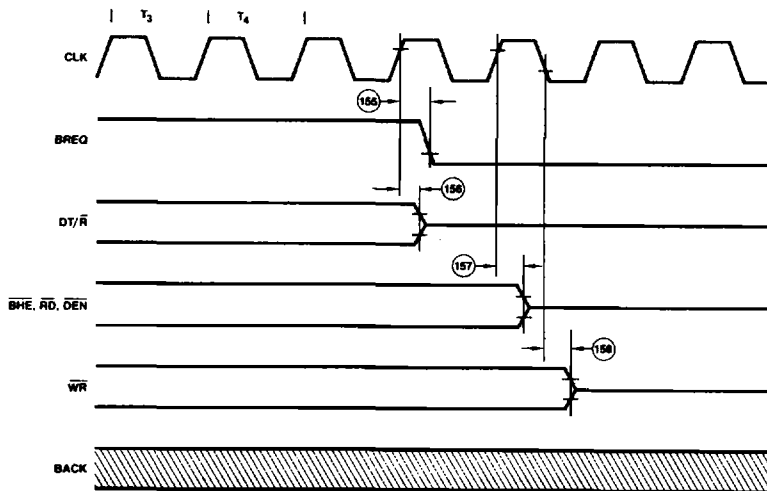
Number	Parameters	Description	Max	Units
150	t _{DBR}	CLK to BREQ Active	100	ns
151	t _{DBA}	BACK to CLK Setup (Sampling Bus Address)	20	ns
152	t _{DDTR}	CLK to DT/R	100	ns
153	t _{DCNTL}	CLK to BWE, RD and DEN	50	ns
154	t _{DWR}	CLK to WR Valid	50	ns



WF008360

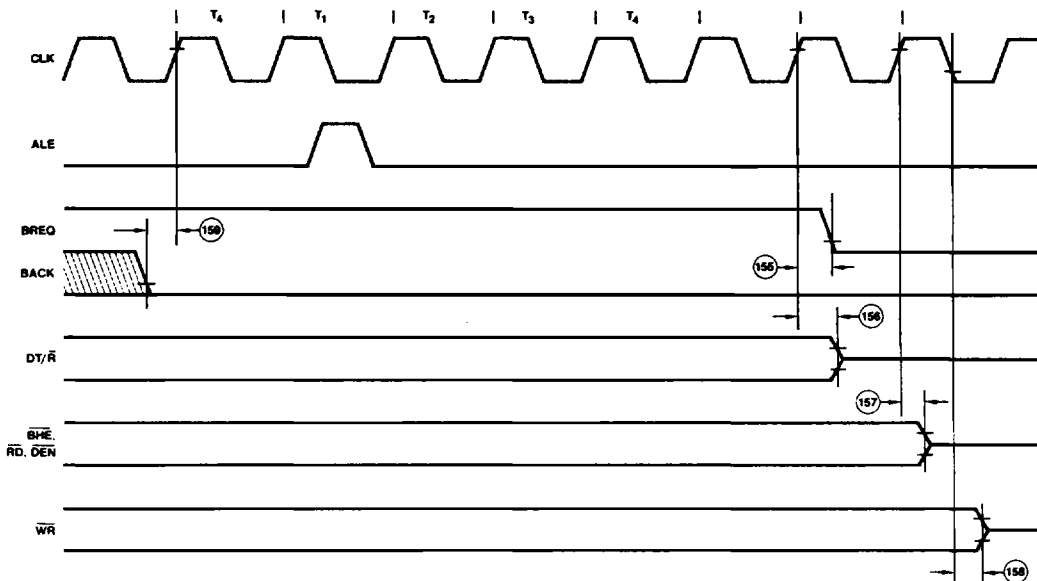
BUS RELEASE

Number	Parameters	Description	Min	Max	Units
155	t _{BREQ}	CLK to BREQ inactive		100	ns
156	t _{IDTR}	CLK to DT/R		100	ns
157	t _{ICNTL}	CLK to BHE, RD, DEN	0	50	ns
158	t _{IWR}	CLK to WR	0	50	ns
159	t _{SBA}	BACK to CLK Set-up (Synchronous Operation)	20		ns



WF008350

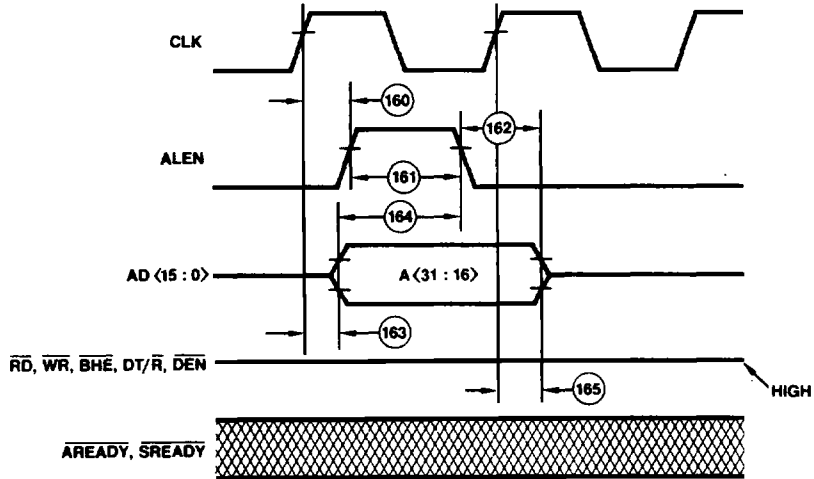
PREEMPTIVE BUS RELEASE



WF008370

UPPER ADDRESS LATCH

Number	Parameters	Description	Max	Units
160	t _{DALEN}	CLK to ALEN Active	50	ns
161	t _{WALEN}	ALEN Pulse Width	40	ns
162	t _{DADDH}	AD <15:0> Hold Time	40	ns
163	t _{DADD}	CLK to AD <15:0> Valid	0	ns
164	t _{SUADD}	AD <15:0> Set-up Time	40	ns
165	t _{IADD}	CLK to AD <15:0> Invalid	0	ns



WF008381