VM65060

ANALOG PRML CHANNEL

VTC Inc.
Value the Customer™

970801

PRELIMINARY

August,1997

FEATURES

- Register programmable user data rates from 46 to 140 Mbps
- Sampled data read channel with maximum likelihood Viterbi detection
- Programmable continuous-time filter with two independently-variable real zeros
- Programmable seven-tap transversal filter for PR4 equalization
- Self-adapting option for FIR tap weights
- Programmable two-level write precompensation with 1.25% resolution
- Direct Write/Read feature for equalizer optimization
- Analog/sampled AGC
- Zero phase restart for fast acquisition
- Servo area detectors for burst demodulation
- Fast timing control during acquisition by bypassing FIR filter
- Register programmable power management (<5 mW Power Down mode)
- 4 or 8-bit wide parallel data interface to disk controller
- Serial interface port for access to internal program storage registers to load and verify
- Single power supply (5V ±10%)
- Small footprint 80-pin PQFP package

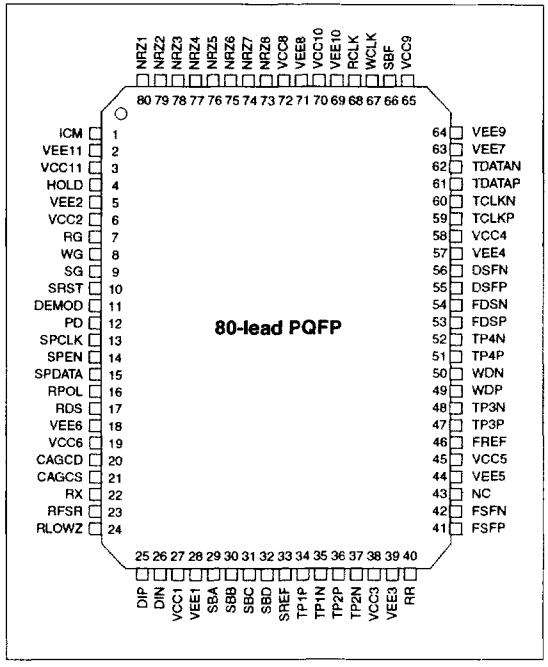
DESCRIPTION

The VM65060 is a high performance BiCMOS read channel IC that provides all of the data processing needed to implement a Partial Response Maximum Likelihood (PRML) read channel for zoned recording MR hard disk drive systems with user data rates from 46 to 140 Mbps.

BiCMOS process technology along with advanced circuit design techniques result in high performance devices with low power consumption. The part requires a single +5V power supply and is available in a 80-Lead PQFP package.

Functional blocks include AGC, programmable continuous time filter, adaptive FIR filter, maximum likelihood Viterbi detector, frequency synthesizer, 2-level nonlinear write precomp and area detectors for servo bursts. Programmable functions such as data rate, filter cutoff/boost, FIR tap weights, adaption parameters, write precomp values, etc. are controlled by writing to the serial port registers. No external component changes are required to change zones.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage
V_{CC} ..... -0.3V to +7V
Input Voltages
Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
Analog Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
Storage Temperature T_{stg} ..... -65°C to 150°C
Junction Temperature T_J ..... 150°C
Thermal Impedance Characteristics, Θ_{JA}:
80-Lead PQFP ..... 39°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} ..... +5V ± 10%
Junction Temperature T_J ..... 0°C to 125°C

MIXED SIGNAL CIRCUITS

BLOCK DIAGRAM DESCRIPTION

AUTOMATIC GAIN CONTROL:
- Dual mode AGC, analog during acquisition, sampled during read data
- Separate AGC level storage pins for data and servo
- Dual rate attack and decay charge pump for rapid AGC recovery
- Programmable, symmetric, charge pump currents during read data
- Charge pump currents track programmable data rate
- Low drift AGC hold circuitry
- Internal Low Z for write mode.
- Externally adjustable one-shot pulse width for LOWZ control
- AGC hold, fast recovery, and AGC input impedance control signals
- Wide bandwidth, precision full-wave rectifier

LOW PASS FILTER/EQUALIZER:
- Programmable, 7-pole, continuous time filter provides:
  - Channel filter and pulse slimming equalization for equalization to PR4
  - Programmable cutoff frequency from 7 to 48 MHz
  - Programmable boost/equalization of 0 to 13 dB
  - Programmable group delay of ±30%
  - Differentiator outputs match normal output phase
  - Minimized size and power

FIR FILTER/EQUALIZER:
- Seven tap filter
- Individual tap adjustment for fine equalization to PR4 target
- No external components required
- Independent and/or dependent self adaption of tap weights
- User programmable adaption parameters:
  - Integration time
  - Dead zone control
  - Tap starting points
  - Number of taps to adapt
  - Selection of which taps to independently adjust

LEVEL QUALIFICATION:
- Level pulse qualifier for servo and sync field reads
- Independent positive and negative thresholds for asymmetrical signals (e.g. from MR heads)
- Independent thresholds for servo

MAXIMUM LIKELIHOOD DETECTOR:
- Sampled Viterbi detection of signal equalized to PR4
- Programmable threshold window
- Survival register length of five

FREQUENCY SYNTHESIZER:
- Better than 1% frequency resolution
- Up to 200 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

TIMING RECOVERY
- Single external capacitor required
- Register programmable to user data rate of 140 Mbps operation
- Fast Acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Programmable damping ratio which is constant over all data rates

WRITE PRECOMPENSATION:
- Independently-programmable write precompensation for three data patterns
- Step resolution of 1.25% up to 40%
- Precompensation tracks Frequency Synthesizer period
- Differential PECL write data output
- Precoding function suited for PR4 channel

SERVO:
- Wide bandwidth, precision full-wave rectifier
- Separate, automatically-selected registers for servo f_c, boost, and group delay
- Individual area detectors for servo bursts A, B, C and D
- Programmable servo gain of ± 4 dB

DIGITAL BACKEND:
- 4-bit (nibble) and 8-bit (byte) wide Bidirectional NRZ interface
- Parallel-to-Serial and Serial-to-Parallel converters
- 8/9 (0, 4/4) Encoder and Decoder
- 8-bit wide data Scrambler and Descrambler, with Pseudo Random Number Generator
- SYNC Byte detector, programmable, dual byte ("or" type)
- Channel clock divider
- 4-bit or 8-bit Direct Test Write and Read

PIN FUNCTIONS AND DESCRIPTION

Pin functions are described on page 57.

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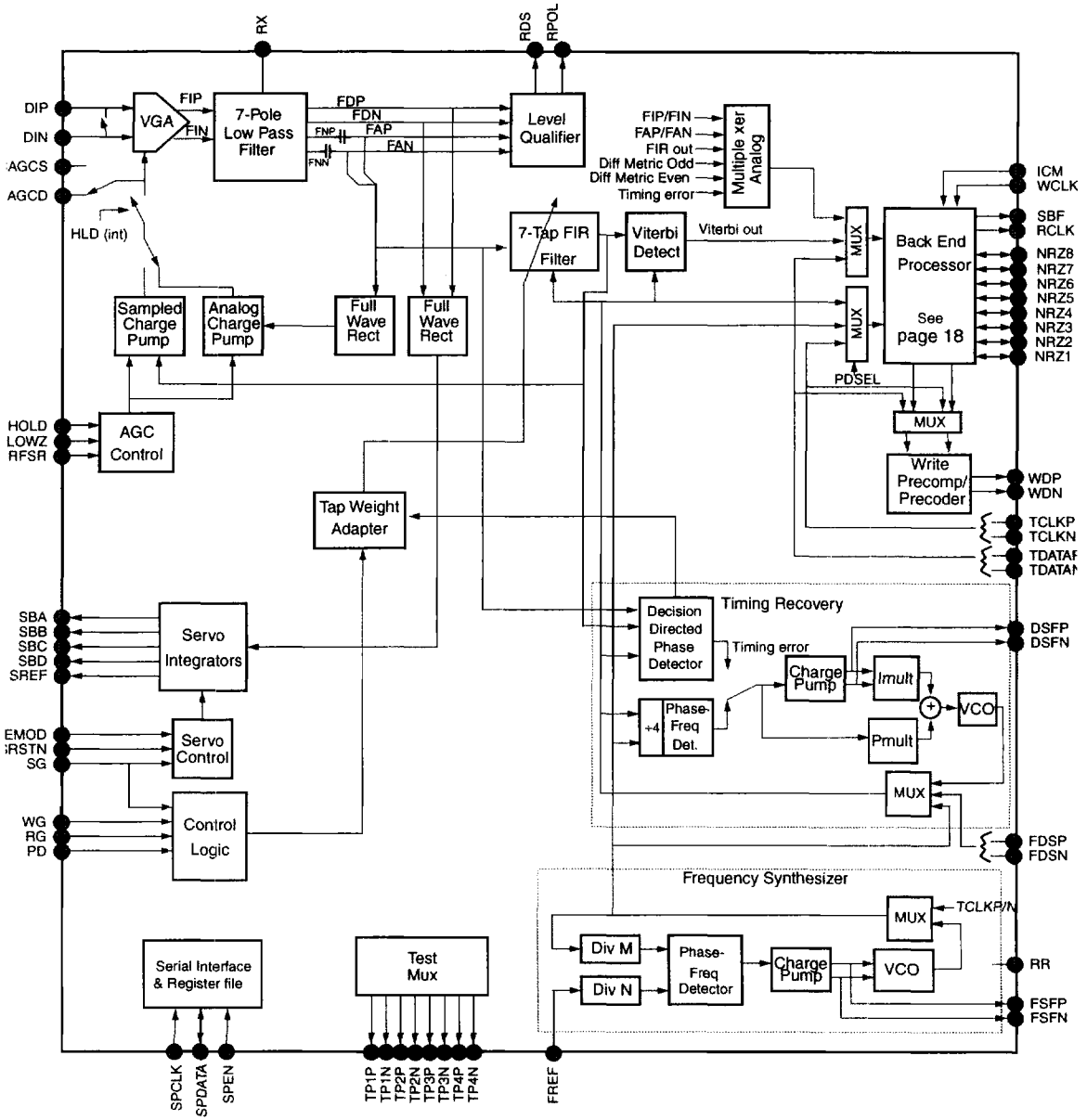
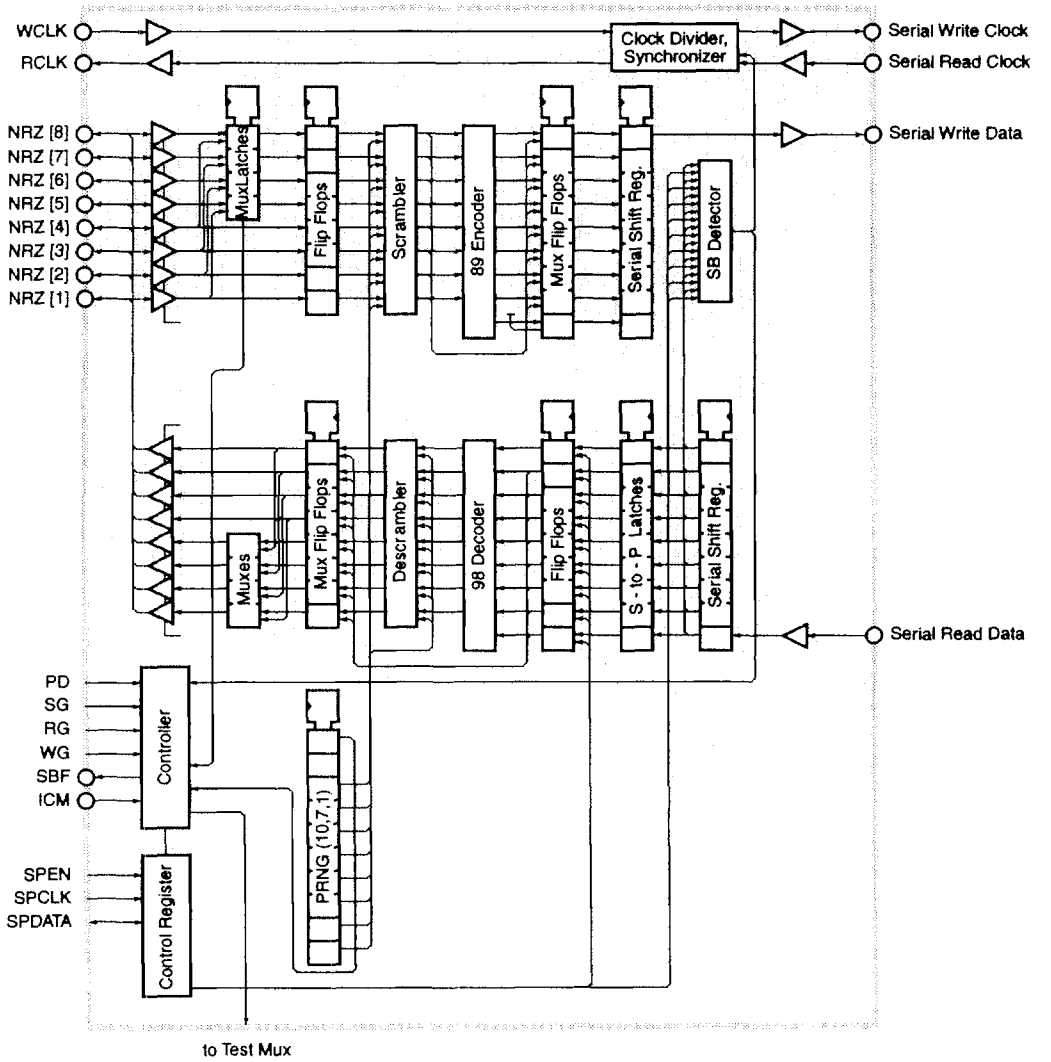
BLOCK DIAGRAM



DIGITAL BACK END TOP LEVEL SCHEMATIC / LOGIC BLOCKS



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BLOCK-BY-BLOCK FUNCTIONAL DESCRIPTION

TheVM65060 implements a complete high performance PRML read channel. The VM65060 includes an AGC, programmable filter/equalizer, adaptive FIR filter, Viterbi detector, frequency synthesizer, decision-directed timing recovery, write precompensation and area detect servo, and supports user data rates up to 140 Mbps. A serial port is provided to read and write control data to the 16 internal programmable storage registers.

GAIN CONTROL (GC)

The Gain Control section of the VM65060 consists of a wideband variable gain amplifier (VGA) and a programmable continuous time filter, with a charge pump, amplitude detector, and exponentiator. The Gain Control has two modes: Automatic (AGC), and Programmable (PGC). The mode is selected with the PGC register bit.

Servo reads employ a fully differential analog AGC loop, while data reads employ both the analog loop (for fast acquisition) and a sampled/decision-directed loop (for fine tuning of the gain). The programmable gain control (PGC) circuit controls the VGA gain with an internal DAC. In PGC mode, the AGC loop is disabled and the VGA gain is a linear function of the DAC count.

The read signal is externally AC-coupled into the VGA amplifier on the DIP/DIN pins. The gain of the VGA is controlled by the voltage stored on the CAGCD hold capacitor for data reads (SG=0) and CAGCS for servo reads (SG=1). Two external holding capacitors allow for data and servo fields to have independent charge and discharge rates to avoid long reacquisitions of the gain at the beginning of the servo and data fields. The read signal is amplified and equalized by a low pass filter. The AGC loop locks the differential peak-to-peak voltage at FAP/FAN to $V_{FA} = 0.5V_{ppd}$ for inputs ranging from 20 to 200 mV_{ppd}. Test modes are provided in which the normal and differentiated filter outputs (FNP/FNN, FDP/FDN), the VGA inputs and outputs (DIP/DIN, DOP/DON), and the pulse qualifier inputs (FAP/FAN) are multiplexed to the TP2P/TP2N output pins respectively.

The analog AGC loop consists of the VGA amplifier, programmable continuous time filter, amplitude detector, exponentiator, and dual rate charge pump for fast transient recovery. Charge currents (decay) increase the capacitor voltage, V_{cagcx}, and increase the VGA gain while discharge currents (attack) lower the capacitor voltage, V_{cagcx}, and reduce the VGA gain.

When switching between data and servo modes, the VGA gain is momentarily squelched and the input impedance is reduced by a factor of 10 (to allow quick recovery from transient offsets), then a fast recovery mode is initiated. External resistor R_{LOWS} sets the amount of time the low Z state is on.

During ultra fast recovery, the VGA gain is increased to 144 times its normal rate until the signal exceeds its target value. The loop then enters a "fast" mode. This high bandwidth mode continues until the fast acquisition window T_{FAQ} times-out, whereupon normal charge pump currents are reinstated and loop bandwidth is reduced to its normal value for servo mode. External resistor R_{FSQ} sets the fast acquisition window period, T_{FAQ}.

To optimize recovery for constant density recording, all charge pump currents track with the value loaded in the data rate register (DRR); current magnitude ranges from I_{QXX} at maximum DR to $I_{QXX}/2$ at minimum DR. The magnitude of the charge pump currents, I_{QXX}, are set by an external resistor connected between the RX pin and ground and are given by the following equations:

$$I_{QND} = \frac{2.16V}{RX} \text{ (DRR = 11111), RX = 6 k}\Omega \qquad \textit{(eq. 1)}$$

$I_{QNC} = I_{QND}/18$, $I_{QFC} = I_{QND}/2..0$, $I_{QUFC} = 8.6I_{QND}$, $I_{QFD} = 8I_{QND}$

The RX = 6 kΩ has been optimized for user data rates of 70-140 Mbps and can be scaled appropriately for lower data rates. VTC recommends that the AGC loop response be altered by varying the CAGCx capacitors and not the RX resistor. Since servo data is written at a lower fixed frequency, the magnitudes of charge pump currents in servo mode are set equal to those that occur at the minimum data rate in read mode.

For data reads, the analog AGC loop is utilized to quickly lock onto the incoming sync field preamble. When RG is asserted, the FIR, Viterbi detector, and decision-directed AGC and timing recovery circuits are powered up (if the programmable power reduction feature is enabled). An internal, delayed RG signal (RGD) is then generated two byte times after external RG is asserted. The sync field count begins when RGD is asserted. Refer to Diagram 2.

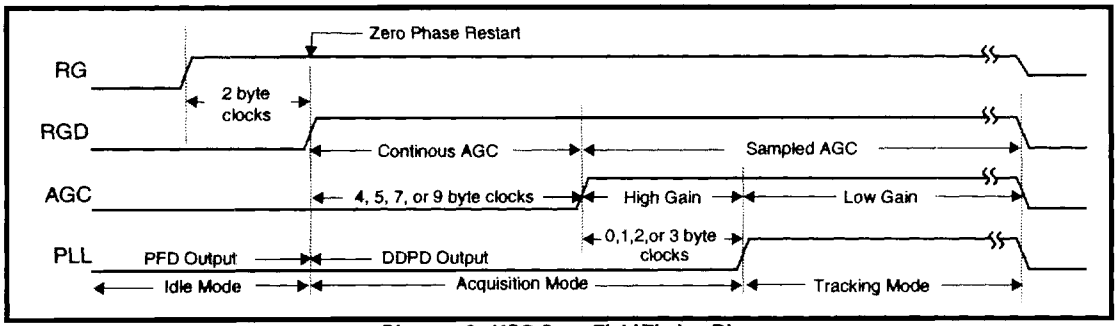


Diagram 2 VCO Sync Field Timing Diagram

The AGC transition in high gain mode and the PLL transition into tracking mode are based on two programmable sync-field counters, the AGC SF counter and the PLL SF counter. The AGC transition from continuous to sampled high gain is determined by one of four programmable counts of 4, 5, 7, or 9 byte times (for this discussion, a 'byte time' equals 8 channel-bit times) which are derived from the frequency synthesizer clock; this is the AGC SF count.
Additionally, the PLL acquisition time can be extended by one of four progammable counts of 0, 1, 2 or 3 byte times following the AGC SF count; this is the PLL SF count. The sampled AGC remains in the high gain mode for the sum of both counts, then transitions into low gain. The PLL transitions from idle to acquisition mode when RGD is asserted. The PLL remains in acquisition mode through the sum of both the AGC SF and PLL SF counts, whereupon, it transitions into the tracking mode.

The sampled AGC loop consists of the VGA, the programmable continuous time filter, the sampling 7-tap FIR equalizer, the decision amplitude detector and charge pump. Symmetrical charge and discharge currents are utilized in the sampled mode. To optimize recovery for constant density recording, the charge pump currents in the sampled mode track with the value loaded in the data rate register (DRR); current magnitude ranges from I_Q at maximum data rate (DR) to $I_Q/2$ at minimum DR. The magnitude of the charge pump currents, I_Q, can be programmed from the sample loop control register to 0, 20, 40, or 60 µA for DRR = 11111. The high gain charge pump current is fixed at 180 µA.

The VGA has an exponential characteristic of gain versus control voltage in order to minimize response time over the entire range of input voltages. When in the PGC mode, the amplitude detector, charge pump, and exponentiator are disabled, and the gain of the VGA is controlled by the PGC control register. The VGA has a linear gain versus DAC count and is expressed by the following equation:

$$A_V = 2.8(N) + 2.4 \qquad \textit{(eq. 2)}$$

where N ranges between 0 and 15 decimal or 0000 to 1111 binary

PULSE QUALIFIER

The pulse detector (PD), converts analog read data into a digital pulse stream, utilizing amplitude discrimination. The timing between peaks is provided on the rising edges of the RDS output. The timing channel inputs, FDP/FDN, are direct-coupled from the differentiated output of the filter. The level channel inputs FAP/FAN are AC-coupled from the normal outputs of the filter.

The timing channel inputs (FD = FDP/FDN) are derived from the differentiated output of the low pass filter. A zero-cross comparator at FD detects the peaks of the waveform to preserve the timing of the read pattern. A bi-directional one shot circuit with nominal pulse width of 4ns clocks the D-type Flip-Flop on either positive or negative transitions of the FD input. Visibility into the timing channel signal HRCLK is provided in test mode "Test Modes" on page 54.

The HRCLK pulses are qualified by signals which are derived from the low pass filter output. Two comparators indicate when the positive (LP) and negative (LN) extents of the signal V_{FA} = V_{FAP}-V_{FAN} exceed either the positive threshold (V_{THP}) or the negative threshold (V_{THN}) level. Independent control of positive and negative thresholds is provided with 5-bit DACs ranging from 20-80% of V_{FA}. Vthx=20+1.9×VALUE in percent, where VALUE ranges from 0 to 31. Once the signal exceeds the level threshold, a high level is presented to the D-input of the Flip-Flop. When the peak is reached, the timing channel clocks a '1' into the Flip-Flop and triggers a one-shot producing the RDS output. The Flip-Flop resets on the rising edge of RDS and is ready for the next bit after the one-shot times out. A nominal pulse width of 24 ns is provided at the RDS output. Consecutive same-polarity pulses are also qualified. RDS polarity information is provided with the RPOL output.

PROGRAMMABLE LOW PASS FILTER (LPF) / EQUALIZER

The filter is implemented as a 7-pole 0.05 degree linear phase equiripple low pass filter with matched normal and differentiated outputs. The cutoff frequency, boost, and DC group delay equalization are programmable.

The filter supplies normal and differentiated low-pass outputs with matched group delays. The normal output goes to the AGC and servo sections. The differentiated output, along with the normal output, is used by the level qualifier block to provide data and servo peak position information. The relative gain AO_D of the differentiated output to the normal output is nearly constant (at two-thirds the unboosted cutoff frequency) over the range of the cutoff frequency and boost level of the filter.

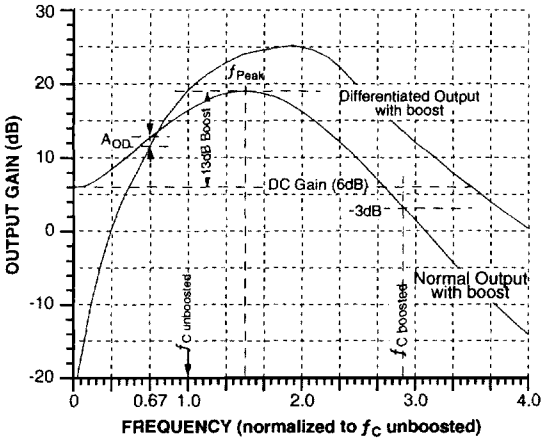
Cutoff frequency is controlled by the continuous time filter f_C DAC. The control word for the DAC is read from the CTF Data f_C register when SG=0; otherwise its read from the CTF Servo f_C register (see Table 9 Serial Register Bit Descriptions). Cutoff frequency (f_C), in MHz, is related to the binary control word by the following equation:

$$f_C = (0.343 \times N) + 4.5 \qquad \textit{(eq. 3)}$$

where N ranges between 0 and 127 decimal

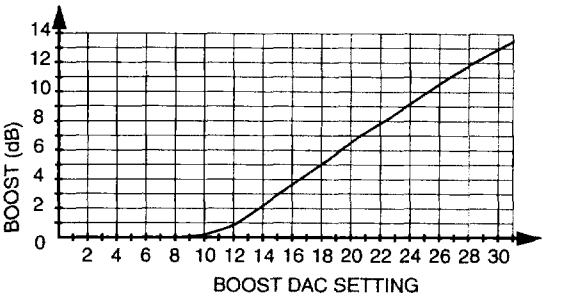
The amount of boost equalization depends on the output of the BOOST DAC. Boost is programmable from 0 to 13dB as measured from the low-frequency gain portion of the frequency domain transfer function to the peak in the transfer function.

Graph 1 shows normalized filter response curves with maximum boost for both the normal and differentiated outputs.



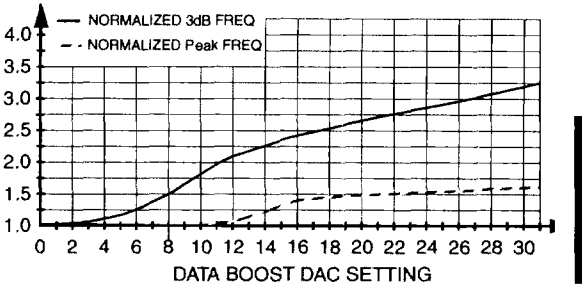
Graph 1 Normal and Differentiated Output Gains

Graph 2 shows the nominal relationship between the BOOST control word and the resulting boost level.



Graph 2 Ideal Boost (in dB) versus BOOST DAC VALUE

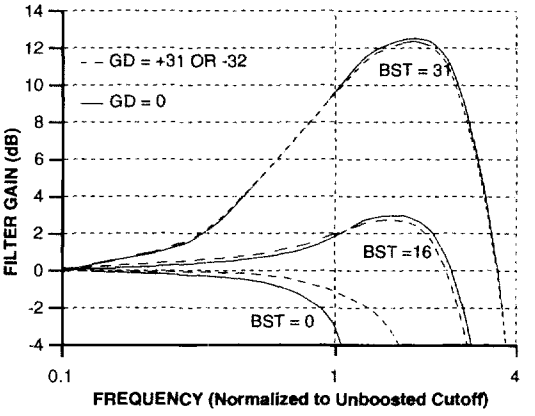
Graph 3 shows the effect of boost on the cutoff frequency.



Graph 3 Normalized f_c and f_{peak} versus DATA

Setting the desired boost through the boost register (with the group delay register set to zero) produces symmetric zeros on the real axis. This maintains the constant group delay as in the no boost case. The group delay register can be used to produce asymmetry in the zeros causing the group delay to vary. This can be desirable to compensate for asymmetry in the heads/media components. Group delay can be varied by ±30% from the symmetric zero (group delay register = 0) condition. The boost is held nearly constant as group delay is varied.

Graph 4 shows what happens to the magnitude response as the Group Delay register varies over extremes and under several boost conditions.



Graph 4 Gain Variations with Different Boost and Group Delay Settings

The group delay register is six bits wide in "two's complement" format. A code of +31 corresponds to a DC shift in group delay of +30%; a code of -32 corresponds to -30% shift in DC group delay. Group delay is expressed as:

$$GD_{DC} = 0.95 \times GD_{DAC} \qquad (eq.\ 4)$$

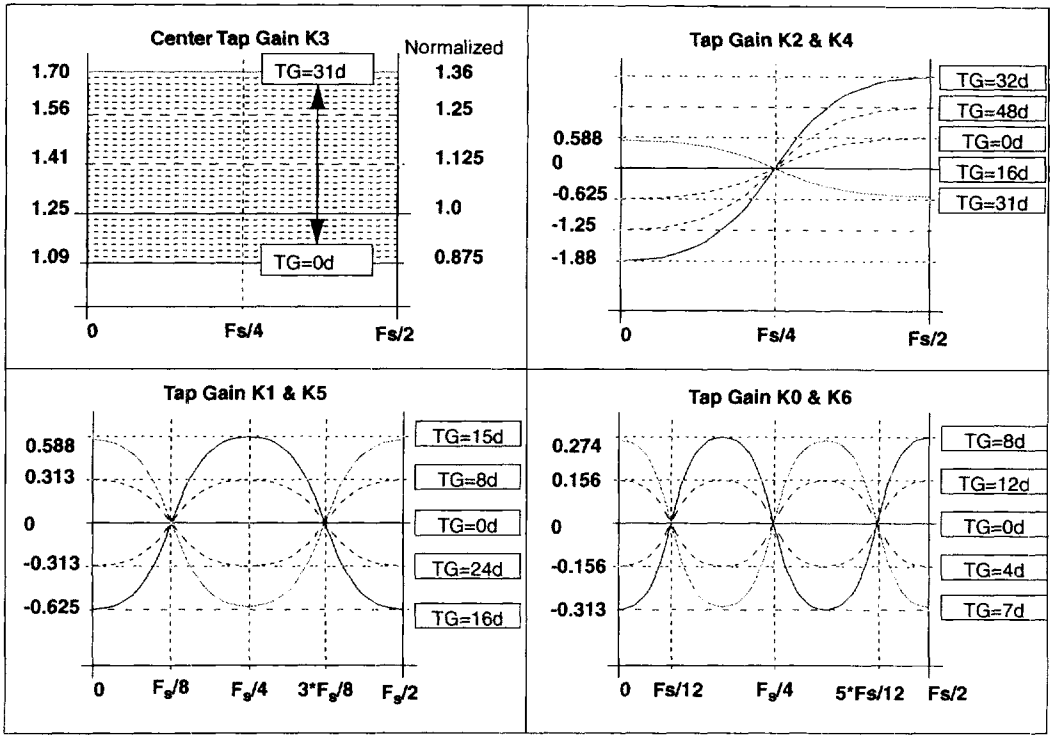
Group delay for an ideal 0.05 degree equiripple filter is flat within one percent out to twice the unboosted cutoff frequency. Because group delay is extremely sensitive to device mismatches and parasitic effects, a "real" filter will have variations of several percent. Group delay flatness is defined as the variation about an average value out to the specified frequency. The VM65060 group delay flatness is specified to be less then ±2% out to 1.5 times the unboosted cutoff frequency. It is expressed in percent because the group delay is inversely related to the unboosted cutoff frequency, and is about 12 ns at a cutoff of 48 MHz. Thus at this cutoff frequency, the group delay varies by less than 0.18 ns out to 72 MHz.

The absolute group delay through the Gain Control block and the filter consists of both a fixed delay and a delay that varies inversely with cutoff frequency. The group delay (T_{GD}), in nanoseconds, is expressed below as a function of the cutoff frequency in MHz.

$$T_{GD} = \left[3 + \frac{434}{f_C}\right] ns \qquad (eq.\ 5)$$

FIR FILTER EQUALIZER

The FIR is a seven (7) tap transversal filter with independently-controllable tap weights. Independent control provides both gain and phase adjustment of the input signal. The following plot illustrates the possible gain variations achievable when symmetric taps are swept together over the allowable ranges, as listed in Table 1.



Graph 5 Symmetric Tap, frequency response curves

The H_0 term provides only a real valued response equal to the center tap gain. The gain response also includes finite bandwidth characteristics of the sampler. The sampler BW is about 350 MHz and will have some effect on the frequency characteristics. The ideal gain limits for the taps are shown below.

Table 1 FIR Tap Gain settings

Tap	K_{-3}	K_{-2}	K_{-1}	K_0	K_1	K_2	K_3
Gain Range	-0.156 +0.137	–0.312 +0.293	–.9375 +0.293	+1.09 +1.70	–.9375 +0.293	-0.312 +0.293	-0.156 +0.137
Actual bits	4	5	6	5	6	5	4
Eff. bits	7	7	7	7	7	7	7
Resolution	(1/64) X 1.25 = 19.56 mV/V						

FIR ADAPTION CIRCUIT

Normal operation:

The adaption process starts after RG has been asserted and the internal delayed read gate RGDP has become active. It should be noted that since the part is accessing the serial registers during adaption, the user should NOT attempt any serial register operation while RG is asserted and the AE bit is set.

Parameter Descriptions:

- Adaptation Control Test "ACTST"
  These bits allow the basic verification of the Adaptation Control logic.
- Adaptation Enable "AE"
  This bit controls whether adaptation is to be performed. It cannot be modified during an adaptation read cycle.
- Dead Zone "DZ"
  This three-bit control specifies how many update samples are required in either direction to cause adaptation in that direction. The value sets the threshold in a symmetrical manner.
- Integration Length "INTL"
  This two-bit control selects the number of samples to average for each update cycle (12, 15, 18, or 21)
- Initial Tap Weight "ITW"
  This value selects which tap to adapt first.
- No Sync Byte "NOSB"
  This feature causes adaptation to occur at the point where the timing recovery circuit makes the transition from acquisition to tracking modes. This occurs during the VCO sync field even before the sync bytes.
  This option may be useful during initial drive optimization and data recovery modes.
- Tap Weight Range "TWR"
  This value sets the number of taps that are adjusted. If all six taps are to be adjusted this value should be set to "0". By setting this value to "1" through "4" a reduced range of taps will be adjusted. The taps that are not adjusted are still active but are held at their preprogrammed values.
- Symmetry control "SYMC"
  This two-bit control selects which sets of taps should be controlled in a symmetrical manner.

Tap weights can be written and read by the controller. Thus the initial tap weight values can be preset near their optimal values and the final values can be read back after each adaption read cycle. The final taps weights remain as the initial tap weights for subsequent read cycles.

Proper selection of DZ and INTL can allow for rapid adaptation or for slow highly-stable tracking of system changes.

VITERBI DETECTOR

The Viterbi detector implements the maximum likelihood (ML) detector for PRML. The Viterbi detector block diagram is shown in Diagram 3.

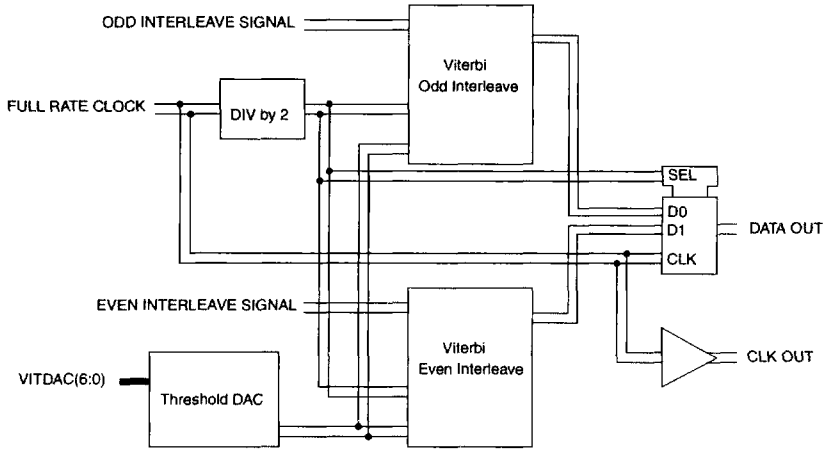


Diagram 3 Viterbi Detector Block Diagram

Note that all signals are differential. The incoming signal (from the FIR filter via the timing recovery block) has been demultiplexed into the odd and even interleaves on a bit-by-bit basis. This is shown in the diagram as the odd interleave signal and the even interleave signal. Each interleave of the Viterbi detector runs at 1/2 the channel data rate. Note that the odd and even interleaves of the Viterbi detector are clocked on opposite phases of the full rate data clock. Each interleave independently processes its data stream. The data streams from the odd and even interleaves are then multiplexed back together on a bit-by-bit basis to yield the recovered bit stream.

The nominal Viterbi threshold window size is set by a 7-bit DAC which is controlled by the Viterbi DAC serial control register. Positive and negative thresholds in the Viterbi detector are modified based on the received data.

The dynamic thresholds in the Viterbi detector function to reject pulses of the same polarity as the most recent pulse, but of lesser amplitude. If a pulse of the same polarity as the most recent pulse exceeds the amplitude of the previous pulse, the 1 associated with the previous pulse (which is of lesser amplitude) is erased in the Viterbi detector's path memory. The path memory only has the ability to erase these smaller pulses if four or fewer zeroes have occurred between the two pulses of the same polarity. This requirement is satisfied by the (0,4,4) encoding that is used with this part.

The AGC circuit adjusts the signal amplitude to ±250 mV peak. Side sampling for PR4 produces a nominal sampled-signal amplitude of ±180 mV. This is a pseudo-ternary signal with the ±1 levels equal to ±180 mV and the zero level equal to 0 mV. Thus, the Viterbi threshold, VIT_{TH}, is nominally set to 90 mV. Since the data is pseudo-ternary, the nominal Viterbi threshold window size is $2 \bullet VIT_{TH}$.

$$VIT_{TH} = \left[0.047 + 0.376\left(\frac{VALUE}{127}\right)\right]mV \qquad \textit{(eq. 6)}$$

where VALUE is between 0 and 127, inclusive

Diagram 4 shows a block diagram of a Viterbi detector interleave.

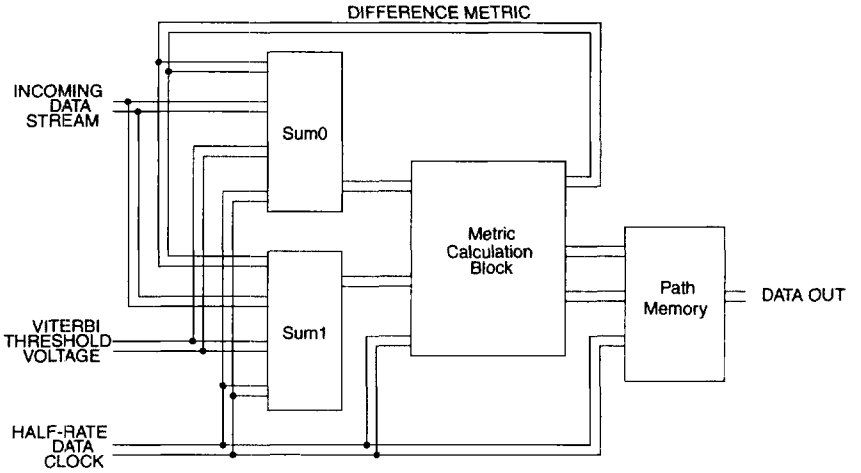


Diagram 4 Viterbi Interleave Block Diagram

The summing blocks, Sum0 and Sum1, each form two signals that are fed to the metric calculation block. Opposite polarities of the incoming data stream and the difference metric are used by Sum0 and Sum1. The metric calculation block outputs the difference metric (which is fed back to the Sum0 and Sum1 blocks) and the two data streams that are used by the path memory block. One of these two data streams from the metric calculation block represents 1's that come from positive pulses in the ternary data signal. The other data stream represents 1's due to the negative pulses in the ternary data stream. Two 1's in one of the data streams without an intervening 1 in the other data stream results in the path memory erasing the first of these two consecutive 1's. A 0 results when neither of the two data streams is a 1. Decoding of the ternary signal is straightforward: a positive or negative pulse results in a 1; no pulse decodes to a 0. This decoding action can be thought of as undoing the precoding function.

FREQUENCY SYNTHESIZER

The Frequency Synthesizer (FS) is a PLL-based circuit that provides a programmable reference frequency for constant density recording applications. The frequency synthesizer output frequency can be programmed with a better than 1% accuracy via the M,N ("divide by") and DR (Data Rate) Registers. The synthesizer output frequency, F_{OUT}, should be programmed as close as possible to ((9/8)•User Data Rate). The synthesizer also supplies the timing reference for write precompensation so that the precompensation tracks the VCO period.

The frequency synthesizer requires an external passive loop filter to control its PLL locking characteristics. This filter is pseudo-differential and balanced in order to reduce the effects of common mode noise.

In Write and Idle modes, the programmable frequency synthesizer is used to provide a stable reference frequency to the timing recovery loop. In the Write and Idle modes, the frequency synthesizer output, when selected by the Control Test Mode Register, can be monitored at the TP3 test pin. In the Read mode, the FS output should not be selected for output on the test pins so that the possibility of jitter in the timing recovery PLL is minimized.

The synthesizer output frequency is programmed using the M and N registers of the frequency synthesizer via the serial port, and is related to the external reference clock input, FREF, as follows:

$$f_{out} = f_{FREF}\left[\frac{(M+1)}{(N+1)}\right] \qquad \textit{(eq. 7)}$$

The M and N values should be chosen with the consideration of phase detector update rate and the external passive loop filter design. The Data Rate Register must be set to the correct VCO center frequency.

The DR register value directly affects the following:

- Center frequency of the frequency synthesizer VCO
- Center frequency of the timing recovery VCO
- Phase detector gain of the frequency synthesizer phase detector
- Write precompensation

The reference current for the DR DAC is set by an external resistor, RR, connected between the GND and RR pins. The VCO center frequency, f_c, and the charge pump current, I_{QP}, are given by the equations below. RR is the resistance of the external resistor in Ohms, X is the decimal equivalent of the DR Register bits and K_{VCO} (rad/V•s) is the VCO gain.

$$\omega_C = \left(\frac{4 \times 10^{10}}{RR}\right) \times (33 + X) \quad (0 \le X \le 31) \qquad \textit{(eq. 8)}$$

$$K_{VCO} = 0.35 \times \omega_C \qquad \textit{(eq. 9)}$$

$$I_{QP} = \left(\frac{0.01875}{RR}\right) \times (63 - X) \qquad \textit{(eq. 10)}$$

TIMING RECOVERY

The data synchronizer uses a fully integrated, fast acquisition, PLL to perform clock recovery from the incoming data stream.

Fast acquisition is obtained by locking the loop to the synthesizer during Write, Servo & Idle modes which minimizes the frequency transient that occurs when the Read mode is initiated. Thus the timing recovery PLL uses two separate phase detectors to drive the loop. A Decision-directed Phase Detector (DDPD) is used in the Read mode and phase-frequency detector (PFD) is used in the Write, Servo, and Idle modes.

The Read mode is initiated by performing a zero phase restart of the VCO, which will force a phase alignment to the incoming 2T (1/4 data-rate) clock pattern. The samples taken immediately after the restart will be used by the DDPD to "coarse adjust" the VCO. After the sync field count has reached the programmed count (AGC + PLL offset), as shown in Diagram 2, the PLL will be switched to tracking mode which reduces the loop bandwidth (BW) by a factor of 2 or 4 depending on the register settings. In the tracking mode the input to the DDPD is taken from the output of the FIR filter.

TIMING RECOVERY OPERATION

In Write or Idle mode, active when the RG (read gate) line is low, the mux selects the PFD as the input to the Q-pump and P-mult circuits. The two signal paths provide Proportional and Integral error terms to the VCO input. The benefit of this architecture is independent control of the loop parameters BW (bandwidth) and ζ (damping factor) via the control registers. The proportional term is controlled by the Damping Ratio DAC and the integral term is controlled by the Data Rate (DR) DAC. The VCO center frequency is set by the DR DAC; as the rate is increased the VCO gain must increase in order to maintain a constant locking range. The damping factor remains constant as the loop BW is changed. The net result of the loop is that it will settle in a constant number of clock cycles independent of the clock period.

The Read mode is initiated by a positive transition on the "RG" line as shown in Diagram 5.

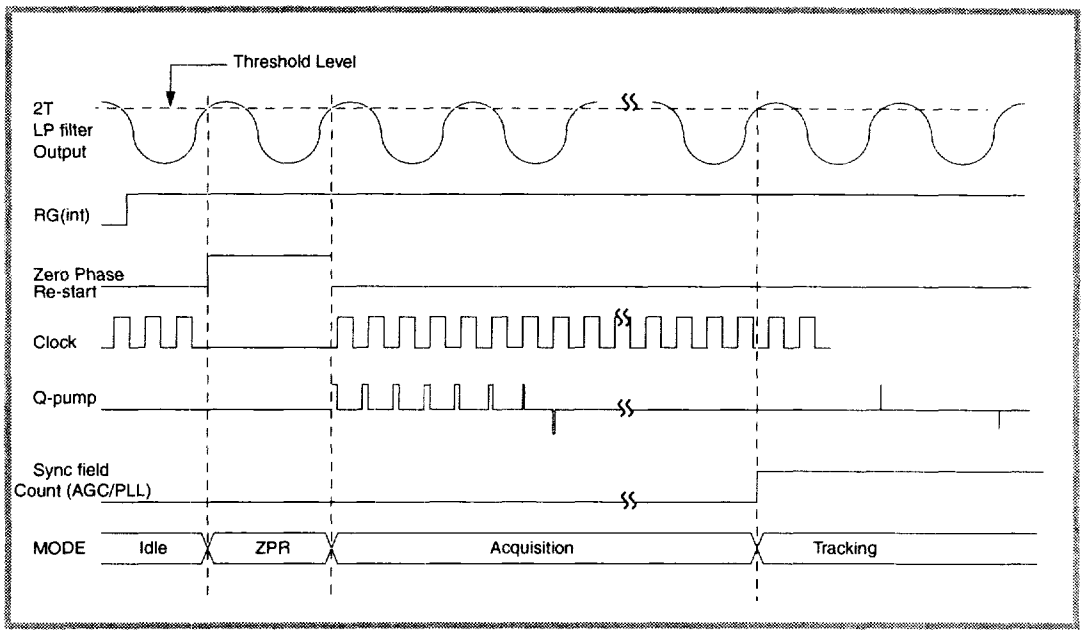


Diagram 5 Timing Recovery Operation

The VCO is held in a low output state when the 2T input signal crosses the threshold set by the Zero Phase Restart DAC. The second time the threshold is crossed the VCO restarts. The threshold is set to align the VCO to the ideal PR4 sample phase of $\Pi/4$, which is 0.707 times the AGC's analog servo voltage V_{TH}. The analog and digital delays in the samplers and the VCO require a slight variation of that sample threshold so a multiplying DAC is used to obtain the optimal set point. Once the VCO restarts, the DDPD output is used as the phase error to drive the PLL. The initial gain will be high to minimize the acquisition time and the computation of the phase error is done with a robust technique which prevents any false lock-up modes. After the sync field count has been reached the error detection mode will be changed to allow for three valid signal levels (only two are used in Acquisition) and the gains are reduced to reduce jitter. Since the AGC gain control is independent the timing control it can be switched at any point after the FIR has taken 7 samples (7-tap filter) and is switched slightly before the timing transition from Acquisition to Tracking. If the DSP mode is in progress this transition will enable the detection of the sync byte.

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WRITE PRECOMPENSATION

The write precompensation circuitry is provided to compensate for media bit shift caused by magnetic nonlinearities. The circuit recognizes six specific write data patterns of 4 channel bit lengths and can add delay in the transition of write data bits to counteract the magnetic non-linearity effect. The magnitude of the time shift is programmable via a Register and is made proportional to the frequency synthesizer's VCO period (i.e. data rate). Since the WPC operation is performed prior to the final T-FF (which is part of the precoding function) only three distinct patterns are decoded. Each of these three patterns may be independently programmed. The precoding operation is included with the WPC circuitry.

Each DAC allows write precompensation delay (Twpc) values to be programmed from 0 to 0.20T with 1.25% resolution as shown in the following equations.

$$Twpc(Pattern1, 3) = (0.013 \bullet Kwp + 0.20 \bullet WPCHR) \bullet T \qquad \textit{(eq. 11)}$$

$$Twpc(Pattern2) = (0.013 \bullet Kwp) \bullet T \qquad \textit{(eq. 12)}$$

where T is the period of the VCO, in nano-seconds, and Kwp is the value of the 4-bit DAC word for any of the three patterns

HBIT is an independently-programmable bit which allows an addition 20% precompensation for patterns 1 and 3. By setting this bit high, patterns 1 and 3 will have a range from 20 to 40 percent of the VCO period. HBIT does not affect pattern 2. If no compensation is desired for any of the three patterns, then that particular DAC word may be set to 0.

The precoder and all internal states in the WPC get reset with the de-assertion of write gate (WG) so that the write path is always in the same state upon assertion of WG. This also prevents any false data from being sent to the preamp during non-write modes.

Pattern	*Data Pattern*	*Write Data Pattern*
1	011	0010/1101
2	101	0110/1001
3	111	0101/1010

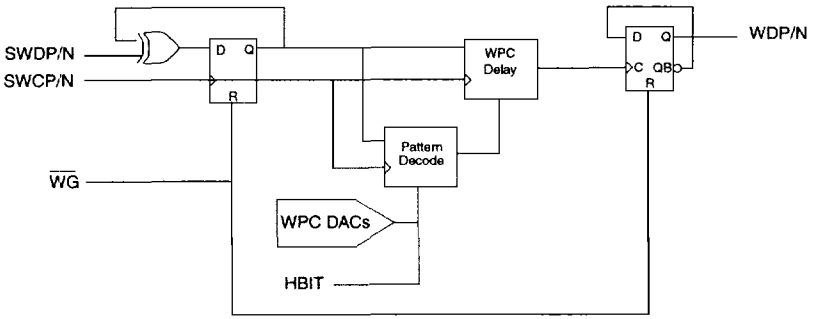

Diagram 6 WPC/Precoder Block Diagram

SERVO DEMODULATOR

The embedded servo demodulator processor extracts the head position error information from the embedded servo bursts using an area detection technique. It supports full quadrature demodulation through the use of an array of four area detector channels. The area detection technique provides improved noise immunity over peak detection. A block diagram for the servo demodulator is shown in Diagram 7.

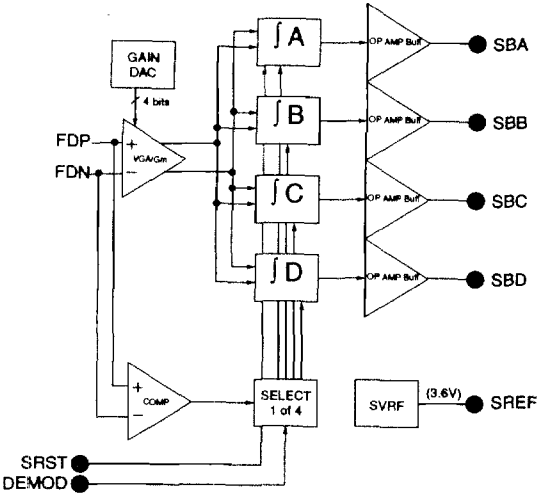

Diagram 7 Servo Demodulator Block Diagram

The demodulator contains a variable gain amplifier, rectifier, four pulse area detectors and required timing logic. The differentiated filtered servo bursts are input to a variable gain amplifier (VGA). The VGA allows the demodulator block to accommodate a wide dynamic range of servo burst amplitudes and process variations of the internal integration capacitors and resistors. The gain range of the VGA is ±40% in steps of 5%, as defined in the servo gain control register. The amplified signal is full-wave rectified and input to an array of four area detectors. The area detector consists of a gm stage driving an on-chip integration capacitor. Note that the ±30% tolerance of the on-chip capacitors and gm block can be calibrated by adjusting the gain of the VGA.

Each area detector is selectively enabled when the DEMOD control input goes high and integrates the pulse voltage amplitude of the servo burst. After the burst pulses have been integrated, the DEMOD signal is brought low, the area detector is disabled and the final integrated voltage is held. Consecutive cycles of the DEMOD pin cause the A, B, C, and D area detectors to sample the input waveform. Upon the low level of SRST, the servo burst outputs are reset to the SREF voltage.

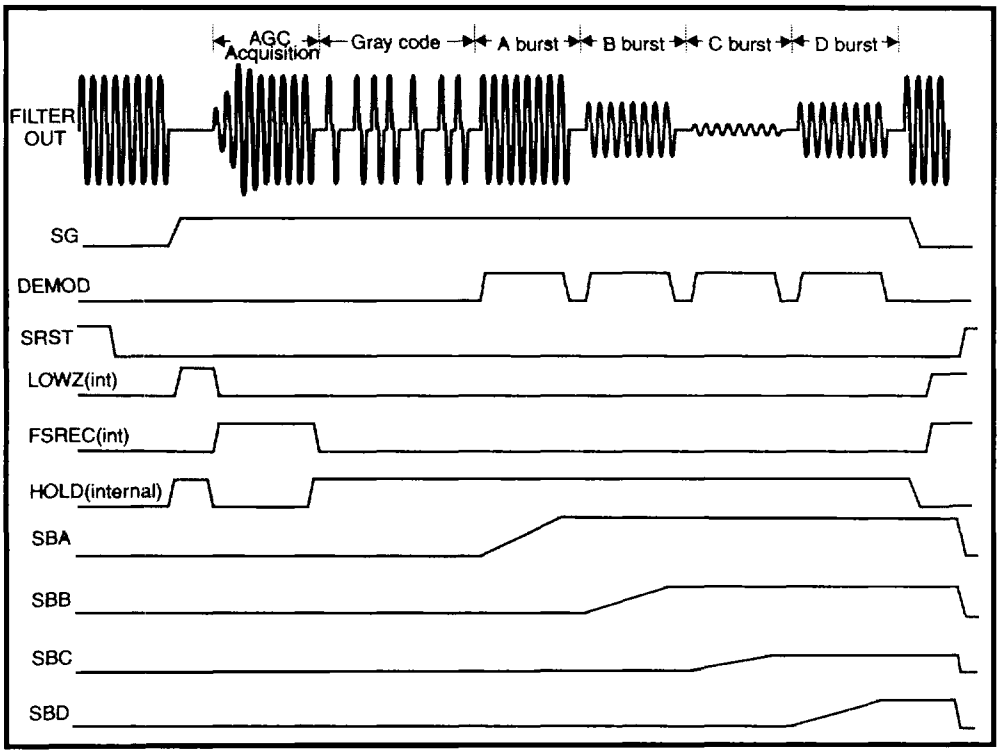

Diagram 8 Servo Timing Diagram

DIGITAL BACK END

The VM65060's digital back end section consists of the following blocks: byte-wide (eight bit) parallel data interface, nibble-wide (four bit) parallel data interface, 8-bit wide scrambler/descrambler with PRNG, 8/9 (0, 4, 4) encoder/decoder, parallel/serial circuitry, sync byte circuitry, channel clock divider and mode control circuitry. These blocks are described below.

8-bit (Byte-Wide) Bidirectional NRZ interface

The 8-bit NRZ interface is a set of eight bidirectional pins that provide the ability to interface with a byte-wide disk controller. Each pin has a TTL level input detector and a tristate TTL level output driver. The input detector is disabled during sleep mode. The output driver is put into high impedance when not driving the NRZ line. These pins, when not driving data out of the digital back end, must be driven by external sources (as all CMOS inputs).

In write mode, the NRZ data can be latched-in on the rising edge of WCLK or either edge of RCLK. The setting of two control register bits determines the configuration. The length of the VCO Sync Field is user-determined. Internal circuitry ignores the first two NRZ bytes, assuming them to be zero. This allows for a possible late driving of the NRZ bus with respect to the rising edge of WG. The end of the VCO Sync Field, and the start of the SYNC Byte section, is determined by the first non-zero byte strobed into the VM65060. NRZ[8] through NRZ[5] are used for non-zero detection. NRZ[4] through NRZ[1] are not monitored by the non-zero detector circuitry. Thus the MSB half of the first SYNC Byte *must* be non-zero, while the LSB half can be all zero.

In read mode, the NRZ data is driven out on the falling edge of RCLK. When RG goes high, the NRZ interface will drive low until either SYNC byte has been detected. The first non-zero data driven out on the NRZ pins will be either the first User Data word or else the SYNC Byte pattern. The user has the option to precede the User Data with the SYNC Byte pattern.

4-bit (Nibble-Wide) Bidirectional NRZ interface

The operation of the 4-bit NRZ interface is similar to that of the 8-bit interface. The main difference being that only the pins NRZ[4] through NRZ[1] are used, with NRZ[8] through NRZ[5] being tied-off by the user. Eight-bit words are still used but they are broken into two 4-bit nibbles. The first nibble is the MSB half and the second nibble is the LSB half. Within the VM65060 the two 4-bit halves are concatenated into a full 8-bit word. During nibble operations the RCLK is run at twice the frequency as the internal byte clock, thus maintaining equivalent byte speed operation.

8-bit wide Scrambler / Descrambler, with PRNG

The Scrambler and Descrambler circuits, which are used to randomize user data, half-add each bit of an 8-bit Pseudo Random Number (PRN) to each bit of the 8-bit user data. The half-adding is done through the use of eight XNOR gates. The same PRN is half-added during write and again during read, resulting in the original user data being returned. The PRN comes from a shared Pseudo Random Number Generator (PRNG) which itself is based upon the $X^{10} + X^3 + 1$ polynomial.

At the beginning of write mode the PRNG is initialized to all 0's. The PRNG then generates a PRN of continuous 00_H until it is set with the FF_H seed. This continuous 00_H PRN in turn allows the scrambler to act as inverting buffers on the NRZ's VCO Sync Field during write mode. This causes the continuous 00_H being detected on the NRZ inputs to be inverted into continuous FF_H before entering the Encoder. At the end of the VCO Sync Field the PRNG is set to all 1's. This allows for a maximum run length PRN pattern as well as allowing the scrambler to act as a noninverting buffer on the NRZ's SYNC Bytes and Spacer byte. At the end of the three Sync Byte cycles, the PRNG is enabled into a free-running condition where PRN's are generated and half-added to the User Data until the end of the write mode.

At the beginning of read mode the PRNG is initialized to all 1's. Following the successful detection of a Sync Byte, the PRNG is enabled into a free-running condition where PRN's are generated and half-added to the User Data before being passing on to the NRZ output drivers until the end of the read mode.

During Idle, Sleep, or Direct Test modes the PRNG's clock is disabled to save power. During normal Write or Read modes the PRNG's clock is enabled. The user has the option to not scramble and descramble the User Data by not generating PRN's with the PRNG. When this option is chosen, the PRNG remains set at all 1's throughout the User Data fields, and the scrambler and descrambler circuitries simply buffer the User Data in both the write path and the read path.

8/9 (0, 4, 4) Encoder / Decoder

In order to provide for proper partial response maximum likelihood (PRML) signaling and detection in the recording channel, a run length limited (RLL) code of parameters (0, 4, 4) is being provided. As 8-bit data words are being provided for recording, the simplest (0, 4, 4) RLL code for 8-bit words is to use a set of qualified 9-bit code words. There are 279 qualified 9-bit code words, out of the possible 512 9-bit words. Only 256 of these are required to encode the 8-bit data word. This is known as an 8/9 code. The code word to data word assignments have been made to minimize both logic delay and chip area. Circuitry has been designed to provide for both encoding and decoding the 8-bit data words.

Table 2 and Table 3 show the relationships between the 8-bit data words (shown in hexadecimal notation) and the 9-bit code words (shown in octal notation) incorporated in the encoder circuitry. Unused or invalid codewords are not shown.

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DATA : CODE	DATA : CODE	DATA : CODE	DATA : CODE
00 : 356	40 : 756	80 : 456	C0 : 416
01 : 351	41 : 751	81 : 451	C1 : 411
02 : 357	42 : 222	82 : 457	C2 : 622
03 : 341	43 : 223	83 : 441	C3 : 623
04 : 354	44 : 754	84 : 454	C4 : 414
05 : 355	45 : 755	85 : 455	C5 : 415
06 : 344	46 : 226	86 : 444	C6 : 626
07 : 345	47 : 227	87 : 445	C7 : 627
08 : 353	48 : 753	88 : 453	C8 : 413
09 : 311	49 : 231	89 : 431	C9 : 631
0A : 307	4A : 232	8A : 432	CA : 632
0B : 313	4B : 233	8B : 433	CB : 633
0C : 314	4C : 234	8C : 434	CC : 634
0D : 315	4D : 235	8D : 435	CD : 635
0E : 316	4E : 236	8E : 436	CE : 636
0F : 317	4F : 237	8F : 437	CF : 637
10 : 656	50 : 706	90 : 446	D0 : 646
11 : 651	51 : 261	91 : 461	D1 : 661
12 : 657	52 : 262	92 : 462	D2 : 662
13 : 641	53 : 263	93 : 463	D3 : 663
14 : 654	54 : 264	94 : 464	D4 : 664
15 : 655	55 : 265	95 : 465	D5 : 665
16 : 644	56 : 266	96 : 466	D6 : 666
17 : 645	57 : 267	97 : 467	D7 : 667
18 : 653	58 : 703	98 : 443	D8 : 643
19 : 611	59 : 271	99 : 471	D9 : 671
1A : 607	5A : 272	9A : 472	DA : 672
1B : 613	5B : 273	9B : 473	DB : 673
1C : 614	5C : 274	9C : 474	DC : 674
1D : 615	5D : 275	9D : 475	DD : 675
1E : 616	5E : 276	9E : 476	DE : 676
1F : 617	5F : 277	9F : 477	DF : 677
20 : 156	60 : 116	A0 : 556	E0 : 516
21 : 151	61 : 111	A1 : 551	E1 : 511
22 : 157	62 : 322	A2 : 557	E2 : 722
23 : 141	63 : 323	A3 : 541	E3 : 723
24 : 154	64 : 114	A4 : 554	E4 : 514
25 : 155	65 : 115	A5 : 555	E5 : 515
26 : 144	66 : 326	A6 : 544	E6 : 726
27 : 145	67 : 327	A7 : 545	E7 : 727
28 : 153	68 : 113	A8 : 553	E8 : 513
29 : 131	69 : 331	A9 : 531	E9 : 731
2A : 132	6A : 332	AA : 532	EA : 732
2B : 133	6B : 333	AB : 533	EB : 733
2C : 134	6C : 334	AC : 534	EC : 734
2D : 135	6D : 335	AD : 535	ED : 735
2E : 136	6E : 336	AE : 536	EE : 736
2F : 137	6F : 337	AF : 537	EF : 737
30 : 146	70 : 346	B0 : 546	F0 : 746
31 : 161	71 : 361	B1 : 561	F1 : 761
32 : 162	72 : 362	B2 : 562	F2 : 762
33 : 163	73 : 363	B3 : 563	F3 : 763
34 : 164	74 : 364	B4 : 564	F4 : 764
35 : 165	75 : 365	B5 : 565	F5 : 765
36 : 166	76 : 366	B6 : 566	F6 : 766
37 : 167	77 : 367	B7 : 567	F7 : 767
38 : 143	78 : 343	B8 : 543	F8 : 743
39 : 171	79 : 371	B9 : 571	F9 : 771
3A : 172	7A : 372	BA : 572	FA : 772
3B : 173	7B : 373	BB : 573	FB : 773
3C : 174	7C : 374	BC : 574	FC : 774
3D : 175	7D : 375	BD : 575	FD : 775
3E : 176	7E : 376	BE : 576	FE : 776
3F : 177	7F : 377	BF : 577	FF : 777

Table 2 8-bit Data Word (hexadecimal) to 9-bit Code Word (octal)

CODE : DATA	CODE : DATA	CODE : DATA	CODE : DATA
111 : 61	313 : 0B	461 : 91	633 : CB
113 : 68	314 : 0C	462 : 92	634 : CC
114 : 64	315 : 0D	463 : 93	635 : CD
115 : 65	316 : 0E	464 : 94	636 : CE
116 : 60	317 : 0F	465 : 95	637 : CF
131 : 29	322 : 62	466 : 96	641 : 13
132 : 2A	323 : 63	467 : 97	643 : D8
133 : 2B	326 : 66	471 : 99	644 : 16
134 : 2C	327 : 67	472 : 9A	645 : 17
135 : 2D	331 : 69	473 : 9B	646 : D0
136 : 2E	332 : 6A	474 : 9C	651 : 11
137 : 2F	333 : 6B	475 : 9D	653 : 18
141 : 23	334 : 6C	476 : 9E	654 : 14
143 : 38	335 : 6D	477 : 9F	655 : 15
144 : 26	336 : 6E	511 : E1	656 : 10
145 : 27	337 : 6F	513 : E8	657 : 12
146 : 30	341 : 03	514 : E4	661 : D1
151 : 21	343 : 78	515 : E5	662 : D2
153 : 28	344 : 06	516 : E0	663 : D3
154 : 24	345 : 07	531 : A9	664 : D4
155 : 25	346 : 70	532 : AA	665 : D5
156 : 20	351 : 01	533 : AB	666 : D6
157 : 22	353 : 08	534 : AC	667 : D7
161 : 31	354 : 04	535 : AD	671 : D9
162 : 32	355 : 05	536 : AE	672 : DA
163 : 33	356 : 00	537 : AF	673 : DB
164 : 34	357 : 02	541 : A3	674 : DC
165 : 35	361 : 71	543 : B8	675 : DD
166 : 36	362 : 72	544 : A6	676 : DE
167 : 37	363 : 73	545 : A7	677 : DF
171 : 39	364 : 74	546 : B0	703 : 58
172 : 3A	365 : 75	551 : A1	706 : 50
173 : 3B	366 : 76	553 : A8	722 : E2
174 : 3C	367 : 77	554 : A4	723 : E3
175 : 3D	371 : 79	555 : A5	726 : E6
176 : 3E	372 : 7A	556 : A0	727 : E7
177 : 3F	373 : 7B	557 : A2	731 : E9
222 : 42	374 : 7C	561 : B1	732 : EA
223 : 43	375 : 7D	562 : B2	733 : EB
226 : 46	376 : 7E	563 : B3	734 : EC
227 : 47	377 : 7F	564 : B4	735 : ED
231 : 49	411 : C1	565 : B5	736 : EE
232 : 4A	413 : C8	566 : B6	737 : EF
233 : 4B	414 : C4	567 : B7	743 : F8
234 : 4C	415 : C5	571 : B9	746 : F0
235 : 4D	416 : C0	572 : BA	751 : 41
236 : 4E	431 : 89	573 : BB	753 : 48
237 : 4F	432 : 8A	574 : BC	754 : 44
261 : 51	433 : 8B	575 : BD	755 : 45
262 : 52	434 : 8C	576 : BE	756 : 40
263 : 53	435 : 8D	577 : BF	761 : F1
264 : 54	436 : 8E	607 : 1A	762 : F2
265 : 55	437 : 8F	611 : 19	763 : F3
266 : 56	441 : 83	613 : 1B	764 : F4
267 : 57	443 : 98	614 : 1C	765 : F5
271 : 59	444 : 86	615 : 1D	766 : F6
272 : 5A	445 : 87	616 : 1E	767 : F7
273 : 5B	446 : 90	617 : 1F	771 : F9
274 : 5C	451 : 81	622 : C2	772 : FA
275 : 5D	453 : 88	623 : C3	773 : FB
276 : 5E	454 : 84	626 : C6	774 : FC
277 : 5F	455 : 85	627 : C7	775 : FD
307 : 08	456 : 80	631 : C9	776 : FE
311 : 09	457 : 82	632 : CA	777 : FF

Table 3 9-bit Code Word (octal) to 8-bit Data Word (hexadecimal)

279 of 512 9-bit words meet the (0, 4, 4) RLL requirement. Of these, only 256 are needed to encode the 256 8-bit data words. Therefore many breaks occur in the codeword sequence of Table 3.

The 256 codewords that are utilized (out of the 279 valid codewords) were chosen so as to be able to realize encoder and decoder logic circuitry in the simplest and fastest means possible. A maximum of five gate delays through the encoder and through the decoder have been realized.

Valid codewords do not allow for runs of more than four zeros in either the data sequence, or in either the even indexed or odd indexed interleaves. Codewords that have zero pairs at either end, in either the main sequence or in either of the interleaves are allowed. Therefore, codewords with zero triplets at either end of any sequence are invalid.

Invalid codeword configurations are identified below.

$000\ XXX\ XXX_B$ $0XX_O$ | $XX0\ 000\ 0XX_B$ 603_O | $XXX\ XXX\ 000_B$ $XX0_O$

$0X0\ X0X\ XXX_B$

$20X_O$ $24X_O$
$21X_O$ $25X_O$

$XXX\ X0X\ 0X0_B$

$X02_O$ $X42_O$
$X12_O$ $X52_O$

$X0X\ 0X0\ XXX_B$

$10X_O$ $42X_O$
$12X_O$ $50X_O$
$40X_O$ $52X_O$

$XXX\ 0X0\ X0X_B$

$X01_O$ $X21_O$
$X04_O$ $X24_O$
$X05_O$ $X25_O$

Invalid cases are shown in Table 4. A total of 233 9-bit words are invalid.

CODE : DATA	CODE : DATA	CODE : DATA	CODE : DATA
117 : 62	051 : 01	220 : 40	460 : 90
147 : 3A	052 : 08	221 : 41	470 : 98
303 : 08	053 : 08	224 : 44	500 : E2
306 : 00	054 : 04	225 : 45	501 : E3
347 : 7A	055 : 05	230 : 48	502 : E8
417 : C2	056 : 00	240 : 12	503 : E8
447 : 9A	057 : 02	241 : 13	504 : E6
517 : E2	060 : 10	242 : 58	505 : E7
547 : BA	061 : 11	243 : 58	506 : E0
606 : 10	062 : 12	244 : 16	507 : EA
647 : DA	063 : 13	245 : 17	510 : E0
707 : 5A	064 : 14	246 : 50	512 : E8
711 : 59	065 : 15	247 : 5A	520 : A0
713 : 5B	066 : 16	250 : 10	521 : A1
714 : 5C	067 : 17	251 : 11	522 : A2
715 : 5D	070 : 18	252 : 18	523 : A3
716 : 5E	071 : 19	253 : 18	524 : A4
717 : 5F	072 : 1A	254 : 14	525 : A5
741 : 43	073 : 1B	255 : 15	526 : A6
744 : 46	074 : 1C	256 : 10	527 : A7
745 : 47	075 : 1D	257 : 12	530 : A8
747 : FA	076 : 1E	260 : 50	540 : A2
757 : 42	077 : 1F	270 : 58	542 : B8
000 : 42	100 : 62	300 : 02	550 : A0
001 : 43	101 : 63	301 : 03	552 : A8
002 : 48	102 : 68	302 : 08	560 : B0
003 : 48	103 : 68	304 : 06	570 : B8
004 : 46	104 : 66	305 : 07	600 : 12
005 : 47	105 : 67	310 : 08	601 : 13
006 : 40	106 : 60	312 : 0A	602 : 18
007 : 4A	107 : 6A	320 : 60	603 : 18
010 : 40	110 : 60	321 : 61	604 : 16
011 : 41	112 : 68	324 : 64	605 : 17
012 : 48	120 : 20	325 : 65	610 : 18
013 : 48	121 : 21	330 : 68	612 : 1A
014 : 44	122 : 22	340 : 02	620 : C0
015 : 45	123 : 23	342 : 78	621 : C1
016 : 40	124 : 24	350 : 00	624 : C4
017 : 42	125 : 25	352 : 04	625 : C5
020 : 00	126 : 26	360 : 70	630 : C8
021 : 01	127 : 27	370 : 78	640 : 12
022 : 02	130 : 28	400 : C2	642 : D8
023 : 03	140 : 22	401 : C3	650 : 10
024 : 04	142 : 38	402 : C8	652 : 18
025 : 05	150 : 20	403 : C8	660 : D0
026 : 06	152 : 28	404 : C6	670 : D8
027 : 07	160 : 30	405 : C7	700 : 52
030 : 08	170 : 38	406 : C0	701 : 53
031 : 09	200 : 12	407 : CA	702 : 58
032 : 0A	201 : 13	410 : C0	704 : 56
033 : 0B	202 : 18	412 : C8	705 : 57
034 : 0C	203 : 18	420 : 80	710 : 58
035 : 0D	204 : 16	421 : 81	712 : 5A
036 : 0E	205 : 17	422 : 82	720 : E0
037 : 0F	206 : 10	423 : 83	721 : E1
040 : 02	207 : 1A	424 : 84	724 : E4
041 : 03	210 : 18	425 : 85	725 : E5
042 : 18	211 : 19	426 : 86	730 : E8
043 : 18	212 : 1A	427 : 87	740 : 42
044 : 06	213 : 1B	430 : 88	742 : F8
045 : 07	214 : 1C	440 : 82	750 : 40
046 : 10	215 : 1D	442 : 98	752 : 48
047 : 1A	216 : 1E	450 : 80	760 : F0
050 : 00	217 : 1F	452 : 88	770 : F8

Table 4 Unused and Invalid 9-bit Word (octal) to 8-bit Word (hex)

Parallel-to-Serial and Serial-to-Parallel converters

One of the main features of the digital back end is the conversion of 8-bit parallel NRZ data into a high speed serial bit stream, and the conversion of high speed serial data back to 8-bit parallel NRZ data. In write operations a 9-bit word is loaded in parallel onto the high speed serial write data bit stream every ninth channel clock cycle (every eighth in direct test) and then shifted out to the analog front end. And in read operations nine bits of the high speed read data bit stream are captured in parallel every ninth channel clock cycle (every eighth in direct test) and then passed toward the NRZ pins.

The coordination of these transfers is timing critical. In write operations, the transfer takes place as a parallel load of a serial shift register for a single channel clock cycle during the second half of the internal NRZ write clock period. This allows the parallel data plenty of time to have settled prior to its parallel loading into the serial shift register of the high speed write data bit stream.

In read operations, the transfer only takes place following a successful SYNC Byte word detection so that the RCLK will have been synchronized with the user data word boundaries. Once synchronization of the clock has been achieved, the user data is captured in 9-bit segments once every ninth cycle and made available to the decoder, descrambler, and NRZ output pins. In direct test the user data is captured in 8-bit segments once every eighth cycle and bypasses the decoder and descrambler on its way to the NRZ output pins.

SYNC Byte Detector, programmable

Detection of a SYNC Byte word in read mode is used to set the framing of the user data field into user data words that can then be passed on to the disk controller. The VCO Sync field, which precedes the SYNC Byte words, is searched at the beginning of read mode by the SYNC Byte detector circuitry. It is looking for either of the two SYNC Byte words to come along in the serial data stream so that the proper data word framing, or boundaries, can be determined and set.

In normal operation, the SYNC Byte words are two 9-bit words separated by a 9-bit spacer word, while in direct test operation they are the combination of 8-bit SYNC Byte words and the last bit of the VCO Sync Field, '1', for SB1 and the last bit of the 8-bit spacer word, '0', for SB2. In order to detect the SYNC Byte words, the detector circuitry must be informed for which pattern to search. The 9-bit SYNC Byte pattern for which to search is stored in the control register. This pattern is for the second SYNC Byte word, SB2, while the pattern for SB1 is the bit by bit inverse of SB2.

The SYNC Byte detector circuitry consists of a bank of nine XNOR/XOR gates. Each gate interrogates a single bit of the serial bit stream, resulting in a string of nine bits being checked in parallel. Each bit is checked with respect to the corresponding bit stored in the control register. If all nine serial stream bits mismatch their corresponding stored pattern, XNOR's $\Rightarrow$ 1, and SB1 is said to be found. If all nine bits are matched, XOR's $\Rightarrow$ 0, and SB2 is said to be found.

Upon detecting either SB1 or SB2 in the serial bit stream, a synchronization signal is passed on to the channel clock divider circuitry so that the divided clock can be adjusted for framing the user data word boundaries. Also, a blocking signal is set that stops the detector circuitry from continuing to search for and detecting subsequent patterns that also match the SYNC Byte patterns. In addition, a SYNC Byte Flag is set and eventually driven out on the SBF pin.

If the SYNC Byte detector circuitry fails to detect either SYNC Byte pattern as it passes through in the serial data stream, possibly due to a corrupted bit stream, the search is allowed to continue until the end of the read mode during which a possible false detection of user data patterns as the SYNC Byte words might occur. Acknowledging the failure to detect the SYNC Byte during the proper portion of the Read Mode is left up to the Controller chip.

The user has the option of requiring patterns SB1 and SB2 to *both* be detected prior to the passing of user data words on to the disk controller. In this way the user can configure tighter error tolerances during the SYNC Byte zone by requiring that both SYNC Bytes must be error free, rather than just one.

As there is a relationship between SB1 and SB2, they must be coordinated when chosen and written. Two tables have been include here to aid in determining pairs of SYNC Bytes.

Table 5 lists the 110 possible SYNC Byte pairs that can be used in 8/9 encoded normal modes. These all have SB1 and SB2 that are the bit-by-bit inverses of each other. SB1's that have NRZ[8:5]= 0 are excluded from this list as they would not be detected properly by the non-zero detector in the write path.

SB1			SB2		
Hex	Oct	Binary	Binary	Oct	Hex
13	641	110100001	001011110	136	2E
16	644	110100100	001011011	133	2B
17	645	110100101	001011010	132	2A
19	611	110001001	001110110	166	36
1B	613	110001011	001110100	164	34
1C	614	110001100	001110011	163	33
1D	615	110001101	001110010	162	32
1E	616	110001110	001110001	161	31
21	151	001101001	110010110	626	C6
23	141	001100001	110011110	636	CE
24	154	001101100	110010011	623	C3
25	155	001101101	110010010	622	C2
26	144	001100100	110011011	633	CB
27	145	001100101	110011010	632	CA
29	131	001011001	110100110	646	D0
2A	132	001011010	110100101	645	17
2B	133	001011011	110100100	644	16
2C	134	001011100	110100011	643	D8
2E	136	001011110	110100001	641	13
30	146	001100110	110011001	631	C9
31	161	001110001	110001110	616	1E
32	162	001110010	110001101	615	1D
33	163	001110011	110001100	614	1C
34	164	001110100	110001011	613	1B
36	166	001110110	110001001	611	19
38	143	001100011	110011100	634	CC
42	222	010010010	101101101	555	A5
43	223	010010011	101101100	554	A4
46	226	010010110	101101001	551	A1
49	231	010011001	101100110	546	B0
4A	232	010011010	101100101	545	A7
4B	233	010011011	101100100	544	A6
4C	234	010011100	101100011	543	B8
4E	236	010011110	101100001	541	A3
51	261	010110001	101001110	516	E0
52	262	010110010	101001101	515	E5
53	263	010110011	101001100	514	E4
54	264	010110100	101001011	513	E8
56	266	010110110	101001001	511	E1
60	116	001001110	110110001	661	D1
61	111	001001001	110110110	666	D6
62	322	011010010	100101101	455	85
63	323	011010011	100101100	454	84
64	114	001001100	110110011	663	D3
65	115	001001101	110110010	662	D2
66	326	011010110	100101001	451	81
68	113	001001011	110110100	664	D4
69	331	011011001	100100110	446	90
6A	332	011011010	100100101	445	87
6B	333	011011011	100100100	444	86
6C	334	011011100	100100011	443	98
6E	336	011011110	100100001	441	83
70	346	011100110	100011001	431	89
71	361	011110001	100001110	416	C0
72	362	011110010	100001101	415	C5

SB1			SB2		
Hex	Oct	Binary	Binary	Oct	Hex
73	363	011110011	100001100	414	C4
74	364	011110100	100001011	413	C8
76	366	011110110	100001001	411	C1
78	343	011100011	100011100	434	8C
81	451	100101001	011010110	326	66
83	441	100100001	011011110	336	6E
84	454	100101100	011010011	323	63
85	455	100101101	011010010	322	62
86	444	100100100	011011011	333	6B
87	445	100100101	011011010	332	6A
89	431	100011001	011100110	346	70
8A	432	100011010	011100101	345	07
8B	433	100011011	011100100	344	06
8C	434	100011100	011100011	343	78
8E	436	100011110	011100001	341	03
90	446	100100110	011011001	331	69
91	461	100110001	011001110	316	0E
92	462	100110010	011001101	315	0D
93	463	100110011	011001100	314	0C
94	464	100110100	011001011	313	0B
96	466	100110110	011001001	311	09
98	443	100100011	011011100	334	6C
A1	551	101101001	010010110	226	46
A3	541	101100001	010011110	236	4E
A4	554	101101100	010010011	223	43
A5	555	101101101	010010010	222	42
A6	544	101100100	010011011	233	4B
A7	545	101100101	010011010	232	4A
B0	546	101100110	010011001	231	49
B8	543	101100011	010011100	234	4C
C0	416	100001110	011110001	361	71
C1	411	100001001	011110110	366	76
C2	622	110010010	001101101	155	25
C3	623	110010011	001101100	154	24
C4	414	100001100	011110011	363	73
C5	415	100001101	011110010	362	72
C6	626	110010110	001101001	151	21
C8	413	100001011	011110100	364	74
C9	631	110011001	001100110	146	30
CA	632	110011010	001100101	145	27
CB	633	110011011	001100100	144	26
CC	634	110011100	001100011	143	38
CE	636	110011110	001100001	141	23
D0	646	110100110	001011001	131	29
D1	661	110110001	001001110	116	60
D2	662	110110010	001001101	115	65
D3	663	110110011	001001100	114	64
D4	664	110110100	001001011	113	68
D6	666	110110110	001001001	111	61
D8	643	110100011	001011100	134	2C
E0	516	101001110	010110001	261	51
E1	511	101001001	010110110	266	56
E4	514	101001100	010110011	263	53
E5	515	101001101	010110010	262	52
E8	513	101001011	010110100	264	54

Table 5 SYNC Byte Pairs for 8/9 (0, 4, 4) Normal

Table 6 shows the 239 possible SYNC Byte pairs that can be used in 8/8 nonencoded direct test modes.

SB1		SB2	
Hex	Binary	Binary	Hex
~~00~~	~~(1)00000000~~	~~(0)11111111~~	~~FF~~
~~01~~	~~(1)00000001~~	~~(0)11111110~~	~~FE~~
~~02~~	~~(1)00000010~~	~~(0)11111101~~	~~FD~~
~~03~~	~~(1)00000011~~	~~(0)11111100~~	~~FC~~
~~04~~	~~(1)00000100~~	~~(0)11111011~~	~~FB~~
~~05~~	~~(1)00000101~~	~~(0)11111010~~	~~FA~~
~~06~~	~~(1)00000110~~	~~(0)11111001~~	~~F9~~
~~07~~	~~(1)00000111~~	~~(0)11111000~~	~~F8~~
~~08~~	~~(1)00001000~~	~~(0)11110111~~	~~F7~~
~~09~~	~~(1)00001001~~	~~(0)11110110~~	~~F6~~
~~0A~~	~~(1)00001010~~	~~(0)11110101~~	~~F5~~
~~0B~~	~~(1)00001011~~	~~(0)11110100~~	~~F4~~
~~0C~~	~~(1)00001100~~	~~(0)11110011~~	~~F3~~
~~0D~~	~~(1)00001101~~	~~(0)11110010~~	~~F2~~
~~0E~~	~~(1)00001110~~	~~(0)11110001~~	~~F1~~
~~0F~~	~~(1)00001111~~	~~(0)11110000~~	~~F0~~
10	(1)00010000	(0)11101111	EF
11	(1)00010001	(0)11101110	EE
12	(1)00010010	(0)11101101	ED
13	(1)00010011	(0)11101100	EC
14	(1)00010100	(0)11101011	EB
15	(1)00010101	(0)11101010	EA
16	(1)00010110	(0)11101001	E9
17	(1)00010111	(0)11101000	E8
18	(1)00011000	(0)11100111	E7
19	(1)00011001	(0)11100110	E6
1A	(1)00011010	(0)11100101	E5
1B	(1)00011011	(0)11100100	E4
1C	(1)00011100	(0)11100011	E3
1D	(1)00011101	(0)11100010	E2
1E	(1)00011110	(0)11100001	E1
1F	(1)00011111	(0)11100000	E0
20	(1)00100000	(0)11011111	DF
21	(1)00100001	(0)11011110	DE
:	:	:	:
:	:	:	:
:	:	:	:
EE	(1)11101110	(0)00010001	11
EF	(1)11101111	(0)00010000	10
F0	(1)11110000	(0)00001111	0F
F1	(1)11110001	(0)00001110	0E
F2	(1)11110010	(0)00001101	0D
F3	(1)11110011	(0)00001100	0C
F4	(1)11110100	(0)00001011	0B
F5	(1)11110101	(0)00001010	0A
F6	(1)11110110	(0)00001001	09
F7	(1)11110111	(0)00001000	08
F8	(1)11111000	(0)00000111	07
F9	(1)11111001	(0)00000110	06
FA	(1)11111010	(0)00000101	05
FB	(1)11111011	(0)00000100	04
FC	(1)11111100	(0)00000011	03
FD	(1)11111101	(0)00000010	02
FE	(1)11111110	(0)00000001	01
~~FF~~	~~(1)11111111~~	~~(0)00000000~~	~~00~~

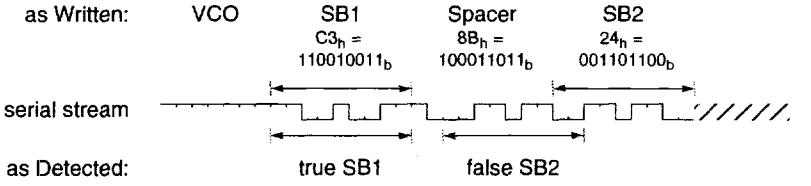
Table 6 SYNC Byte Pairs for Direct Test (8-Bit)

These also have SB1 and SB2 that are the bit-by-bit inverses of each other; SB1's that have NRZ[8:5]= 0, along with the indiscernible case of all 1's and all 0's, have been crossed out in the table. The MSB 9th bits of both SB1 and SB2 are shown in parentheses to shown that for SB1 a '1' is added from the VCO Sync field, and for SB2 a '0' is added from the Spacer word. In both tables it is the 9-bit binary SB2 that must be stored in the control register.

It should be noted that the Spacer word plays a more important role than simply separating SB1 and SB2. Although it separates the two sync bytes so that a bit error late in SB1 does not also corrupt SB2 (resulting in failure to synchronize), it performs an additional function. The LSB of the Spacer word completes the SB2 pattern (which here must be a '0'), as seen in the non-encoded direct test case.

In addition, care must be taken in selecting a Spacer word that coordinates with the SB1 and SB2 patterns so as to not allow a false detection of SB2.

The following example illustrates how an unfortunate choice of SB1, Spacer, and SB2 words can lead to problems. SB2 was chosen to be 24_h, which means (per Table 5) that SB1 would then be $C3_h$. A Spacer word of $8B_h$ was also chosen. How these three words combine into a serial bit stream is shown below.



The problem with this combination of choices is that it results in the SB2 bit patterns showing up more than once in the bit stream. An additional, and false, SB2 is noted below the bit stream, due to the combination of the Spacer and the SB2 words. If a bit error were to foul SB1, or if the user chose to require both SYNC Bytes, then the false SB2 would be detected resulting in an incorrect clock synchronization and data word framing.

This illustrates that a user must study his choice of SB1, Spacer, and SB2 words and examine their resultant serial bit stream, checking for possible false or alias patterns. This is equally true for 8/9 encoded normal mode and for 8/8 non-encoded direct test mode, where the use of the last VCO '1' and last Spacer bit '0' are used to complete the SB1 and SB2 patterns.

The user also has the option to forego SYNC Byte detection and framing altogether. In this option the serial bit stream is not searched for the SB1 and SB2 patterns, the RCLK is not synchronized to anything, and the serial bit stream is simply captured in sequential eight bit sections and passed out to the NRZ pins. This is intended as a 'last resort' option when the serial bit stream is so corrupted that SYNC Byte words can not be detected for use in framing.

Channel clock divider

The base (or channel rate) clock for the digital back end write or read operations comes from the frequency synthesizer (or timing recovery) in the analog front end. The maximum frequency for this clock is beyond 202.5MHz (which is 9/8 x 180Mbit/sec, where 180Mbit/sec is the NRZ bit rate or frequency). This same clock is echoed by the digital back end during write mode operations as the serial write clock to strobe serial write data out of the digital back end and into the analog front end.

The minimum pulse width (high or low) for RCLK in byte mode is four channel-rate clock periods, regardless of whether the chip is in normal operational mode or direct test mode, or whether RCLK is free-running or synchronizing up to the SYNC Byte words. In Direct Test (÷ 8) both high and low pulses of RCLK are four channel-rate clock periods. In normal operation (÷ 9) the high pulse remains at four while the low pulse is expanded out to five channel rate clock periods.

For nibble mode, the minimum pulse width (high or low) for RCLK in byte mode is two channel-rate clock periods. This, too, is regardless of whether the chip is in normal operational mode or direct test mode, or whether RCLK is free-running or synchronizing up to the SYNC Byte words. In Direct Test both high and low pulses of RCLK are two channel-rate clock periods. In normal operation the low pulses remain at two while the high pulses alternate between two and three channel-rate clock periods. Thus the normal nibble clock period alternates between four and five channel clock periods just as the normal byte clock pulses alternate between four high and five low.

The NRZ read clock, RCLK, is used to strobe parallel NRZ data out of the VM65060 to the disk controller on the falling edge. This same clock is used to strobe parallel NRZ data into the VM65060. Either edge of the RCLK output can be selected and used to accommodate for phase delays either in the controller chip or in the NRZ interconnect lines. Also, an 'echo' of the RCLK output, supplied back to the WCLK input, can be used to strobe NRZ data in using the WCLK input's rising edge.

When synchronization occurs at a SYNC Byte word, either the low or the high pulse of one RCLK period is expanded per the diagrams below. Short pulse glitches during synchronization are thus not allowed to happen.

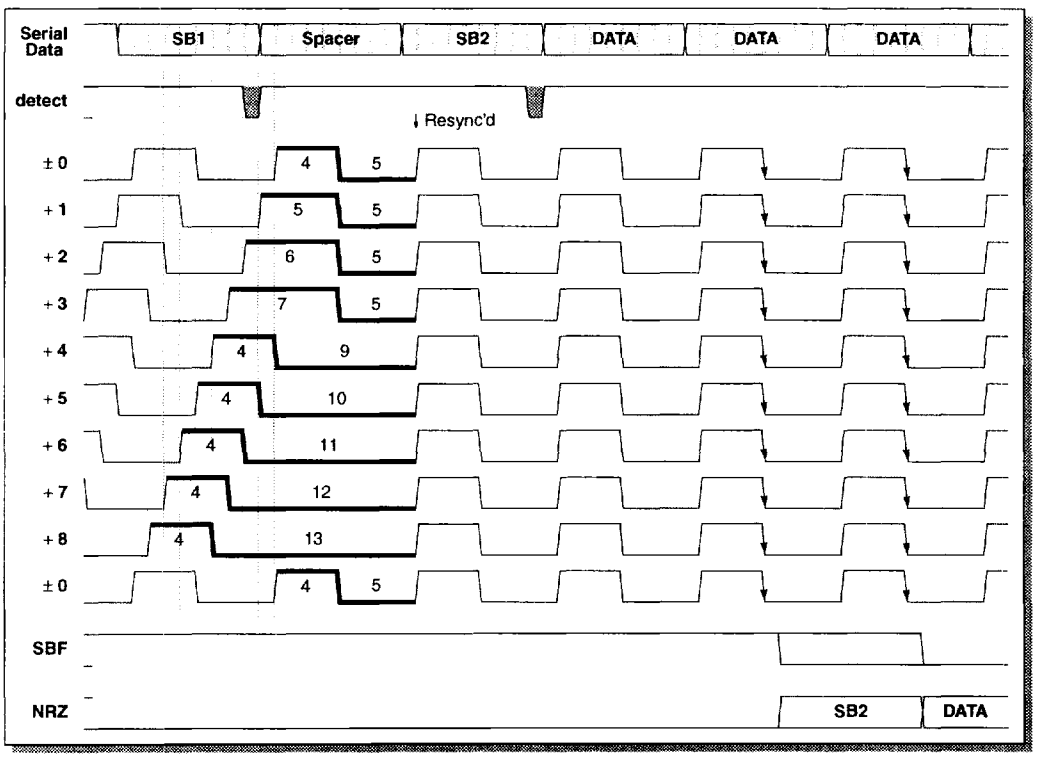


Diagram 9a RCLK Synchronization Cases (Byte-Wide)

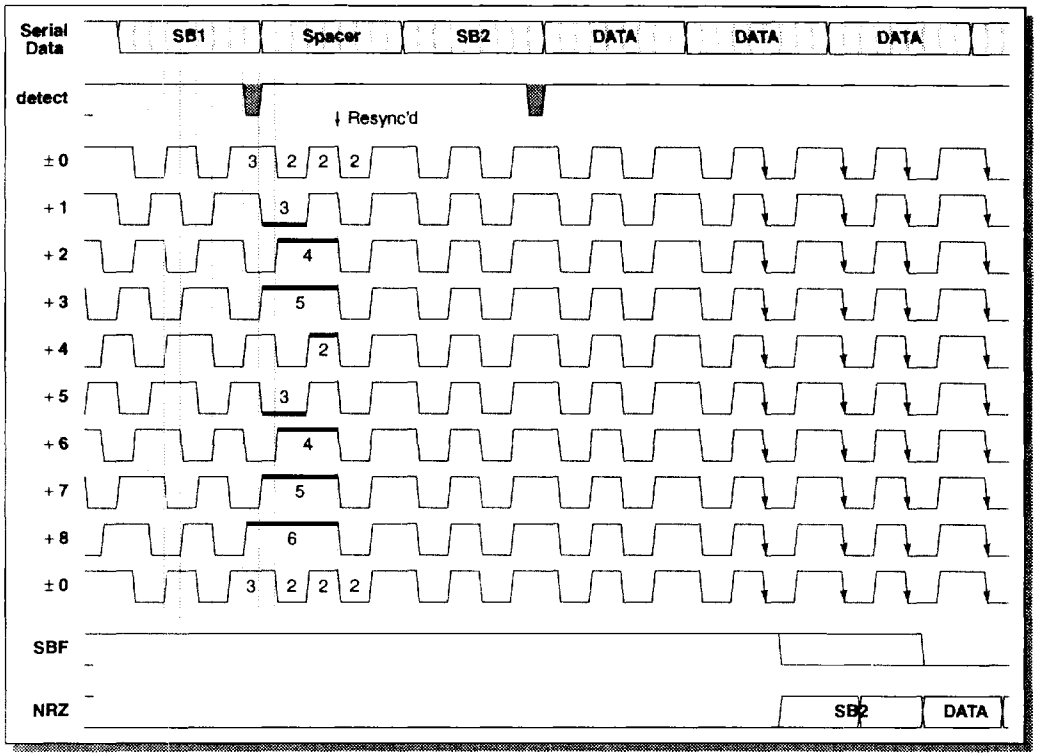


Diagram 9b RCLK Synchronization Cases (Nibble-Wide)

The channel clock divider circuitry consists of a 4-bit counter that rolls over after either eight or nine clock cycles, depending on the setting of the DT bit in the serial control register. The rollover, or clearing, of the counter is based on the established count length or on the detection of a SYNC Byte word. When a SYNC Byte word is detected, the counter is cleared regardless of where it is in the count. The RCLK is created through the use of a synchronous set/reset flip flop with setting and resetting based on various decoded count values of the counter. The use of this flip flop eliminates any clock glitches during synchronization. The clearing of the counter due to the detection of a SYNC Byte words may cause either a second reset to follow an earlier reset resulting in an extended low pulse, or a second set to follow an earlier set resulting in an extended high pulse. There is no case where either pulse would be shortened due to synchronization.

The clock divider circuitry also creates the pulses used to control the parallel-to-serial and the serial-to-parallel transfers of data. These pulses are framed up with the incoming NRZ data words (with the first non-zero word) for write operations, and with the SYNC byte words for read operations.

WCLK Input

The WCLK input provides an optional input strobe for parallel NRZ data being written into the digital back end. The rising edge of this input is used as the strobing edge. The Control Register bit EXT is used to select the WCLK option. The signal sent to the WCLK input must be a copy, or echo, of the RCLK output. An externally-generated signal replicating the RCLK frequency is not acceptable. The RCLK output itself may be tied back into the WCLK input, but a more common practice is for the RCLK output to drive into a controller chip, used there to strobe out NRZ data; the controller then "turns around" the received RCLK and sends it back to the VM65060, along with the NRZ data, as the WCLK signal.

Initialize Clock Maker (ICM) Input

In order to synchronize testing of the digital back end, the Clock Divider circuitry needs to be initialized to a known starting point and then released.

The Control Register bit VTC2 can be used for this purpose. but this requires writing the bit twice. An alternate method is provided via the ICM input pin. A '1' on ICM initializes the clock divider, and a falling edge releases it to respond to serial clock pulses. Note that the bit VTC2 and the pin ICM must both be low for normal operation of the VM65060.

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

MODE CONTROLLER AND SEQUENCE CONTROLLERS

Four signal pins and three control register bits guide and determine the main operations of the digital back end. The pins are Servo Gate (SG), Read Gate (RG), Write Gate (WG), and Power Down (PD). The control register bits are Direct Test Mode (DTM), No Scramble (NOPR), and Sleep (SLEEP).

SG=X RG=X WG=X PD=X SLEEP bit =1

- ♦ Power Down Mode [PDM]
  - CML logic off
  - NRZ, SG, RG, WG inputs disabled
  - NRZ outputs tristated

⇒ Can exit this PDM only by changing SLEEP bit to '0'.
This should be done with SG=0, RG=0, & WG=0, i.e. into Idle Mode

SG=X RG=X WG=X PD=1 SLEEP bit =0

- ♦ Power Down Mode [PDM]
  - CML logic off
  - NRZ, SG, RG, WG inputs disabled
  - NRZ outputs tristated

⇒ Should exit PDM only with SG=0, RG=0, & WG=0, i.e. into Idle Mode

SG=0 RG=0 WG=0 PD=0 SLEEP bit =0

- ♦ Idle Mode [IM]
  - CML logic on
  - Sequencers initialized but disabled, i.e. not running
  - PRNG initialized but disabled, i.e. not running
  - NRZ inputs disabled
  - NRZ outputs tristated

SG=1 RG=X WG=X PD=0 SLEEP bit =0

- ♦ Servo Mode [SM] (SM ≡ IM for the digital back end)
  - CML logic on
  - Sequencers initialized but disabled, i.e. not running
  - PRNG initialized but disabled, i.e. not running
  - NRZ inputs disabled
  - NRZ outputs tristated

⇒ Should exit SM only with RG=0, & WG=0, i.e. into Idle Mode

SG=0 RG=1 WG=X PD=0 SLEEP bit =0

- ♦ Read Mode [RM]
  - CML logic on
  - NRZ outputs enabled, initially driving low
  - PRNG ready and waiting for enable upon SBF, uses RCLK
  - NRZ inputs disabled

⇒ Should exit RM only with SG=0, & WG=0, i.e. into Idle Mode
⇒ Should enter RM only with SG=0, & WG=0, i.e. from Idle Mode

SG=0 RG=0 WG=1 PD=0 SLEEP bit =0

- ♦ Write Mode [WM]
  - CML logic on
  - PRNG ready and waiting for enable upon NZD, uses internal WCLK (RCLK ↑ or RCLK ↓)
  - NRZ inputs enabled
  - NRZ outputs tristated

⇒ Should exit WM only with SG=0, & RG=0, i.e. into Idle Mode
⇒ Should enter WM only with SG=0, & RG=0, i.e. from Idle Mode

As seen above, the Sleep bit (SLEEP), when set to a '1', has the effect of overriding the four controlling pins. The No Scramble (NOPR), and Direct Test Mode (DTM) bits only modify the performance and operations within the various modes.

In byte operations (NIB=0) whenever DTM=0 the clock divider circuitry divides the serial channel clock frequency by nine to create RCLK. Whenever DTM=1 the division is changed to eight.

Whenever DTM=1, the PRNG circuitry is also disabled, regardless of the value of NOPR. Whenever DTM=0, the enabling of the PRNG is dependent upon the value of NOPR, with NOPR=1 providing a disable and NOPR=0 providing an enable.

The following diagram shows, in state diagram form, the three operational modes of the digital back end. These modes are Idle / Servo mode, Read mode, and Write mode. Note that Idle and Servo modes are one and the same for the digital back end. This is not the case for the analog front end, where Idle mode is not equivalent to Servo mode. Also shown are the transitions between these modes. The usual and intended transitions are shown with the heavy arrows and control settings in bold. Other possible valid but less standard transitions are shown with dotted arrows.

These transitions are set via the hierarchy: SG overrides RG which overrides WG. These inputs are, by nature, all asynchronous. But there is a relationship between WG input, NRZ input, and the active clock write strobe edge, be it WCLK, RCLK rising, or RCLK falling. The first two input write clock edges following WG rising, or whichever signal put the chip into Write mode, are the two NRZ inputs that are ignored and assumed to be zero, whereas the third clock edge actually strobes in the NRZ inputs that are first checked for non-zero patterns.

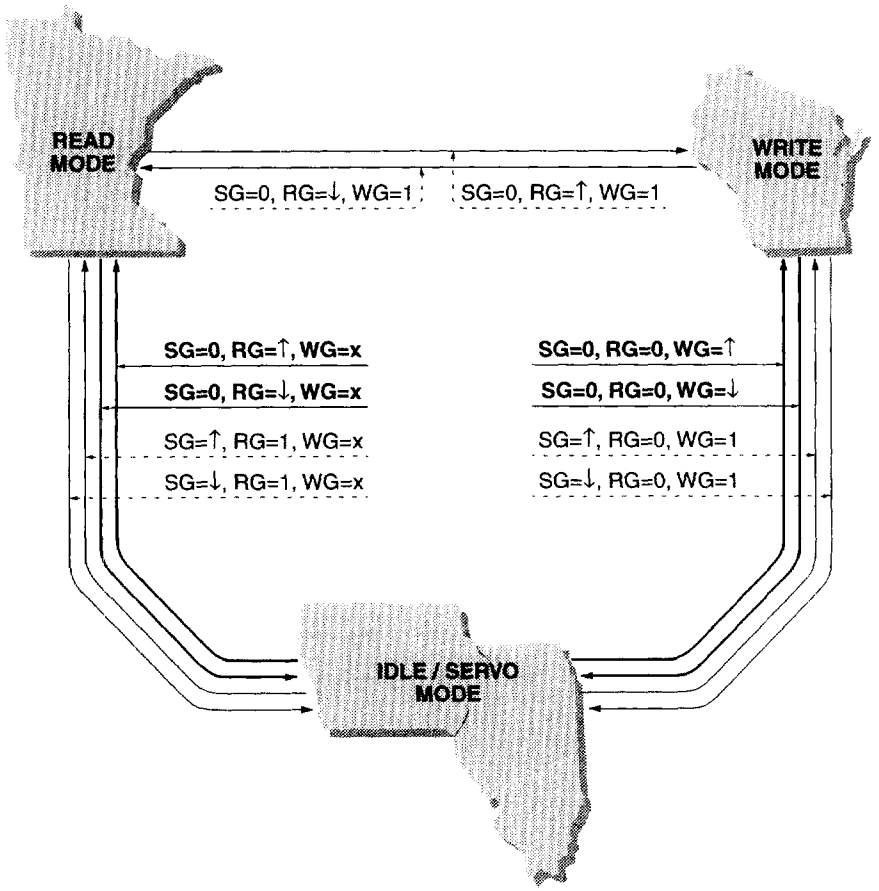


Diagram 10 State Diagram of Mode Transitions

MODE CONTROL AND POWER MANAGEMENT

The fundamental operating modes are controlled by the servo gate (SG), read gate (RG), and write gate (WG) input pins. The exclusive assertion of any of these inputs causes the circuit to enter that mode. If none of these inputs is asserted, the circuit is in IDLE mode. If more than one of the inputs is asserted, the mode is determined by the following hierarchy: SG overrides RG which overrides WG. The mode that is overriding takes effect immediately. SG and RG are asynchronous inputs and may be initiated or terminated at any time. WG is also an asynchronous input, but should not be terminated prior to the last output write data pulse to the preamp.

Table 7 Mode Control

WG	*RG*	*SG*	*PD*	*MODE*
X	X	X	1	Entire chip powered down; serial port still functional
0	0	0	0	IDLE mode; read data blocks powered down if PREN = '1'
X	X	1	0	SERVO mode; read data blocks powered down if PREN = '1'
X	1	0	0	READ mode; read data blocks powered on
1	0	0	0	WRITE mode; read data blocks powered down if PREN = '1'

DIGITAL CONTROL

Control of the chip is performed through a serial digital interface and a (16,12) bit wide register file. Control information is stored in the register file and used directly as digital control lines or sent to one of the DACs to create analog control signals.

The interface consists of three CMOS-level signals for input/output data, clock, and enable. Upon asserting SPEN, the serial port is enabled and ready for input on SPDATA and SPCLK. The SPDATA line provides the read/write, address and data information.

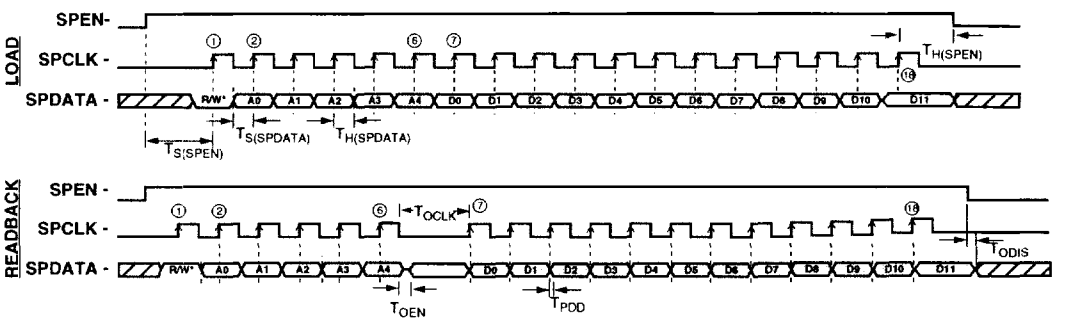


Diagram 11 Serial Register Load & Readback Timing

Table 8 Serial Register Bit Allocation

Register Address	Data Bit											
	11	10	9	8	7	6	5	4	3	2	1	0
0	PGC DAC				SQPI DAC		FIR Tap 0				rsrv'd	rsrv'd
1	DR DAC					TFAQ	FIR Tap 6				rsrv'd	rsrv'd
2	CTF Data Group Delay						FIR Tap 1					rsrv'd
3	CTF Servo Group Delay						FIR Tap 5					rsrv'd
4	WPC Pattern 2				PGCEN	DHBW	FIR Tap 2					
5	WPC Pattern 3				WPCHR	FAQSEN	FIR Tap 4					
6	WPC Pattern 1				TRBWR	TC24	TC3	FIR Tap 3				
7	FS Divide-by-N						SLEEP	PRST	TRCKS L	PED	PDTST	VITOWD
8	Servo Gain				FSCKS L	Viterbi Threshold DAC						
9	Level Qual Pos V_{TH}					Damping Ratio DAC						
10	Level Qual Neg V_{TH}					LPFBYP	WDSEL[1:0]		SRVDB	TRGAIN	REF-SEL	PREN
11	CTF Data Fc						CTF Data Boost					
12	CTF Servo Fc						CTF Servo Boost					
13	HLD	TSRV	CPTST	ACTST		SYMC	Zero Phase Restart DAC				PE Offset DAC	
14	CMXEN	TP1 Select			SELTE	DAGC	DPLL	BMXEN	Test Mux Select			
15	FS Divide-by-M								AGC SF Count		PLL SF Count	
16	rsrv'd	VTC2	SB9	SB8	SB7	SB6	SB5	SB4	SB3	SB2	SB1	rsrv'd
17	DTM	NONE	BOTH	BESEL	FESEL	rsrv'd	EXT	SBRT	EDGE	NOPR	NIB	rsrv'd
24	AE	DZ		INTL		ITW			NOSB	TWR		

*rsrv'd bits are VTC reserved control bits which should be programmed low

Table 9 Serial Register Bit Descriptions

Reg. Addr	Bit(s)	Description	Usage
0	1:0	rsrv'd	always program low
	5:2	FIR Tap 0 2's Complement	K_0=0.0194×VALUE in V/V -8 ≤ VALUE ≤ 7
	7:6	SQPI DAC: AGC Sampled Charge Pump Current DAC	I=20×VALUE in µA I=Charge Pump Current
	11:8	PGC DAC: Programmable Gain Control DAC	$A_V = [2(2.5 + VALUE)]$ 0 ≤ VALUE ≤ 15 A_V=VGA Gain

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Table 9 Serial Register Bit Descriptions

1	1:0	rsrv'd	always program low
	5:2	FIR Tap 6 2's Complement	$K_6 = 0.0194 \times$ VALUE in V/V $-8 \leq$ VALUE ≤ 7
	6	TFAQ: Test Fast Acquisition. Allows for testing of ultra fast decay current.	0: Normal Mode 1: Test Mode (Fast Acquisition. always on)
	11:7	DR DAC: Data Rate DAC	$\omega_C = \left(\frac{\pi \times 10^{10}}{RR}\right) \times (33 + \text{VALUE})$ in Mrad/s $0 \leq$ VALUE ≤ 31 ω_c = VCO center frequency RR = Value of external resistor in Ohms
2	0	rsrv'd	always program low
	5:1	FIR Tap 1 2's Complement	$K_1 = 0.0195 \times$ VALUE in V/V $-16 \leq$ VALUE ≤ 15
	11:6	CTF Data Group Delay 2's Complement	$GD_{DC} = 0.95 \times$ VALUE in % $-32 \leq$ VALUE ≤ 31
3	0	rsrv'd	always program low
	5:1	FIR Tap 5 2's Complement	$K_5 = 0.0195 \times$ VALUE in V/V $-16 \leq$ VALUE ≤ 15
	11:6	CTF Servo Group Delay 2's Complement	$GD_{DC} = 0.95 \times$ VALUE in % $-32 \leq$ VALUE ≤ 31
4	5:0	FIR Tap 2 2's Complement	$K_2 = (0.0195 \times \text{VALUE}) - 0.3125$ in V/V $-32 \leq$ VALUE ≤ 31
	6	DHBW: Disable High Bandwidth Mode of AGC. Forces FAQ to remain low.	0: Normal Mode 1: Disable high bandwidth
	7	PGCEN: Enable Programmable Gain Control Mode of VGA. Allows the VGA gain to be adjusted through PGC DAC.	0: Normal Mode (AGC loop active) 1: Programmable Gain Mode
	11:8	WPC Pattern 2: Determines amount of precomp for pattern 2	$Twpc = (0.013 \bullet \text{VALUE}) \bullet T$ $0 \leq$ VALUE ≤ 15 Twpc = time delay of pattern transition T = Period of Data Rate clock
5	5:0	FIR Tap 4 2's Complement	$K_4 = (0.0195 \times \text{VALUE}) - 0.3125$ in V/V $-32 \leq$ VALUE ≤ 31
	6	FAQSEN: Enable Fast Acquisition on falling edge of Servo Gate (SG).	0: Normal Mode 1: Enable fast Acquisition
	7	WPCHR: WPC High Range Bit; Selects patterns 1& 3's precomp range See WPC Pattern 1 & 3	0: 0 - 20% Precompensation 1: 20 - 40% Precompensation
	11:8	WPC Pattern 3: Determines amount of precomp for pattern 3	$Twpc = (0.013 \bullet \text{VALUE} + 0.20 \bullet \text{WPCHR}) \bullet T$ $0 \leq$ VALUE ≤ 15 Twpc = time delay of pattern transition T = Period of Data Rate Clock WPCHR = WPCHR Bit Setting

Table 9 Serial Register Bit Descriptions

6	4:0	FIR Tap 3	$K_3 = (0.0195 \times \text{VALUE}) + 1.094$ in V/V $0 \le \text{VALUE} \le 31$
	5	TC3: Tap Centering, 3rd Tap. Controls gain offset in FIR center tap (tap 3).	0: Normal Mode, $1 < \text{gain} < 1.7$ 1: Test Mode, $0 < \text{gain} < 0.7$
	6	TC24: Tap Centering, 2nd & 4th Taps. Controls the gain offset of FIR taps 2 & 4.	0: Normal Mode, $-.93 < \text{gain} < +.3$ 1: Test Mode, $-.62 < \text{gain} < +.62$
	7	TRBWR: Reduces the Pmultiplier gain by factor of 1/4 in tracking mode.	0: Selects Pmult gain, P 1: Selects Pmult gain, P/4
	11:8	WPC Pattern 1: Determines amount of precomp for Pattern 1	$Twpc = (0.013 \bullet \text{VALUE} + 0.20 \bullet \text{WPCHR}) \bullet T$ $0 \le \text{VALUE} \le 15$ Twpc = time delay of pattern transition T = Period of Data Rate Clock WPCHR = WPCHR Bit Setting
7	0	VITOWD: Viterbi OverWrite Disable. Allows the path memory over-write feature to be disabled in the Viterbi Detector	0: Normal Mode 1: Over-write disabled
	1	PDTST: Phase Detector Test. A high prevents the input to the decision-directed phase detector (and Viterbi detector) from switching from the low pass filter output to the FIR output.	0; Normal Mode 1: Test Mode
	2	PED: Timing Recovery Phase adjustment direction.	0: I_{offset} set by PE offset DAC added to DSFN 1: I_{offset} set by PE offset DAC added to DSFP
	3	TRCKSL: Timing Recovery Clock select, chooses between the TR VCO output being chosen or an alternative reference in its place	0: Timing Recovery VCO chosen (Normal) 1: Alternative reference chosen, specific reference determined by REFSEL bit
	4	PRST: Programmable reset for synth. dividers and divide-by-4's	0: Normal Mode 1: Reset Mode
	5	Sleep	0: Normal (Powered On) Mode 1: Power Off Mode
	11:6	FS Divide-by-N: Reference divider value in the Frequency Synthesizer	$f_{out} = f_{FREF}\left[\frac{(M+1)}{(N+1)}\right]$ in MHz f_{out} = the output frequency of VCO f_{FREF} = input frequency on FREF pin M = divide-by-M setting N = divide-by-N setting
8	6:0	Viterbi Threshold DAC. Nominal setting is VALUE = 45.	$VIT_{TH} = 0.047 + 0.376\left(\frac{\text{VALUE}}{127}\right)$ in Volts $0 \le \text{VALUE} \le 127$
	7	FSCKSL: Frequency Synthesizer clock select	0: VCO output selected (Normal Mode) 1: TCLKP/N input selected
	11:8	Servo Gain DAC: 4 bit DAC which controls the voltage gain of the servo block.	$V_{SB} = \left[\left(\frac{N \cdot V_{DIFF}}{3}\right) \cdot \left(0.6 + \frac{SDAC}{20}\right)\right] + 0.05$ V_{SB} = Integrated servo burst output in V. N = Number of integer servo burst cycles. V_{DIFF} = Continuous time filter differentiated output. (dppV). This signal can be measured on TP2 test point output. SDAC = Servo DAC setting (0 - 15). Nominal setting: 1000.

Table 9 Serial Register Bit Descriptions

9	6:0	Damping Ratio DAC	$P = K \bullet (\frac{127 - VALUE}{127})$ $\xi = \frac{P}{2}\sqrt{\frac{KVCO \cdot KDS \cdot C}{I \cdot G_m}}$ $0 \le VALUE \le 127$ K = Gain of Pmultiplier KVCO = Gain of TR VCO KDS = Gain of phase detector, either the PFD in W/I mode or DDPD in Read Mode C = Value of external capacitor I = Gain of Imultiplier G_m = Gain of QPUMP
	11:7	Level Qual Pos V_{TH}: PDQ Positive Threshold Qualification Level. Measured as a percentage of V_{LQ}	Vth = 20 + (1.9 × VALUE) in percent $0 \le VALUE \le 15$
10	0	PREN: WRITE/IDLE (W/I) mode power reduction enable	0: No power reduction in W/I mode 1: FIR/VIT/DDPD powered off during W/I
	1	REFSEL: Selects reference to use in place of Timing Recovery VCO output. Used in conjunction with TRCKSL Bit	0: Selects FDSP/N Input 1: Selects synth. output as reference
	2	TRGAIN: Selects Gain of QPUMP and Pmultiplier while in Tracking Mode compared to respective gains in Acquisition Mode	0: Attenuate QPUMP gain by 16, Pmult by 4 1: Attenuate QPUMP gain by 4, Pmult by 2
	3	SRVDB: Disables (powers down) Servo block and enables analog test mux	0: Servo block enabled 1: Servo block disabled
	5:4	WDSEL: Write Data Select, determines what signal will be output on the WDP/N lines	BIT (5:4) 0 0: Toggle Flip-Flop in data path 0 1: No Toggle Flip-Flop in data path 1 0: bypass precoder and write precomp 1 1: FDSP/N inputs outputted
	6	LPFBYP: Low Pass Filter Bypass. Allows differential signal to be injected immediately after the internal AC Coupling Caps. Test signal is input on RLOWZ and RFSR pins	0: Normal Mode 1: Test Mode (lowpass filter bypassed)
	11:7	Level Qual Neg V_{TH}: PDQ Negative Threshold Qualification Level. Measured as a percentage of V_{LQ}	V_{TH} = -20 + (1.9 × VALUE) in percent $0 \le VALUE \le 15$
11	4:0	CTF Data Boost	See Graph 2 on page 21
	11:5	CTF Data Fc: Cutoff frequency of LPF while in READ Mode	$f_C = (0.323 \times VALUE) + 7$ in MHz $0 \le VALUE \le 127$
12	4:0	CTF Servo Boost	See Graph 2 on page 21
	11:5	CTF Servo Fc: Cutoff frequency of LPF while in SERVO Mode	$f_C = (0.323 \times VALUE) + 7$ in MHz $0 \le VALUE \le 127$

Table 9 Serial Register Bit Descriptions

13	1:0	PE Offset DAC: Phase Error Offset DAC used to add current to DSFP or DSFN depending on the PED bit setting. Corrects for phase offset in the timing recovery loop.	0.....0 µA 1.....5 µA 2.....10 µA 3.....15 µA
	4:2	ZPR DAC: Zero Phase Restart DAC used to determine time before first sample is taken on the Sync Field 2T pattern	Nominal setting: 10001
	6:5	Symmetric Control: Determines which if any of the taps will be symmetrically adjusted. See "FIR Adaption Circuit" on page 24 for details.	SYMC.....Taps which will be identical --- 0.....(2 & 4) 1.....(2 & 4) & (1 & 5) 2.....(2 & 4) & (1 & 5) & (0 & 6) 3.....all taps asymmetric
	8:7	Adaption Control Test: Allows the adaption circuitry to be tested by forcing either an up, down or hold signal. See "FIR Adaption Circuit" on page 24 for details.	ACtest.....Resulting mode --- 0.....Normal operation 1.....Up forced 2.....Down forced 3.....Hold forced
	9	CPTST: Used to test timing recovery charge pump (QPUMP) gains in Idle mode.	0: Normal Mode 1: Test Mode
	10	TSRV: Test Servo operating mode	0: Normal Mode (synchronous) 1: Test Mode (asynchronous)
	11	HLD: Hold mode for AGC and timing recovery loops.	0: Normal operation. 1: Both AGC and timing recovery loops forced into a hold (coast) mode. Intended for coasting over thermal asperities.

Table 9 Serial Register Bit Descriptions

14	3:0	Test Mux Select: Selects which internal signal will be outputted on the various output pins	See Table 11
	4	BMXEN: Enables the Bipolar test point muxes	0: Bipolar Test Muxes disabled (Normal Mode) 1: Bipolar Test Muxes enabled
	5	DPLL Allows the internal PLL signal to be programmably enabled/disabled for test purposes. PLL is asserted at the transition from acquisition mode to tracking mode	0: Normal Mode, (PLL SF count enabled) 1: Test Mode, (PLL SF count disabled)
	6	DAGC: Allows the internal AGC signal to be programmably enabled/disabled for test purposes. AGC is asserted once the AGC count is reached in the Sync Field	0: Normal Mode, (AGC SF count enabled) 1: Test Mode, (AGC SF count disabled)
	7	SELTE: Selects which Timing Error the QPUMP will receive from the DDPD	0: Resampled Timing Error (Normal Mode) 1: Non-resampled Timing Error
	10:8	TP1 Select: Selects which internal signal to mux out to the TP1 test point.	See Table 10
	11	CMXEN: CMOS Test muxes enable	0: CMOS test mode disabled (Normal Mode) 1: CMOS test mode enabled

Table 9 Serial Register Bit Descriptions

15	1:0	PLL SF Count: Determines how many user data bytes of data rate clock pass, after AGC has timed out, before PLL signal, tracking mode, begins	Byte Clocks / Bit 1 0 0 0 0 1 0 1 2 1 0 3 1 1
	3:2	AGC SF Count: Determines how many user data bytes of data rate clock pass, after RGD has occurred, before AGC signal begins RGD occurs 2 user data bytes clocks following external RG being asserted	Byte Clocks / Bit 1 0 4 0 0 5 0 1 7 1 0 9 1 1
	11:4	FS Divide-by-M: VCO feedback divider value in the Frequency Synthesizer	$f_{out} = f_{FREF}\left[\frac{(M+1)}{(N+1)}\right]$ in MHz f_{out} = the output frequency of VCO f_{FREF} = input frequency on FREF pin M = divide-by-M setting N = divide-by-N setting
16	0	rsrv'd	always program low
	9:1	Sync Byte 2 Pattern	This nine bit pattern and its complement define the two sync bytes.
	10	VTC2: Test mode to initialize clockmaker. Must be low for normal operation of VM65060.	0: Normal Mode 1: Clockmaker held at reset state
	11	rsrv'd	always program low
17	0	rsrv'd	always program low
	1	NIB: Control bit to determine NRZ interface mode	0: 8-bit wide (byte) mode 1: 4-bit wide (nibble) mode
	2	NOPR: Control bit which allows the pseudo random number generator to be disabled, thus the scrambler/descrambler also controlled	0: Normal Mode 1: Pseudo Random Number Generator (Scrambler/Descrambler) disabled
	3	EDGE: Determines which edge of RCLK the NRZ lines will be strobed in on	0: Positive edge of RCLK 1: Negative edge of RCLK
	4	SBRT: Determines if Sync Byte 2 will be returned prior to user data	0: No sync byte returned 1: Sync Byte 2 returned
	5	EXT: Select clock to strobe NRZ input data in	0: internal RCLK 1: External WCLK rising edge
	6	rsrv'd	always program low
	7	FESEL: *Front End Select. Allows signals inputted* on TDATA/TCLK to be sent to the endec processor (digital backend)	0: Normal Mode 1: TDATA/TCLK sent to endec processor
	8	BESEL: Backend Select. Allows signals inputted on TDATA/TCLK to be sent to Precoder/WPC	0: Normal Mode 1: TDATA/TCLK sent to Precoder/WPC
	9	BOTH: Determines if both sync bytes need to be found or either	0: Either Sync Bytes may be found 1: Both Sync Bytes must be found
	10	NONE: Control bit which allows readback framing to be initialized with RG rather then Sync Byte Detect	0: Normal Mode 1: RG initializes readback framing
	11	*DTM: Direct Test Mode which allows NRZ data to* be directly passed through the backend, i.e. no scrambling/descrambling or encoding/decoding	0: Normal Mode 1: Direct Test Mode enabled

Table 9 Serial Register Bit Descriptions

24	2:0	Tap Weight Rollover value: Determines which of the FIR taps will be adapted by determining which tap gets adapted following Tap 4. See "FIR Adaption Circuit" on page 24 for details.	TWR .....Tap to 'roll-back' to --- 0.....Tap 0 1.....Tap 6 2.....Tap 1 3.....Tap 5 4.....Tap 2 5.....Tap 4
	3	NO Sync Byte: Allows the FIR adaption routine to begin without requiring a Sync Byte Found to occur. Adaption will begin after PLL SF Count has been reached with this bit set.	0: Normal mode, Sync Byte starts adaption 1: PLL SF Count starts adaption
	6:4	Initial Tap Weight: Determines which tap the adaption routine will adapt first. See "FIR Adaption Circuit" on page 24 for more details.	ITW.....Tap to adjust first --- 0.....Tap 0 1.....Tap 6 2.....Tap 1 3.....Tap 5 4.....Tap 2 5.....Tap 4
	8:7	Integration Length: Determines the number of cycles the adaption circuit will integrate over when deciding weather the current tap weight should be incremented, decremented or held. See "FIR Adaption Circuit" on page 24 for more details.	INTL.....Integration Length --- 0.....12 cycles 1.....15 cycles 2.....18 cycles 3.....21 cycles
	10:9	Dead Zone: Determines the required differential number of updates (delta) in either direction to qualify an increment or decrement decision. If this delta is not reached then the current tap weight is simply held. See "FIR Adaption Circuit" on page 24 for more details.	DZ.....Differential number of updates --- 0.....delta = 2 1.....delta = 4 2.....delta = 6 3.....delta = 8
	11	Adaption Enable: Enables the adaption circuitry	0: Adaption circuit NOT active 1: Adaption circuit enabled

TEST MODES

There are sixteen test modes that are used in the VM65060. The test modes are controlled by two different sets of test addresses (TSEL[3:0] & TP1[2:0]) in the serial register, the bipolar test enable (BMXEN) and the CMOS test enable (CMXEN), as shown in Table 11 and Table 12.

Table 10 TP1 Control

BMXEN	TP1 SEL[2:0] bits			Output pins
	2	1	0	TP1 (diff analog)
1	0	0	0	TR VCO/4
1	0	0	1	Timing Error
1	0	1	0	Y_n
1	0	1	1	Vit Sig E
1	1	0	0	Held Sig Odd
1	1	0	1	FIR out
1	1	1	0	TR VCO Control
1	1	1	1	CTF norm ac
0	X	X	X	normal op.

Table 11 Bipolar Test Register Decode

BMXEN	TSEL[3:0] bits				mode	Output pins		
	3	2	1	0		TP2 (diff analog)	TP3 (PECL)	TP4 (PECL)
1	0	0	0	0	0	CTF norm	DV64	DV256
1	0	0	0	1	1	VGA in	FSUP	FSDN
1	0	0	1	0	2	VGA out	FS VCO	TR VCO
1	0	0	1	1	3	Vit Sig O	MX	T0
1	0	1	0	0	4	Held Sig Evn	YHB/YLB	XPB/XNB
1	0	1	0	1	5	CTF diff	TRUP	TRDN
1	0	1	1	0	6	Int_$\mathcal{E}$	$\mathcal{E}_n$	C_n
1	0	1	1	1	7	Y_{n-1}	X_1	X_{N1}
1	1	0	0	0	8	none	FEDATA	FECLK
1	1	1	1	1	15	none	BEDATA	BECLK
0	X	X	X	X	X	power down	power down	power down

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Table 12 CMOS Test Register Decode

CMXEN	TSEL[2:0] bits			mode	Output pins	
	2	1	0		RDS (CMOS)	RPOL (CMOS)
1	0	0	0	0	LP	HCLK
1	0	0	1	1	LZDEL	FRDEL
1	0	1	0	2	HLDEL	RGDP
1	0	1	1	3	dv/dt comp	
1	1	0	0	4	AGCN	PLLN
1	1	0	1	5	SHGN	PDSELN
1	1	1	0	6	DMN	SRVCNT
1	1	1	1	7	NZD	PRN10
0	X	X	X	X	normal op.	normal op.

Table 13 Test Signal Descriptions

Test Signal Name	Description
TR VCO/4	Timing recovery VCO clock divided by 4
Timing Error	Timing error for the Timing Recovery Loop.
Yn	Resampled FIR output at the "current" time
Vit Sig E	The even FIR interleave being input to the Viterbi detector.
Held Sig Odd	Held signal value for the odd interleave of Viterbi detector.
FIR out	Output of the Finite Impulse Response filter.
TR VCO Control	Analog control input to the Timing Recovery VCO.
CTF diff	Differentiated output of the Continuous Time Filter.
Held Sig Evn	Held signal value for the even interleave of Viterbi Detector.
DV64	Output of the 6-bit divide-by-N counter in the frequency synthesizer.
DV256	Output of the 8-bit divide-by-M counter in the frequency synthesizer.
VGA in	Analog input to the Variable Gain Amplifier of the AGC loop.
FSUP	Pump up signal from the phase-frequency detector in the frequency synthesizer.
FSDN	Pump down signal from the phase-frequency detector in the frequency synthesizer.
VGA out	Analog output of the Variable Gain Amplifier of the AGC loop.
FS VCO	Frequency synthesizer VCO output.
TR VCO	Timing recovery VCO output.
Vit Sig O	The odd FIR interleave being input to the Viterbi detector.

Table 13 Test Signal Descriptions

Test Signal Name	*Description*
MX	FIR mux0 to mux1 transition.
T0	FIR track and hold 0 control signal.
CTF norm	Normal output of the Continuous Time Filter
YHB/YLB	Timing recovery pump up (=0) / down (=1) in sampled mode, qualified by XPB/XNB signal = 1.
XPB/XNB	Timing recovery positive/negative sample sign indicator. Equivalent to (X1 xor X2).
CTF norm ac	AC coupled normal output of the Continuous Time Filter
TRUP	Pump up signal into the charge pump of the Timing recovery loop.
TRDN	Pump down signal into the charge pump of the Timing recovery loop.
Int_$\mathcal{E}$	Integrated lms tap weight error
$\mathcal{E}_n$	Sign of the PR4 equalization error estimate
C_n	Sign of the Channel data
Yn-1	Resampled FIR output at the sampled one clock cycle before the "current" time
X1	Positive sample sign indicator for decision directed phase detector in the timing recovery.
XN1	Negative sample sign indicator for decision directed phase detector in the timing recovery.
LP	Signal from the level qualifier block indicating when the input pulse exceeds the programmed threshold.
HCLK	Signal from the level qualifier block which outputs a pulse for each input peak.
LZDEL	One-shot pulse which controls how long the AGC loop stays in low impedance mode. The RLOWZ external resistor controls the one-shot pulse width.
HLDEL	Hold control signal for the AGC loop. Active only in servo mode.
FRDEL	One-shot pulse which controls how long the AGC loop stays in fast acquisition mode. The RFSR external resistor controls the one-shot pulse width.
RGDP	Read gate delayed. Internal control signal which is delayed from RG by two bytes.
dv/dt comp	The CTF differentiated output after passing it through a comparator. Used by the servo block.
AGCN	Internal control signal indicating when the AGC loop switches from continuous time loop to samples time loop.
PLLN	Internal control signal indicating when the timing recovery loop switches from decision directed acquisition mode to decision directed tracking mode.
PDSELN	Phase detector select signal. Lo selects the decision directed phase detector, hi selects the phase frequency detector.
DMN	Servo control signal that when hi indicates one of the servo channels is integrating.
NZD	Non Zero Detect; test signal from digital backend.
SRVCNT	One bit from the servo 2-bit counter which controls servo channel selection sequence.
PRN10	Pseudo Random Number 10; PRNG output from digital backend.
BEDATA	Test signal: Digital Back End Data
BECLK	Test signal: Digital Back End Clock
FEDATA	Test signal: Analog Front End Data
FECLK	Test signal: Analog Front End Clock

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ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage

VCC . . . . . -0.3V to +7V

Input Voltages

Digital Input Voltage V_{IN} . . . . . -0.3V to VCC+0.3V

Analog Input Voltage V_{IN} . . . . . -0.3V to VCC+0.3V

Storage Temperature T_{stg} . . . . . -65°C to 150°C

Junction Temperature T_J . . . . . 150°C

Thermal Impedance, Θ_{JA} 80-Lead PQFP . . . . . 39°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage

VCC . . . . . +5V ± 10%

Junction Temperature T_J . . . . . 0°C to 125°C

PIN FUNCTION LIST AND DESCRIPTION

There are a number of different input and output buffers used on this chip. There are CMOS TTL inputs, Bipolar ECL-like differential outputs, Analog differential inputs, and several analog reference input and output pins. Because of pin limitations some pins serve double duty. A table showing the various pin types is provided in Table 14 below.

Table 14 VM65060 Pin Descriptions

PIN TYPE	*PIN NAME*	*#*	*INFORMATION*
Power Supplies	VCC1	27	LPF, servo, analog AGC, analog pulse qualification, analog test mux power
	VCC2	6	FIR, Viterbi detector, digital test muxes power
	VCC3	38	Frequency synthesizer analog power
	VCC4	58	Timing recovery analog power
	VCC5	45	Frequency synthesizer digital, timing recovery digital, write precomp and PECL output power
	VCC6	19	Front end digital CMOS power and N well.
	VCC7		Not Used (not a pin)
	VCC8	72	Digital backend CMOS power
	VCC9	65	Digital backend bipolar read power
	VCC10	70	Digital backend CMOS N well connection
	VCC11	3	Digital backend bipolar write power

Table 14 VM65060 Pin Descriptions

PIN TYPE	*PIN NAME*	*#*	*INFORMATION*
Ground Supplies	VEE1	28	LPF, servo, analog AGC, analog pulse qualification, analog test mux ground
	VEE2	5	FIR, Viterbi detector, digital test muxes ground
	VEE3	39	Frequency synthesizer analog ground
	VEE4	57	Timing recovery analog ground
	VEE5	44	Frequency synthesizer digital, timing recovery digital and write precomp ground
	VEE6	18	Front end digital CMOS ground
	VEE7	63	Bipolar substrate connection
	VEE8	71	Digital backend CMOS ground
	VEE9	64	Digital backend bipolar read ground
	VEE10	69	Digital backend CMOS substrate
	VEE11	2	Digital backend bipolar write ground
CMOS Inputs	ICM	1	Initialize ClockMaker, VTC test control. MUST BE LOW FOR NORMAL OPERATION.
	HOLD	4	External hold control which overrides the internally generated hold signal (Active Low)
	RG	7	Read Gate. When this signal is asserted, the read path circuitry is enabled (active high).
	WG	8	Write Gate. When this signal is asserted, the write path circuitry is enabled (active high).
	SG	9	Servo Gate. When this signal is asserted, the servo demodulator circuitry is enabled (active high).
	SRST	10	Servo Reset (active high)
	DEMOD	11	Enables selected area detector
	SPEN	14	Serial port I/O enable (active high)
	SPCLK	13	Serial port clock (latch on positive edge)
	PD	12	Power down control signal. When this signal is asserted, the chip is powered down (active high).
	WCLK	67	NRZ Write Clock; if used, must be synchronous with RCLK
Bipolar TTL Input	FREF	46	Reference frequency for the frequency synthesizer
CMOS Bidirectional	SPDATA	15	Bidirectional serial port data signal
	NRZ8-NRZ1	73-80	NRZ Parallel Read/Write Data
CMOS Outputs	RDS	17	Level qualifier data output. A high indicates a servo peak of qualified amplitude.
	RPOL	16	Level qualifier polarity output. A high indicates positive servo polarity. A low indicates negative servo polarity.
	SBF	66	Sync Byte Found Flag (Active Low)
	RCLK	68	User Data Read Clock

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Table 14 VM65060 Pin Descriptions

PIN TYPE	PIN NAME	#	INFORMATION
Bipolar ECL-like Differential inputs (PECL)	FDSP FDSN	53 54	Reference frequency used to replace the timing recovery VCO output.
	TDATAP TDATAN	61 62	Test-mode Data inputs
	TCLKP TCLKN	59 60	Test-mode Clock inputs
Bipolar ECL-like Differential Outputs (PECL)	WDP WDN	49 50	Write data to the preamplifier.
	TP3P TP3N	47 48	Test point 3 output
	TP4P TP4N	51 52	Test point 4 output
Analog Inputs	DIP DIN	25 26	Differential Analog Read Data input from the preamplifier chip.
Analog Outputs	SREF	33	Servo Reference Voltage (0.6V)
	SBA	29	Servo burst A integrator output
	SBB	30	Servo burst B integrator output
	SBC	31	Servo burst C integrator output
	SBD	32	Servo burst D integrator output
	TP1P TP1N	34 35	Differential Analog test point 1 output
	TP2P TP2N	36 37	Differential Analog test point 2 output
External Component Connections	RX	22	Filter reference resistor. An external 1% resistor is connected from this pin to analog ground to establish a precise internal reference current for the DACs controlling the continuous-time filter cut-off frequency. Resistor (4KΩ to 32KΩ) to ground [see Eq. 1]
	RR	40	PLL reference resistor. An external 1% resistor is connected from this pin to analog ground to establish a precise internal reference current for the DACs controlling the timing recovery and synthesizer VCO center frequencies. Resistor (2KΩ to 6KΩ) to ground [see Eq. 8]
	RLOWZ	24	Low Z duration control. A resistor between this pin and ground defines the duration of the Low Z period.
	RFSR	23	Fast recovery/decay duration control. A resistor between this pin and ground defines the duration of the fast gain acquisition period.
	CAGCD	20	AGC data field gain storage, capacitor (390pF) to ground
	CAGCS	21	AGC servo field gain storage, capacitor (390pF) to ground
	DSFP DSFN	55 56	Timing Recovery PLL loop filter. Differential connections for the timing recovery PLL loop filter component. Capacitor (150pF) between pins.
	FSFP FSFN	41 42	Frequency Synthesizer PLL loop filter. Differential connections for the frequency synthesizer PLL loop filter components.
No Connect	nc	43	This pin may be connected to ground, if desired.

ELECTRICAL PARAMETERS, BY FUNCTIONAL SECTION

AC and DC CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified. 0°C < T_A < 70°C, 4.5V < VCC < 5.5V

OVERALL

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode, Data Rate = 55 Mbps		TBD	TBD	mA
		Read Mode, Data Rate = 140 Mbps		TBD	TBD	mA
		Standby Mode			TBD	mA
Recovery Time Standby to Fully Functional	T_{REC}	AGC within 10% final value, Pulse Detector w/o pulse pairing, Filter cutoff within 10% final value			10	µs

LOGICAL SIGNALS; ALL DIGITAL PINS

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Input High Voltage	V_{IH}		2.0		VCC + 0.3	V
Input Low Voltage	V_{IL}		–0.3		0.8	V
Input Leakage Current	I_{IL}	V_{IL} = 0.8V			±10	µA
	I_{IH}	V_{IH} = 2.0V			±10	µA
Control Signal Rise and Fall Times	T_{CS}				100	ns
Input Capacitance	C_{IN}				10	pF

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GAIN CONTROL

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Input Dynamic Range	V_{DI}	$V_{DI} = (V_{DIP} - V_{DIN})$	20		200	mV_{ppd}
Input Common Mode Voltage	V_{CMDI}	$V_{CMDI} = (V_{DIP} + V_{DIN})/2$	VCC–3.1	VCC-2.7	VCC–2.3	V
Differential Input Resistance	$R_{in(DA)}$	LOWZ = Low	1.2	2.5	3.8	kΩ
		LOWZ = High, WG=4.0V	120	250	380	Ω
Single Ended Input Resistance	$R_{in(SA)}$	LOWZ = Low	.6	1.25	1.9	kΩ
		LOWZ = High, WG=4.0V	60	125	190	Ω
VGA Minimum Gain PGCEN Reg bit=0	AV_{min}	$AV=(V_{TP2P} - V_{TP2N})/V_{DI}$ V_{CAGCD}=0.8V, Test Mode 2,			4.0	V/V
VGA Maximum Gain PGCEN Reg bit=0	AV_{max}	$AV=(V_{TP2P} - V_{TP2N})/V_{DI}$ V_{CAGCD}=3.2V, Test Mode 2,	39	47		V/V
VGA Maximum Gain PGCEN Reg bit=1	AV_{max}	$AV=(V_{TP2P} - V_{TP2N})/V_{DI}$, TM2 DAC= 0000 DAC= 0001 DAC= 0011 DAC= 0111 DAC= 1111		5 12 18 28 46		V/V
Output Common Mode Voltage	V_{CM}	$V_{CM} = (V_{TP2P} + V_{TP2N})/2$ Test Mode 2	VCC–3.2	VCC-2.5	VCC–1.8	V
Output Offset Voltage	V_{OS}	$V_{OS}=(V_{TP2P} - V_{TP2N})$, over entire gain range, Test Mode 2	–50		50	mV
Output Distortion	THD	V_{DI} = 200mV_{ppd}, $V_{TP2} \leq 0.75V_{ppd}$, Test Mode 2, 1st, 2nd, and 3rd harmonics only			1.0	%

AGC / CHARGE PUMP (unless otherwise specified, RG = 0)

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
RX pin voltage	V_{RX}	R_{ext} = 6kΩ	1.05	1.2	1.35	V
Normal Charging Current, Continuous Mode, LPFBPY=1	I_{QNC}	$V_{IN}=V_D+V_{CM}$, V_{CM}=VCC-.5V $V_D=(V_{RLOWZ}-V_{RFSR})$ = 0.2V SG=0, DRR=11111 SG=0, DRR=00000 SG=1, DRR=XXXXX	 16 8 8	 20 10 10	 24 12 12	 µA µA µA
Normal Discharging Current, Continuous Mode	I_{QND}	$V_D=(V_{RLOWZ}-V_{RFSR})$ = 0.275V SG=0, DRR=11111 SG=0, DRR=00000 SG=1, DRR=XXXXX	 288 144 144	 360 180 180	 432 216 216	 µA µA µA
Fast Discharging Current, Continuous Mode	I_{QFD}	$V_D=(V_{RLOWZ}-V_{RFSR})$ = 0.375V SG=0, DRR=11111 SG=0, DRR=00000 SG=1, DRR=XXXXX	 2.01 1.00 1.00	 2.52 1.26 1.26	 3.02 1.51 1.51	 mA mA mA
Ultra Fast Charging Current, Continuous Mode	I_{QUFC}	$V_D=(V_{RLOWZ}-V_{RFSR})$ = 0.375V SG=0, DRR=11111 SG=0, DRR=00000 SG=1, DRR=XXXXX	 -2.01 -1.00 -1.00	 -2.52 -1.26 -1.26	 -2.52 -1.26 -1.26	 mA mA mA
Charge Pump Currents, Sampled Mode I_{QCD} =0, 20,40,60µA	I_{QCD}	$V_{DI} \leq 0.2V$ (static) SG=0, DRR=11111 SG=0, DRR=00000	 .8·I_{QCD} .4·I_{QCD}	 I_{QCD} .5·I_{QCD}	 1.2·I_{QCD} .6·I_{QCD}	 µA µA
Charge Pump Leakage Current	I_{LK}	HOLD = Active, Test Mode	-10		10	nA
Output Dynamic Range	V_{FA}	$V_{FA}=(V_{FAP}-V_{FAN})$ $20mV_{ppd} \leq V_{DI} \leq 200mV_{ppd}$ 5MHz < f_{in} < 40MHz	0.45		.55	V_{ppd}
Gain Settle from -30% V_{DI} Step	T_{GD}	$V_{FN} \geq 0.9$·(final value)		20	25	µs
Gain Settle from +30% V_{DI} Step	T_{GA}	$V_{FN} \leq 1.1$·(final value)			1.5	µs
LOWZ One-shot Pulse Width	PW_{LZ}	LOWZ = Active, Test Mode R_{LOWZ}=4.3kΩ	.28	.35	.42	µs
FSREC One-shot Pulse Width	PW_{LZ}	LOWZ = Active, Test Mode R_{FSR}=20.0kΩ	1.2	1.5	1.8	µs
Differential Input Capacitance	$C_{in(DA)}$				10	pF
Input Referred Noise Voltage	V_{IRN}	gain =AV_{max}, BW = 15MHz V_{DIP} = V_{DIN}			10	nV/√Hz
Bandwidth	BW	No AGC action. All gain values.	100			MHz
Common Mode Rejection Ratio	CMRR G	gain = AV_{max}, f_{in} = 5MHz, V_{DIP} = V_{DIN} = 100mV_{pp}	40			dB
Power Supply Rejection Ratio	PSRR G	gain = AV_{max}, f_{in} = 5MHz ΔVCC or ΔVEE =100mV_{pp}	45			dB
AGC Gain Sensitivity to CAGCx Voltage	AV_{PV}	(Typical range is 1.4V to 2.8V)		17.5		dB/V

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LOW PASS FILTER (7-POLE, 0.05°, EQUIRIPPLE PHASE)

(Signals measured at TP2 unless otherwise specified)

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Filter Cutoff Frequency (low end)	f_{Cmin}	Fc_{DAC}=00h, REXT=6kΩ	4.9	7	9.1	MHz
Filter Cutoff Frequency (middle)	f_{Cmid}	Fc_{DAC}=40h, REXT=6kΩ	25.9	27.5	29.1	MHz
Filter Cutoff Frequency (high end)	f_{Cmax}	Fc_{DAC}=7Fh, REXT=6kΩ	45.6	48	50.4	MHz
Normal Lowpass Gain (V_{FN} vs. V_{FI})	AO_N	$BOOST_{DAC}$=00h, Fc_{DAC}=00h, REXT=6kΩ, f_{in} = 4MHz	-4.2	-3.2	-2.2	dB
Differentiated Lowpass Gain (V_{FD} vs. V_{FN})	AO_D	$BOOST_{DAC}$=00h, $f_{in} = 0.67f_C$	AO_N–5.0	AO_N–3.5	AO_N-2.3	dB
Boost Accuracy	BA		-1		+1	dB
Filter Boost (low end)	AB_{min}	$BOOST_{DAC}$=00h, REXT=6kΩ		0	0.5	dB
Filter Boost (high end)	AB_{max}	$BOOST_{DAC}$=1Fh, REXT=6kΩ	12.0	13.0	14.0	dB
Normal Filter Output Offset	V_{OSFN}	V_{FI} = 0.0V	–200		200	mV
Differentiated Filter Output Offset	V_{OSFD}	V_{FI} = 0.0V, FDP/N outputs	–10		10	mV
AC Coupled Filter Output Offset	V_{OSFA}	V_{FI} = 0.0V, FAP/N outputs	–10		10	mV
Total Harmonic Distortion (V_{FN} or V_{FD} vs. V_{FI})	THD_F	$f_{in} = 0.67f_C$, Fc_{DAC}=7Fh, REXT=6kΩ, $V_{FI} \leq 0.7V_{ppd}$, 2nd, and 3rd harmonics only			1.5	%
Group Delay	T_{GD}	Fc_{DAC}=7Fh, REXT=6kΩ	10	12	14	ns
Group Delay Variation (normal or differential), GD=00h (i.e. symmetric zeros). Measured at Normal Outputs.	T_{GD1}	$0.1f_C \leq f_{in} \leq 1.5f_C$, 7 MHz $\leq f_C \leq$ 48 MHz, $BOOST_{DAC}$=00h, REXT=6kΩ	–2.0		2.0	%
	T_{GD2}	$0.1f_C \leq f_{in} \leq 1.5f_C$, 7 MHz $\leq f_C \leq$ 48 MHz, $BOOST_{DAC}$=1Fh, REXT=6kΩ	–2.5		2.5	%
Group Delay Variation Nonsymmetric Zeros	T_{GD3}	DC @ FNP/N outputs. GD_{DAC}=-32, relative to GD_{DAC}=0	–32		-28	%
	T_{GD4}	DC @ FNP/N outputs. GD_{DAC}=+31, relative to GD_{DAC}=0	28		30	%
Normal Output Noise Voltage	V_{NN}	BW = 100MHz, f_C = 30MHz [1] $V_{DIP} = V_{DIN}$, Test Mode 4			TBD	mV_{rms}
Differentiated Output Noise Voltage	V_{ND}	BW = 100MHz, f_C = 30MHz [1] $V_{DIP} = V_{DIN}$, Test Mode 4			9.0	mV_{rms}
Common Mode Rejection Ratio	$CMRR_F$	f_{in} = 5MHz, Fc_{DAC}=7Fh, REXT=6kΩ$V_{DIP} = V_{DIN}$ = 100mV_{pp}	40			dB

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	$PSRR_F$	f_{in} = 5MHz, V_{DI} = 0V, ΔVCC or ΔVEE = 100mV_{pp}	40			dB
Filter Settle From Step in Fc and BOOST	T_{FS}	Fc_{DAC} or $BOOST_{DAC}$ step to V_{FN} settle		85	300	ns

[1] Fc_{DAC}=7Fh, $BOOST_{DAC}$=1Fh (boost level is 13dB).

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FINITE IMPULSE RESPONSE FILTER

PARAMETER	SYM	CONDITIONS[1]	MIN	TYP	MAX	UNITS
Nom. Center Tap Gain	AV_c	Set bit three in K3 & bits 4 in K2/K4	1.0XX	1.2XX	1.2XX	V/V
Nom. Center Tap off	OFF_c	Set bit three in K3 & bits 4 in K2/K4		5		5mV
Feed Through	FTH	Set all taps to 0, clear TC3 & TC24 feed in a.5vp-p low freq. square wave		TBD		Vp-p diff
Output Toggle Test	OTT	Same as AV_c with.5vp-p $F_S/2$ square wave [2]		TBD		Vp-p diff
Center Tap Large Signal BW	LSBW	Same as AV_c,with the input being a swept AC signal 0.5vp-p diff.[2]		TBD		MHz
Center Tap Small Signal BW	SSBW	Same as AV_c,with the input being a swept AC signal 0.05vp-p diff.[2]		TBD		MHz
Center Tap K3 Gain & Linearity	OFF_3	Gain with the input code at zero		1.0xx		V/V
	AV_3	K_3=11111 bin		1.8xx		V/V
	DNL_3	Differential non-linearity		5		mV/V
	INL_3	Integral non-linearity		19.8		mV/V
Tap K2 & K4 Gain & Linearity	OFF_{24}	Gain with the input code at zero		-.3xx		V/V
	AV_{24}	Gain relative to $AV_3$with the center tap gain set to 0 & K_x=100000 bin		-0.9xx		V/V
	DNL_{24}	Differential non-linearity		5		mV/V
	INL_{24}	Integral non-linearity		19.8		mV/V
Tap K1 & K5 Gain & Linearity	OFF_{15}	Gain with the input code at zero		0		V/V
	AV_{15}	Gain relative to $AV_3$with the center tap gain set to 0 & K_x=10000 bin		-0.3xx		V/V
	DNL_{15}	Differential non-linearity		5		mV/V
	INL_{15}	Integral non-linearity		19.8		mV/V
Tap K0 &K6 Gain & Linearity	OFF_{06}	Gain with the input code at zero		0		V/V
	AV_{06}	Gain relative to $AV_3$with the center tap gain set to 0 & K_x=1000 bin		-0.15x		V/V
	DNL_{06}	Differential non-linearity		5		mV/V
	INL_{06}	Integral non-linearity		19.8		mV/V

[1]The part must be placed in test mode and the ac bypass will be used as an input and the FIR out test points used as outputs. The sample clock is taken from the external clock input and the frequency can be set for convenience.
[2]These test should be done at the highest device clock rate.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
DC Offset Variation	OV	DC in =0 v [1]			TBD	mV
Gain Variation	GV	DC in +-0.25 Vdiff [1]			TBD	%

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Acquisition Alignment	AA	Min. to Max. sample delay variation[1]			TBD	ns
TH Droop	DAV	Average droop 0.25 v diff [1]			30	V/µs
	DD	Delta droop max to min [1]			15	V/ns
Center Tap Distortion	$MX2^{nd}$	Set the input to 0.5vp-pdiff @ 31/ 128*F_S with F_S set to max data rate CT only [1]			-35	dBc
	$MX3^{rd}$				-35	dBc
	MXTHD				-30	dBc
Max EQ Distortion	$MX2^{nd}$	Same as center tap distribution. with amplitude set to 0.17vp-pdiff. Max peaking [2]			-35	dBc
	$MX3^{rd}$				-35	dBc
	MXTHD				-30	dBc
Noise	η_{CT}	CT only [1]				Vrmsd/ $\sqrt{Hz}$
	η_{MX}	Max peaking [2]				Vrmsd/ $\sqrt{Hz}$
2T Boost at $F_S/4$ [3]	MXB_{2T}	K2 & K4 set to 32, Vin =0.1 Vp-p diff, K3=8			1.91	V/V
	MNB_{2T}	K2 & K4 set to 31, vin =0.1 Vp-p diff, K3=8	-.6			V/V
2T Boost at $F_S/4$ [1,3]	MXB_{2T}	K1 & K5 set to 16			0.64	V/V
	MNB_{2T}	K1 & K5 set to 15	-.6			V/V
6T Boost at $F_S/4$ [1,3]	MXB_{6T}	K0 & K6 set to 8			0.32	V/V
	MNB_{6T}	K0 & K6 set to 7	-0.28			V/V

[1] Set taps K3=8 & K2/K4 = 16 and clear all others
[2] Set taps K3=31, K2/4=32, K1/5=16, & K0/6=8
[3] Relative to the nominal center tap gain

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VITERBI DETECTOR

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
All Zeros Bit Error Rate		Read Mode, data being output, sine wave input into DIN/DIP, VGA gain fixed, corrected gain from sine wave source to Viterbi input = 1. Sine wave frequency = data rate/4 Sine wave amplitude = VIT_{TH}/0.778 See Eq. 6 for VIT_{TH} formula.	TBD (0.999)			
All Ones Bit Error Rate		Read Mode, data being output, sine wave input into DIN/DIP, VGA gain fixed, corrected gain from sine wave source to Viterbi input = 1. Sine wave frequency = data rate/4 Sine wave amplitude = VIT_{TH}/0.636 See Eq. 6 for VIT_{TH} formula.	TBD (0.999)			
Additional Amplitude of Consecutive +1 (-1) Required to Overwrite Previous +1 (-1).		Read Mode, data being output, test signal to bypass internal ac coupling, Viterbi overwrite enabled. Test both polarities of signal with 1, 2, 3 & 4 intervening zeros between 1s of same polarity (per interleave).			TBD (15)	mV
PLLP 0-to-1 Transition to Path Memory Set Released.		Read mode			75	ns
Viterbi DAC Differential Nonlinearity					1	LSB

DETECTING SERVO DEMODULATOR

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Servo Input Frequency	f_{INS}		4		13.5	MHz
Gain $[(V_{SVO}-V_{SVR})/V_{LQ}]$	AV_S	measured over 1/4 to 3/4 of scale [4]		TBD		V/V
Linearity of V_{FN} vs. V_{DI}	V_{FL}	measured over 1/8 to 7/8 of scale [6]	–0.5		0.5	%
Linearity of $V_{SVO}-V_{SVR}$ vs. V_{DI}	V_{DL1}	measured over 1/8 to 3/4 of scale [6]	–1.4		1.4	%
	V_{DL2}	measured over 3/4 to 7/8 of scale [6]	–4.5		4.5	%
Output Offset (not referred to input)	V_{SO}	intercept of regressed line [6]	–40		40	mV
Output for Zero Input	V_{ZI}	6	0	30	60	mV
Channel A, B, C & D Mismatch	V_{MM}	Variation for a common input % of full scale			±1.0	%
SREF Voltage	V_{SR}		3.50	3.60	3.70	V
Integrating Cap Decay Rate	V_{DR}	0.1% of full scale droop in 50µs			40	V/sec
Channel to Channel Cross Talk	V_{CT}	Effect of A on B etc. % of full scale			±0.5	%
Output Impedance	R_{SO}	SREF and SRVOUT pins			50	Ω
Demodulator Repeatability (52dB)	N_{DR}	Repeatability without external noise			±5.0	mV
Power Supply Rejection Ratio	$PSRR_S$	f_{in} = 5MHz, V_{DI} = 0V, ΔV_{CC} or ΔV_{EE} = 100mV_{pp} [8]	25			dB
Common Mode Rejection Ratio	$CMRR_S$	0MHz ≤ f_{in} ≤ 1MHz V_{LQP} = V_{LQN} = 100mV_{pp} [8]	25			dB
Total System Gain Variation $[(V_{SVO}-V_{SVR})/V_{DI}]$	AV_A	over all V_{DI}, 1/4 to 3/4 of scale [4]		TBD		V/V

[4] This specification is the slope of the characteristic ratio of a DC voltage to a peak to peak voltage.
[5] V_{DIL} and V_{DIH} specify the input range over which all other specifications must be met.
[6] In addition to the linearity and offset specifications, the output must also be guaranteed monotonic.
[7] Refer to waveshapes below for this specification.
[8] The required demodulator output Signal-to-Noise Ratio (SNR) due to external noise is 49dB.

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FREQUENCY SYNTHESIZER

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
VCO Frequency	f_{VCO}	$X=f_{0(VCO)}\cdot(1+k_v\cdot(V_{fsfp}-V_{fsfn}))$				MHz
		Guaranteed Range	51		203	MHz
VCO Center Frequency	$f_{0(VCO)}$	$X=k_I\cdot I_{REF}\cdot(33+K_{fsf})$	0.90·X		1.10·X	MHz
VCO Gain	k_v	measured at TP4P/N	0.30		0.40	V^{-1}
VCO Dynamic Range	$f_{dr(VCO)}$	$V_{fsfp}=V_{fsfn}$, K_{fsf}=0 to 32	±2			% / LSB
RR Voltage	V_{rr}		1.20	1.28	1.36	V
FSFP Voltage	V_{fsfp}		V_{fsfn}-1.0		V_{fsfn}+1.0	V
FSFN Voltage	V_{fsfn}		2.10	2.35	2.60	V
FSFILT Leakage Current	$I_{Lfsfilt}$				±300	nA
FS Charge Pump Current	I_{fsqp}	$X=I_{REF}(0.5+((31-K_{fsf})/62))$	0.90·X		1.10·X	µA
		Guaranteed Range	100		700	µA
Closed Loop Jitter	σ_F	VCO output, sample size=100,000 samples		100		ps

k_I is 5.05 MHz/mA
K_{fsf} is the value of the Data Rate DAC word, [0 to 31]
I_{REF} is the reference current being sunk from pin RR in µA, $I_{REF}=V_{rr}/R_{ext}$

TR (TIMING RECOVERY) LOOP

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
TRVCO Frequency	f_{TRVCO}	$X=f_{0(TRVCO)}\cdot(1+k_v\cdot(V_{dsfp}-V_{dsfn}))$ DAMP DAC = 127	53		160	MHz
TRVCO Center Frequency	$f_{0(TRVCO)}$	$X=k_I\cdot I_{REF}\cdot(33+K_{fsf})$, DAMP DAC = 127	0.90·X		1.10·X	MHz
TRVCO Gain	k_v	measured at TP4P/N, DAMP DAC = 127	0.35		0.45	V^{-1}
TRVCO Dynamic Range	$f_{dr(TRVCO)}$	$V_{dsfp}=V_{dsfn}$, K_{fsf}=0 to 32	±2			% / LSB
DSFP/N CM Voltage	V_{CM}		1.80	2.10	2.40	V
TR Charge Pump Gain (I_{QP}/Timing Error)	I_{TRQP}	Idle/Acquisition Mode	322	460	598	µA/V
		Tracking Mode: TRGAIN = 0	18	26	34	µA/V
		TRGAIN = 1	81	115	150	µA/V
Pmult Gain (TRVCO Cntl/Tmg Err.)	k_{PMULT}	$X=0.35((127-K_{pmult})/127)$: Idle/Acq. $X=0.088((127-K_{pmult})/127)$:Trck, TRGAIN=0 $X=0.175((127-K_{pmult})/127)$: Trck,TRGAIN=1. DSFP=DSFN, DR DAC = 0	-20		+20	%

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Closed Loop Jitter	σ_F	TRVCO output, sample size=100,000 samples		100		ps

k_I is 3.98MHz/mA
K_{fsf} is the value of the Data Rate DAC word, [0 to31]
K_{pmult} is the value of the Damping Ratio DAC word, [0 to127]
I_{REF} is the reference current being sunk from pin RR in µA, $I_{REF}=V_{rr}/R_{ext}$

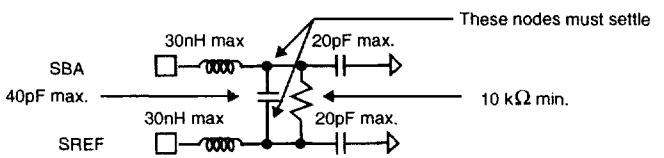
TIMING PARAMETERS

AC CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified. 0°C < T_A < 70°C, 4.5V < VCC < 5.5V

SERVO DEMODULATOR TIMING

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
SRST Pulse Width	T_{SR}		600			ns
DEMOD Pulse Width	T_{DMD}		150			ns
DEMOD Recovery Time	T_{REC}		150			ns
DEMOD to Corresponding Select Ciock Delay	T_{DS}		0			ns
Trailing Edge SRST to SBA-SBD Reset Delay	T_R	0.25% of final value [9]	150			ns
Trailing Edge SRST to DEMOD Recovery	T_{RR}		100			ns

[9] Load conditions given below.



MIXED SIGNAL CIRCUITS

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SERVO SYSTEM TIMING

Pins: SG, DEMOD

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
FSREC Leading Edge to V_{FN} Stable	T_{FD}	V_{FN} stable within 10%			2.3	µs
Trailing Edge of LOWZ to V_{FN} Stable to 10%	T_{WR}	CAGCD value correct			500	ns
Lead, Trailing Edge SG to V_{FN} stable 10%	T_{GS}	CAGCS or D value correct			500	ns
WG Pulse Width (given for reference only)	T_{WG}		1.6			µs

WRITE PRECOMPENSATION

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WPC Resolution (absolute max)	T_{pc}	X = (0.04·T)/16 for patterns 1&3 X = (0.02·T)/16 for pattern 2	0.9·X		1.1·X	ns
WPC Delay	T_{wpc}	X = (0.013·K_{wp} +0.20·WPCHR)·T 1&3 X = 0.013·K_{wp}·T Pattern 2	0.9·X		1.1·X	ns
T is the period of the VCO clock WPCHR is the WPC high range bit in serial register K_{wp} is value of the write precompensation DAC word [0 to 15]						

DIGITAL BACKEND I/O

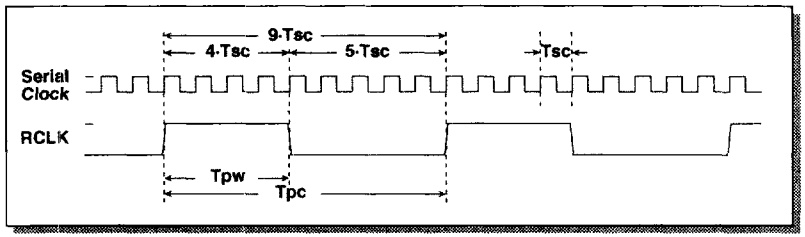

Diagram 12a Byte-Wide RCLK with respect to serial clock, Normal

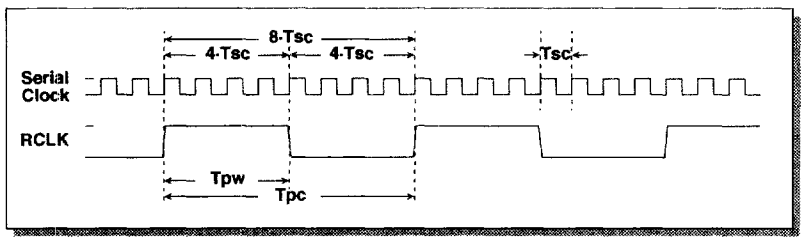

Diagram 12b Byte-Wide RCLK with respect to serial clock, Direct Test

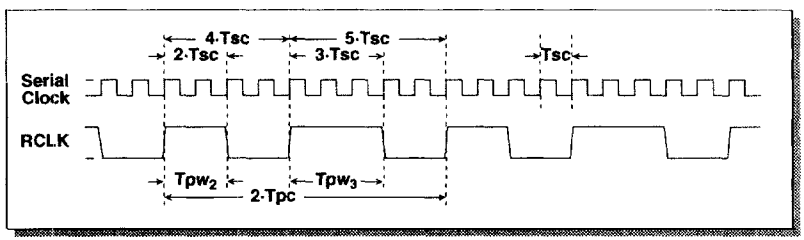

Diagram 12c Nibble-Wide RCLK with respect to serial clock, Normal

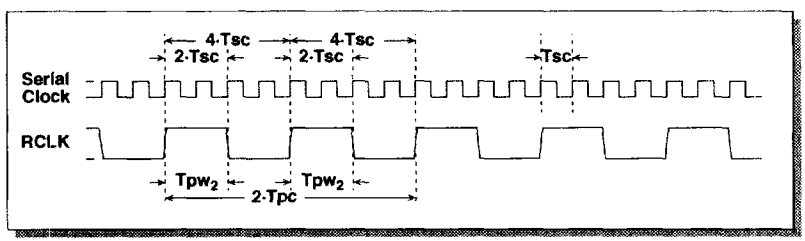

Diagram 12d Nibble-Wide RCLK with respect to serial clock, Direct Test

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Channel Clock Frequency	f_{chclk} (max)	Data Rate=140Mbit/s	157.5			MHz
Parallel Read Clock Frequency	f_{RCLK} (max)	Control Reg Bit DTM=0; Byte-wide	17.5	$1/9 \cdot f_{chclk}$		MHz
		Control Reg Bit DTM=1; Byte-wide	19.7	$1/8 \cdot f_{chclk}$		MHz
Serial Channel Clock Period	T_{SC} (min)	Data Rate=140Mbit/s			6.35	ns
		Data Rate=180Mbit/s			4.94	ns
Parallel Read Clock Pulse Width	TPW	at 1.5V points; $C_L \leq 15pF$	$4 \cdot T_{SC} - x$		$4 \cdot T_{SC} + x$	ns
	TPW2	at 1.5V points; $C_L \leq 15pF$	$2 \cdot T_{SC} - x$		$2 \cdot T_{SC} + x$	ns
	TPW3	at 1.5V points; $C_L \leq 15pF$	$3 \cdot T_{SC} - x$		$3 \cdot T_{SC} + x$	ns
Parallel Read Clock Period	T_{PC}	Byte-wide, Normal Operation	$9 \cdot T_{SC}$	$9 \cdot T_{SC}$	$9 \cdot T_{SC}$	ns
		Byte-wide, Direct Test	$8 \cdot T_{SC}$	$8 \cdot T_{SC}$	$8 \cdot T_{SC}$	ns
	$2 \cdot T_{PC}$	Nibble-wide, Normal Operation	$9 \cdot T_{SC}$	$9 \cdot T_{SC}$	$9 \cdot T_{SC}$	ns
		Nibble-wide, Direct Test	$8 \cdot T_{SC}$	$8 \cdot T_{SC}$	$8 \cdot T_{SC}$	ns
Control Signal rise and fall times	t_{CS}	20% to 80%			< 10 >	ns
Recovery time Powerdown to fully functional	t_{REC}				<TBD>	ns

PARALLEL WRITE

Pins: WG, WCLK or RCLK, NRZ[8:1] or NRZ[4:1]

Timing Diagrams:

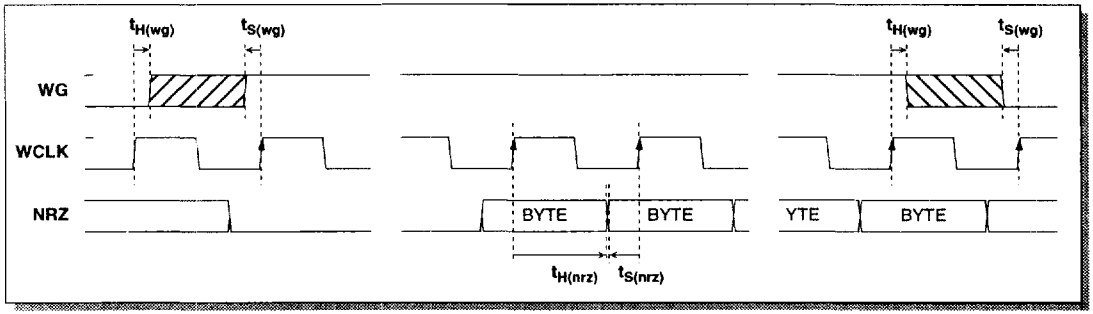

Diagram 13a Parallel Write Timing: WCLK, Byte-Wide

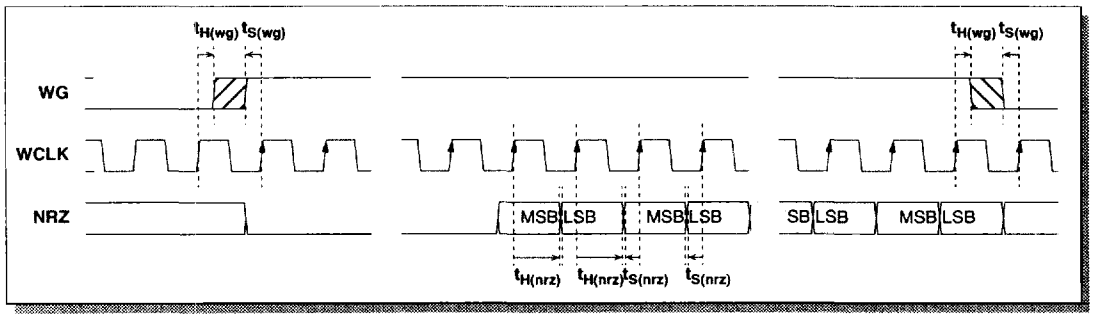

Diagram 13b Parallel Write Timing: WCLK, Nibble-Wide

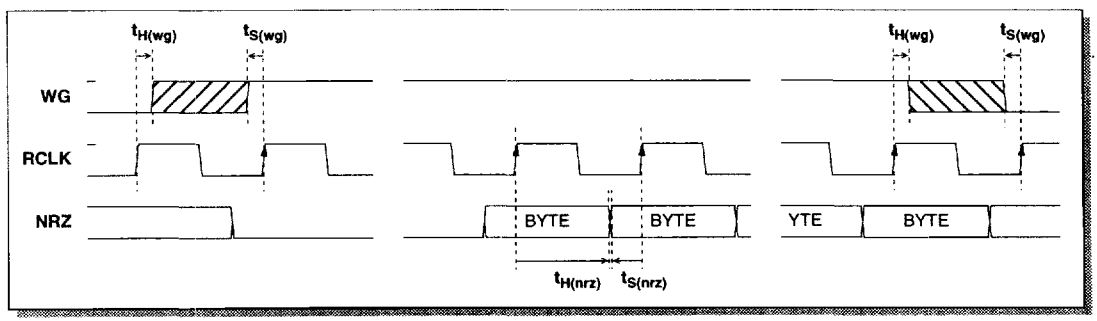

Diagram 13c Parallel Write Timing: RCLK Rising Edge, Byte-Wide

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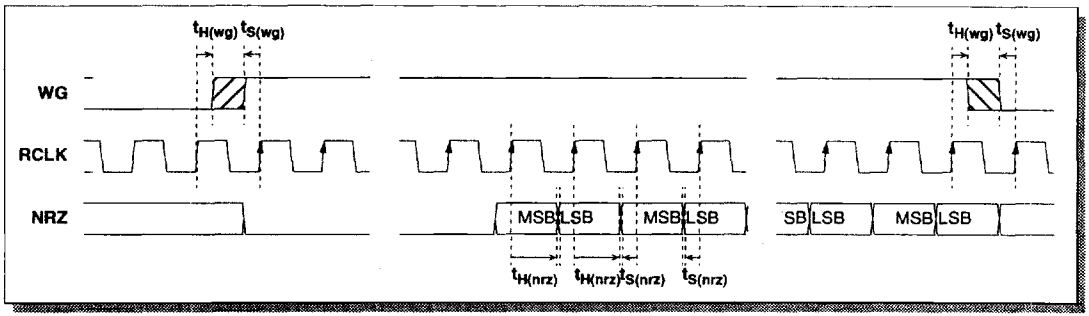

Diagram 13d Parallel Write Timing: RCLK Rising Edge, Nibble-Wide

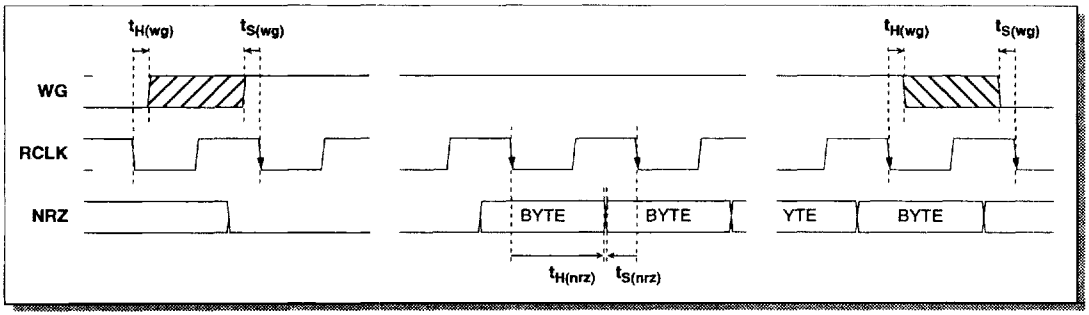

Diagram 13e Parallel Write Timing: RCLK Falling Edge, Byte-Wide

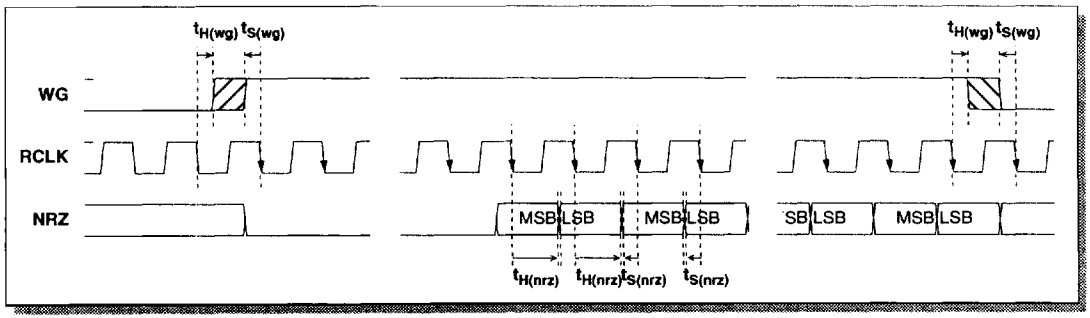

Diagram 13f Parallel Write Timing: RCLK Falling Edge, Nibble-Wide

(Parallel Write)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WG Hold Time	$t_{H(wg)}$	w.r.t. WCLK; at 1.5V points	<TBD>			ns
		w.r.t. RCLK; at 1.5V points	<TBD>			ns
WG Setup Time	$t_{S(wg)}$	w.r.t. WCLK; at 1.5V points	<TBD>			ns
		w.r.t. RCLK; at 1.5V points	<TBD>			ns
NRZ Hold Time	$t_{H(nrz)}$	w.r.t. WCLK; at 1.5V points	<TBD>			ns
		w.r.t. RCLK; at 1.5V points	<TBD>			ns
NRZ Setup Time	$t_{S(nrz)}$	w.r.t. WCLK; at 1.5V points	<TBD>			ns
		w.r.t. RCLK; at 1.5V points	<TBD>			ns
$\overline{WM}$ time prior to WM	$t\,\overline{WM}$	$\overline{WM}$ = Idle mode or Read mode	<TBD>			ns

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PARALLEL READ

Pins: RG, RCLK, SBF, NRZ[8:1] or NRZ[4:1]

Timing Diagrams:

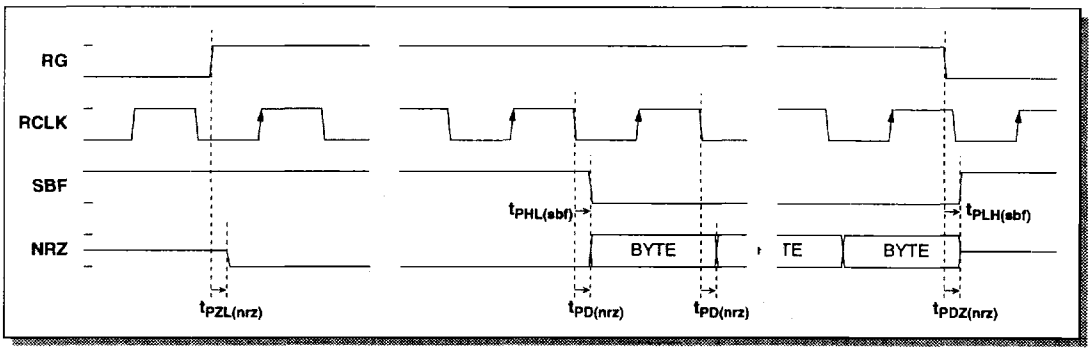

Diagram 14a Parallel Read Timing: Byte-Wide

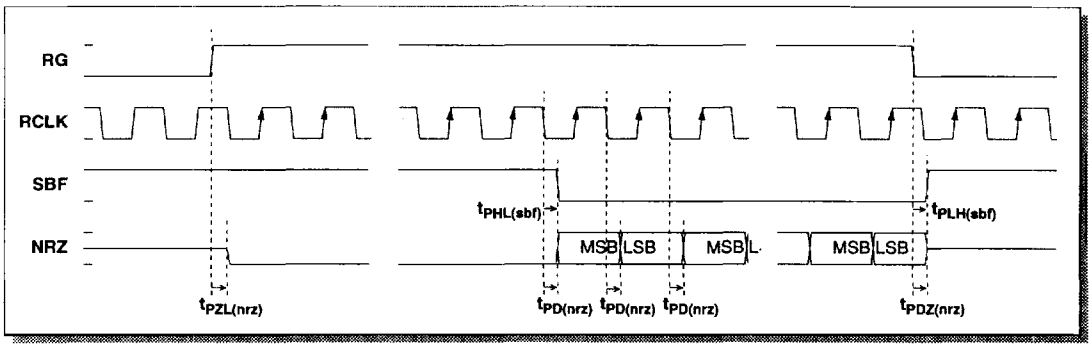

Diagram 14b Parallel Read Timing: Nibble-Wide

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
RCLK to SBF falling	$t_{PHL(sbf)}$	measured at 1.5V points; $C_L \leq 15pF$			<TBD>	ns
RG to SBF rising	$t_{PLH(sbf)}$	measured at 1.5V points; $C_L \leq 15pF$			<TBD>	ns
RG to NRZ enabled	$t_{PZL(nrz)}$	measured at 1.5V points; $C_L \leq 15pF$			<TBD>	ns
RCLK to NRZ change	$t_{PD(nrz)}$	measured at 1.5V points; $C_L \leq 15pF$			<TBD>	ns
RG to NRZ disabled	$t_{PDZ(nrz)}$	measured at 1.5V points; $C_L \leq 15pF$			<TBD>	ns
$\overline{RM}$ time prior to RM	t $\overline{RM}$	$\overline{RM}$ = Idle mode or Write mode	<TBD>			ns

SERIAL INTERFACE TIMING

PARAMETER	*SYM*		*MIN*	*TYP*	*MAX*	*UNITS*
SPCLK period	T		50			ns
SPEN set-up time	$T_{S(SPEN)}$	Relative to SPCLK ↑	40			ns
SPEN hold time	$T_{H(SPEN)}$	Relative to SPCLK ↑	50			ns
SPEN hi to low to hi (Time between successive operations)	T		50			ns
SPDATA set-up time	$T_{S(SPDATA)}$	Relative to SPCLK ↑	20			ns
SPDATA hold time	$T_{H(SPDATA)}$	Relative to SPCLK ↑	5			ns
SPDATA enable	T_{OEN}	Relative to SPCLK ↓	5			ns
SPCLK low time	T_{OCLK}	Relative to SPCLK ↓	30			ns
SPDATA disable	T_{ODIS}	Relative to SPEN ↓			30	ns
Delay to SPDATA output data change	T_{PDD}	Relative to SPCLK ↑			10	ns

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