

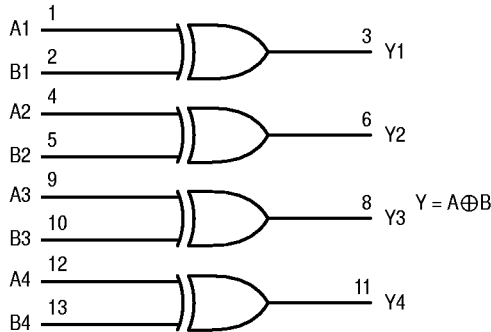
# Quad 2-Input XOR Gate

The MC74VHC86 is an advanced high speed CMOS 2-input Exclusive-OR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

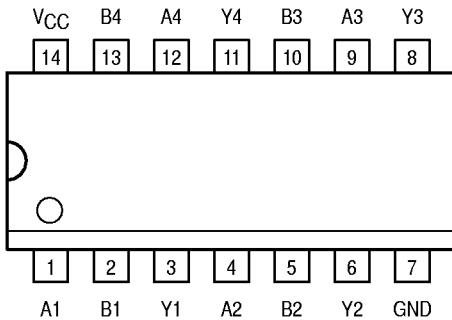
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed:  $t_{PD} = 4.8ns$  (Typ) at  $V_{CC} = 5V$
- Low Power Dissipation:  $I_{CC} = 2\mu A$  (Max) at  $T_A = 25^\circ C$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise:  $V_{OLP} = 0.8V$  (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 56 FETs or 14 Equivalent Gates

### LOGIC DIAGRAM



### Pinout: 14-Lead Packages (Top View)



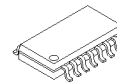
## MC74VHC86



**D SUFFIX**  
14-LEAD SOIC PACKAGE  
CASE 751A-03



**DT SUFFIX**  
14-LEAD TSSOP PACKAGE  
CASE 948G-01



**M SUFFIX**  
14-LEAD SOIC EIAJ PACKAGE  
CASE 965-01

### ORDERING INFORMATION

MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L



**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage	- 0.5 to + 7.0	V
V <sub>out</sub>	DC Output Voltage	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current	- 20	mA
I <sub>OK</sub>	Output Diode Current	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

†Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	5.5	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	- 40	+ 85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> = 3.3V ±0.3V V <sub>CC</sub> = 5.0V ±0.5V	0 100 0 20	ns/V

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High-Level Input Voltage		2.0 3.0 to 5.5	1.50 V <sub>CC</sub> × 0.7			1.50 V <sub>CC</sub> × 0.7		V
V <sub>IL</sub>	Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 V <sub>CC</sub> × 0.3		0.50 V <sub>CC</sub> × 0.3	V
V <sub>OH</sub>	High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = - 50µA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = - 4mA I <sub>OH</sub> = - 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50µA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 4mA I <sub>OL</sub> = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	
I <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	µA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5			2.0		20.0	µA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay, A or B to Y	$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		7.0	11.0	1.0	13.0	ns
				9.5	14.5	1.0	16.5	
$C_{in}$	Input Capacitance	$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		4.8	6.8	1.0	8.0	pF
				6.3	8.8	1.0	10.0	

$C_{PD}$	Power Dissipation Capacitance (Note NO TAG)	Typical @ $25^\circ\text{C}$ , $V_{CC} = 5.0\text{V}$		pF
		18		

1.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$  (per gate).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

**NOISE CHARACTERISTICS** (Input  $t_r = t_f = 3.0\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $V_{CC} = 5.0\text{V}$ , Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	0.3	0.8	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-0.3	-0.8	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		3.5	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		1.5	V

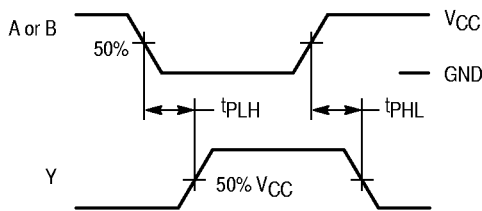
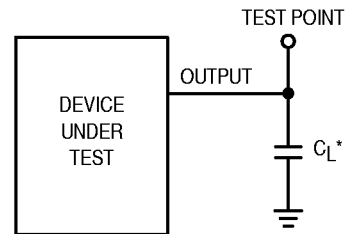


Figure 1. Switching Waveforms



\* Includes all probe and jig capacitance

Figure 2. Test Circuit

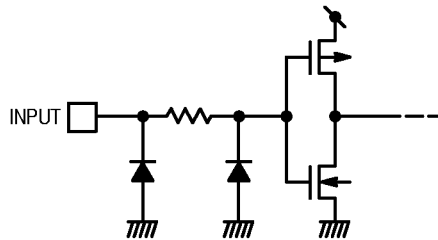
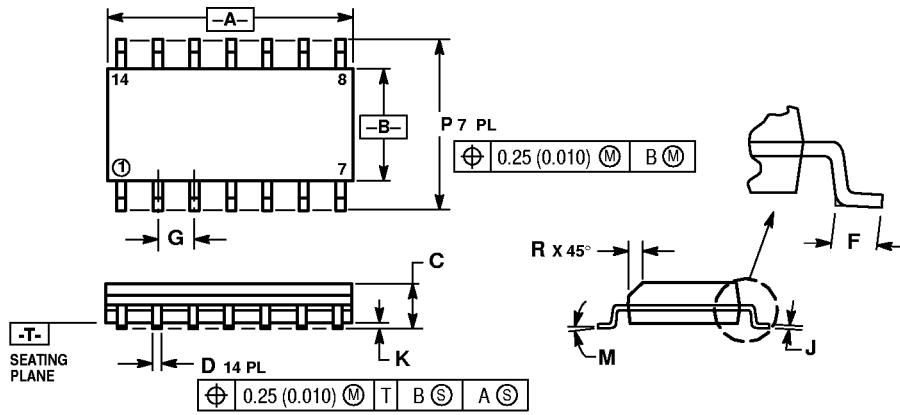


Figure 3. Input Equivalent Circuit

OUTLINE DIMENSIONS

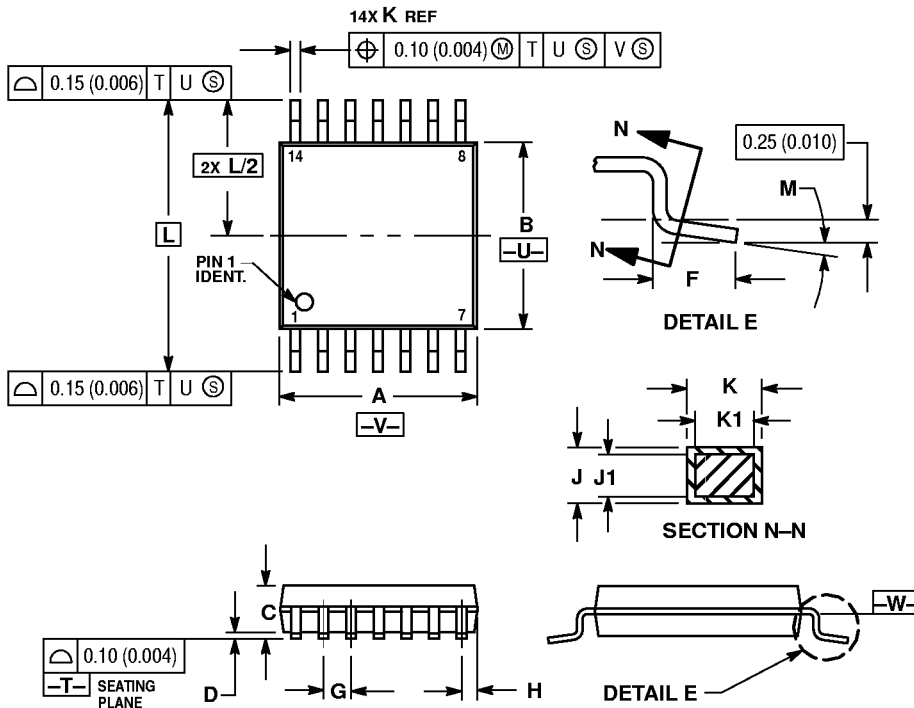
**D SUFFIX**  
 PLASTIC SOIC PACKAGE  
 CASE 751A-03  
 ISSUE F



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

**DT SUFFIX**  
 PLASTIC TSSOP PACKAGE  
 CASE 948G-01  
 ISSUE O

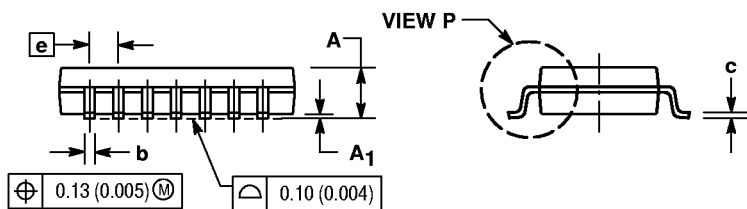
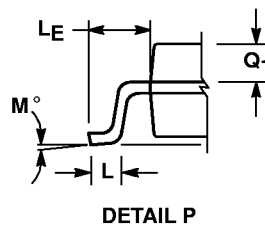
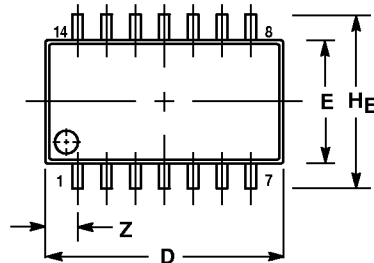


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

OUTLINE DIMENSIONS

**M SUFFIX**  
**PLASTIC SOIC EIAJ PACKAGE**  
**CASE 965-01**  
**ISSUE O**



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>F</sub>	7.40	8.20	0.291	0.323
0.5D	0.50	0.85	0.020	0.033
L <sub>F</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	—	1.42	—	0.056

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