OKI Semiconductor

MSM5279

80-DOT SEGMENT DRIVER

GENERAL DESCRIPTION

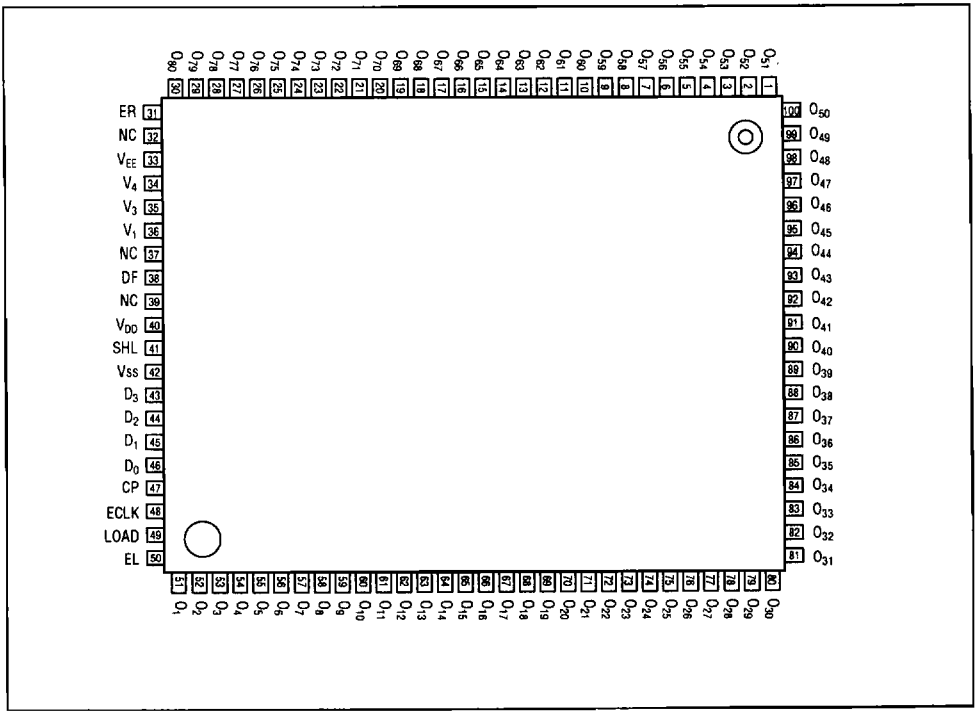
The MSM5279 is a dot matrix LCD segment driver LSI, which is fabricated by CMOS low power metal gate technology. This LSI consists of 80-bit bidirectional shift register, 80-bit latch, 80-bit level shifter and 80-bit 4-level driver.
It receives the display driving data, which consists of 4-bit parallel, from the LCD controller LSI, then outputs the LCD driving waveform to the LCD panel.
The MSM5279 has a power down function which permits reduced power consumption.
The MSM5279 can drive a variety of LCD panels because the bias voltage, which determines the LCD driving voltage, can be supplied from the external source.

FEATURES

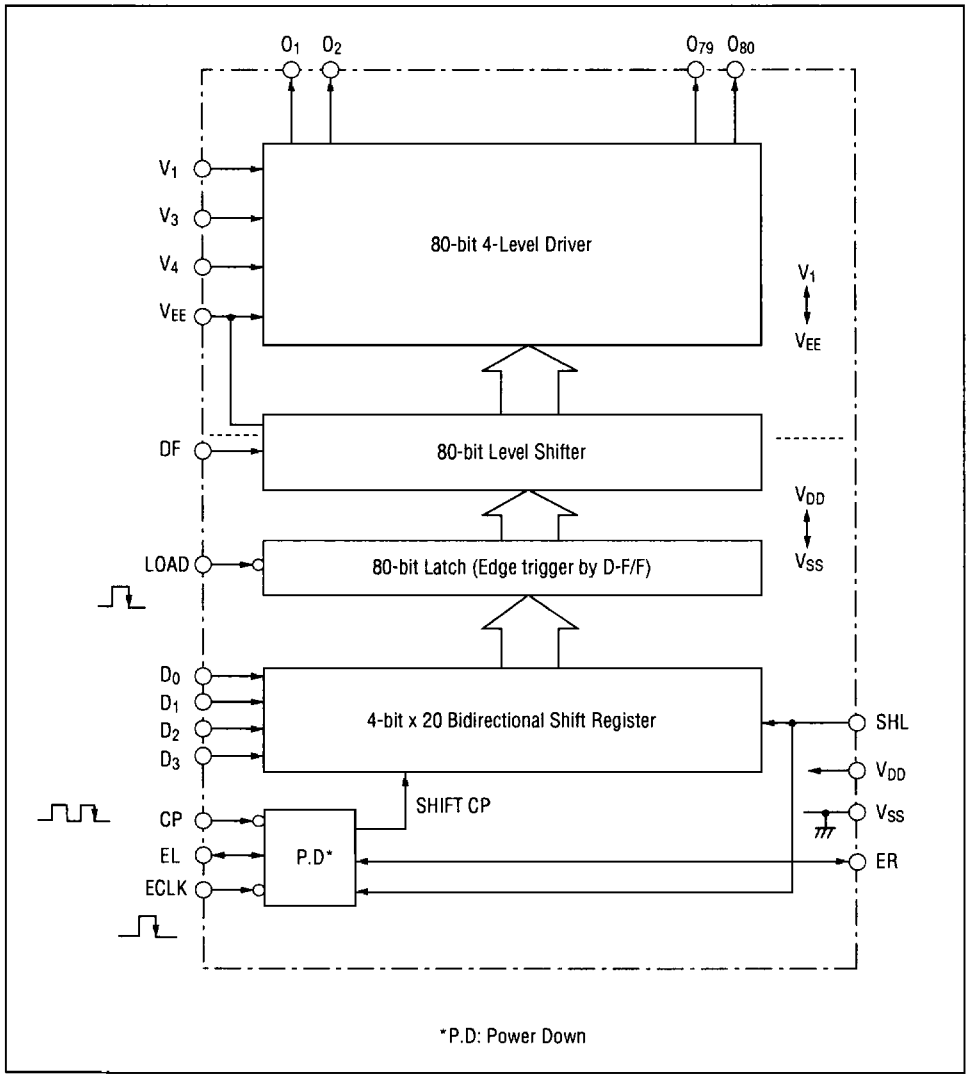
- Supply voltage : 4.5 ~ 5.5V
- LCD driving voltage : 8 ~ 20V
- Applicable LCD duty : 1/64 ~ 1/128
- Bias voltage can be supplied externally
- Power down function
- 4-bit parallel data processing
- Can be interfaced with the MSM6255, MSM6265, LCD controller LSI
- 100-pin plastic QFP (QFP100-P-1420-K)

PIN CONFIGURATION

(Top view) 100-pin plastic QFP



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	T_a = 25°C	-0.3 ~ 6	V
Supply Voltage (2)	V_{DD} - V_{EE}*1	T_a = 25°C	0 ~ 22	V
Input Voltage	V_I	T_a = 25°C	-0.3 ~ V_{DD} +0.3	V
Storage Temperature	T_{stg}	–	-55 ~ +150	°C

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_1 \leqq V_{DD}$

• Operating Range

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	–	4.5 ~ 5.5	V
Supply Voltage (2)	V_{DD} - V_{EE}*1	–	8~ 20	V
Operating Temperature	Top	–	-20 ~ +85	°C

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_1 \leqq V_{DD}$

• DC Characteristics

(V_{DD} = 5V±10%, Ta = -20 ~ +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}*1	–	0.8V_{DD}	–	–	V
"L" Input Voltage	V_{IL}*1	–	–	–	0.2V_{DD}	V
"H" Input Current	I_{IH}*1	$V_{IH} = V_{DD}$	–	–	1	µA
"L" Input Current	I_{IL}*1	V_{IL} = 0V	–	–	-1	µA
"H" Output Voltage	V_{OH}*2	I_O = -0.2mA	V_{DD} - 0.4	–	–	V
"L" Output Voltage	V_{OL}*2	I_O = 0.2mA	–	–	0.4	V
ON Resistance	R_{ON}*4	V_{DD}-V_{EE} = 18V *3 $\|V_N$-$V_O\|$ = 0.25V	–	2	4	kΩ
Stand-by Current*Consumption	I_{DD}SBY	CP =1MHz V_{DD}-V_{EE} = 18V, No load*5	–	–	200	µA
Current Consumption (1)	I_{DD1}	CP = 1MHz V_{DD}-V_{EE} = 18V, No load*6	–	–	4	mA
Current Consumption (2)	IV	CP = 1MHz V_{DD}-V_{EE} = 18V, No load*7	–	–	±100	µA
Input Capacitance	C_I	f = 1MHz	–	5	–	pF

*1 Applicable to LOAD, CP, D_0 ~ D_3, ECLK, EL, ER, SHL, DF terminals.
*2 Applicable to EL, ER terminals.

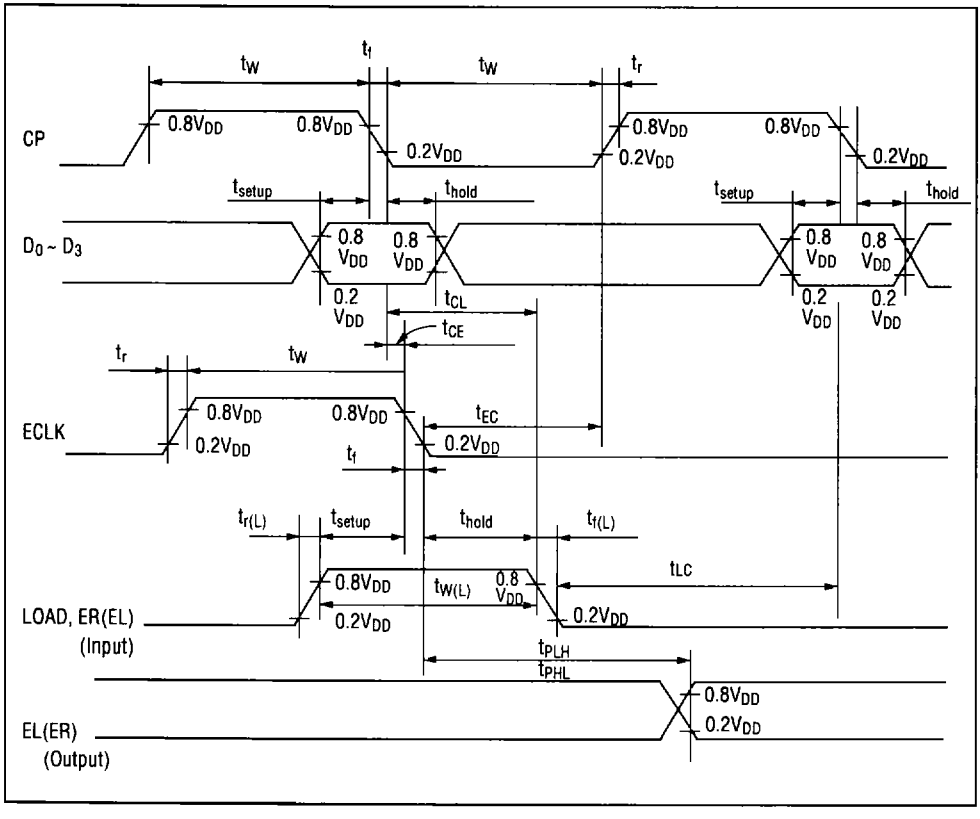
*3 $V_N = V_{DD} - V_{EE}$, $V_3 = \frac{9}{11}(V_{DD} - V_{EE})$, $V_2 = \frac{2}{11}(V_{DD} - V_{EE})$, $V_{DD} = V_1$.

*4 Applicable to O_1 ~ O_{80} terminals.
*5 Display data 1010 ..... DF=40Hz, current from V_{DD} to V_{SS} when the display data is not processing.
*6 Display data 1010 ..... DF=40Hz, current from V_{DD} to V_{SS} when the display data is processing.
*7 Display data 1010 ..... DF=40Hz, current on V_1, V_3, V_4 and V_{EE} terminals.

• Switching Characteristics

(V_{DD} = 5V±10%, Ta = -20 ~ +85°C, C_L = 15pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" propagation delay time	t_{PLH}, t_{PHL}	–	–	–	250	ns
MAX. clock frequency	f_{CP}	DUTY = 50%	3	–	–	MHz
CP ECLK pulse width	t_W	–	125	–	–	ns
Load pulse width	$t_{W(L)}$	–	125	–	–	ns
Data set-up time	t_{setup}	–	100	–	–	ns
CP → LOAD time	t_{CL}	–	250	–	–	ns
LOAD → CP time	t_{LC}	–	0	–	–	ns
Data hold time CP → D_0 ~ D_3, ECLK → LOAD	t_{hold}	–	100	–	–	ns
Clock pulse Rising/Falling time	t_r t_f	–	–	–	50	ns
Load pulse Rising/Falling time	$t_{r(L)}$ $t_{f(L)}$	–	–	–	1	µs
CP → ECLK time	t_{CE}	–	0	–	–	ns
ECLK → CP time	t_{EC}	–	150	–	–	ns



PIN DESCRIPTION

- **ER, EL**

Pin	Input/Output	SHL	Description
ER	Input	L	Input pin to ENABLE F/F of MSM5279
EL	Output		Output pin of ENABLE F/F. EL is connected to next MSM5279's ER when MSM5279s are connected in series (cascade connection).
EL	Input	H	Input pin to ENABLE F/F of MSM5279
ER	Output		Output pin of ENABLE F/F. ER is connected to next MSM5279's EL when MSM5279s are connected in series (cascade connection).

- **ELCK**

Clock pulse input pin for ENABLE F/F. The active condition of ENABLE F/F is shifted to next MSM5279's ENABLE F/F at the falling edge of the clock pulse. ELCK is required every 20 CPs. (Clock Pulse).

- **CP**

Clock pulse input pin for the 4-bit parallel shift register. The data is shifted to 80-bit latch at the falling edge of the clock pulse. The clock pulse, which was input when the ENABLE F/F is not in the active condition, is invalid.

- **SHL**

ER and EL can be used as either an input pin or an output pin depending on the H/L condition of SHL. The shifting direction of each data, $D_0 \sim D_3$, the Input/Output condition of ER and EL and the H/L condition of SHL are described in the table below.

SHL	ER	EL	Shifting direction
L	Input	Output	$D_0 \rightarrow O_1 \rightarrow O_5 \longrightarrow O_{77}$ $D_1 \rightarrow O_2 \rightarrow O_6 \longrightarrow O_{78}$ $D_2 \rightarrow O_3 \rightarrow O_7 \longrightarrow O_{79}$ $D_3 \rightarrow O_4 \rightarrow O_8 \longrightarrow O_{80}$
H	Output	Input	$D_0 \rightarrow O_{80} \rightarrow O_{76} \longrightarrow O_4$ $D_1 \rightarrow O_{79} \rightarrow O_{75} \longrightarrow O_3$ $D_2 \rightarrow O_{78} \rightarrow O_{74} \longrightarrow O_2$ $D_3 \rightarrow O_{77} \rightarrow O_{73} \longrightarrow O_1$ ↑ end data ↑ start data

- **D_0, D_1, D_2, D_3**

Data input pins for 4-bit parallel shift register and it is input synchronized with the clock pulse. The combination of D_0 - D_3 level, DF signal, display data output level and the display on the LCD panel is described on the table below.

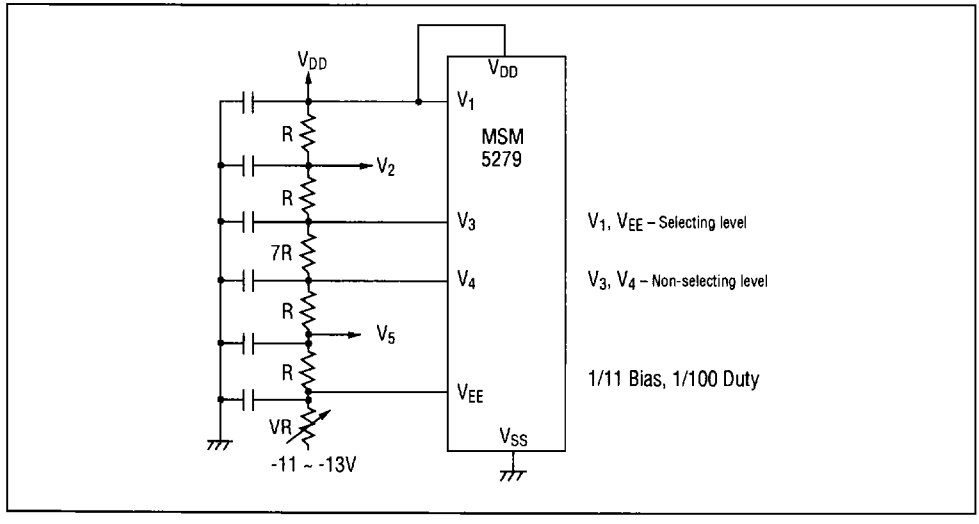
$D_0 \sim D_3$	DF	Display data output level	Display on the LCD
L	L	V_3	OFF
H	L	V_1	ON
L	H	V_4	OFF
H	H	V_{EE}	ON

- **LOAD**
  The signal for latching the shift register contents is input from this pin. When LOAD pin is set at "H" level, the shift register contents are transferred to 80-bit latch at the falling edge of the LOAD pulse. When more than two MSM5279s are connected in series, cascade connection, the first MSM5279's EL terminal (when SHL = "H") or ER terminal (when SHL = "L") should be connected with the first MSM5279's LOAD terminal.

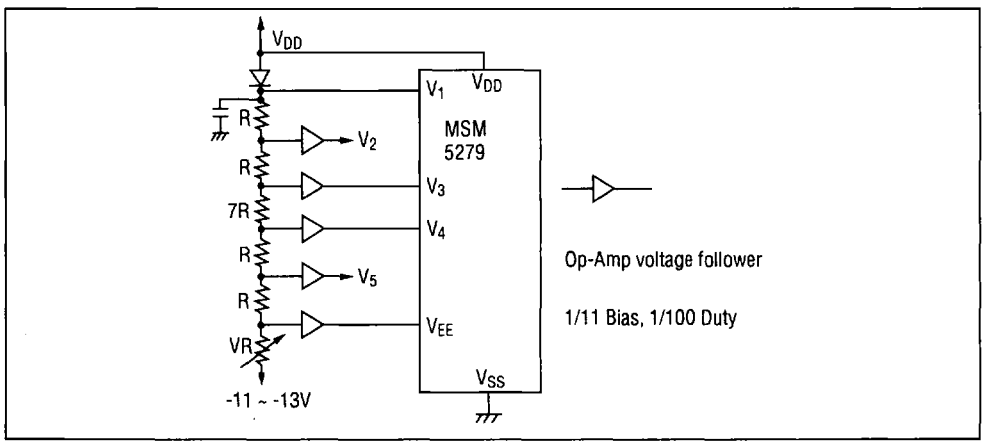
- **DF**
  Alternate signal input pin for LCD driving. Frame inversion signal is input to this terminal.

- **V_{DD}, V_{SS}**
  Supply voltage pins. V_{DD} should be 4.5 ~ 5.5V. V_{SS} is a ground pin (V_{SS}=0V).

- **V_1, V_3, V_4, V_{EE}**
  Bias supply voltage pin to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source. The figure below shows the case when bias voltage, which determines the LCD driving voltage, is supplied from the external source. V_1 is not necessarily connected with V_{DD}.



The figure below shows the case when the bias voltage is supplied by using Op-Amps, which enables the bias source at low impedance and low power consumption.



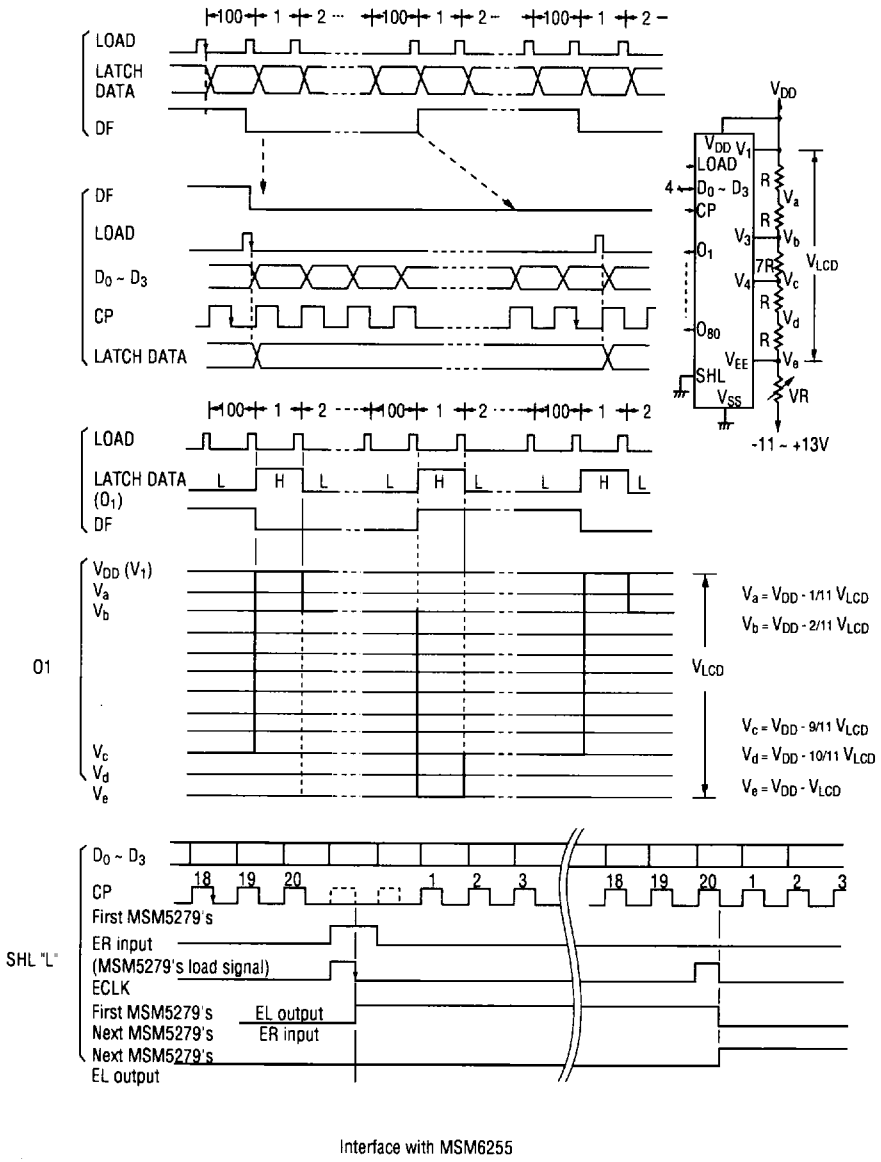
- **O_1 - O_{80}**

Display data output pin which corresponds to the respective latch contents. One of V_1, V_3, V_4 and V_{EE} is selected as a display driving voltage source according to the combination of the latched data level and DF signal. (Refer to the truth table below.)

DF	Latched data	Display data output level
L	L	V_3
L	H	V_1
H	L	V_4
H	H	V_{EE}

Truth table

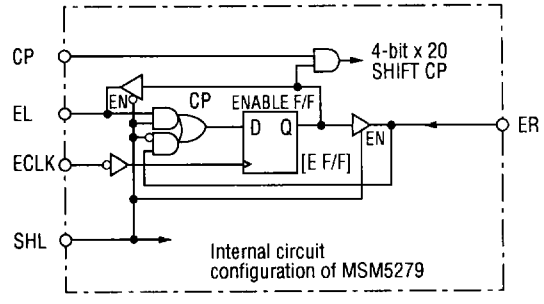
TIMING CHART (1/100 duty, 1/11 Bias)

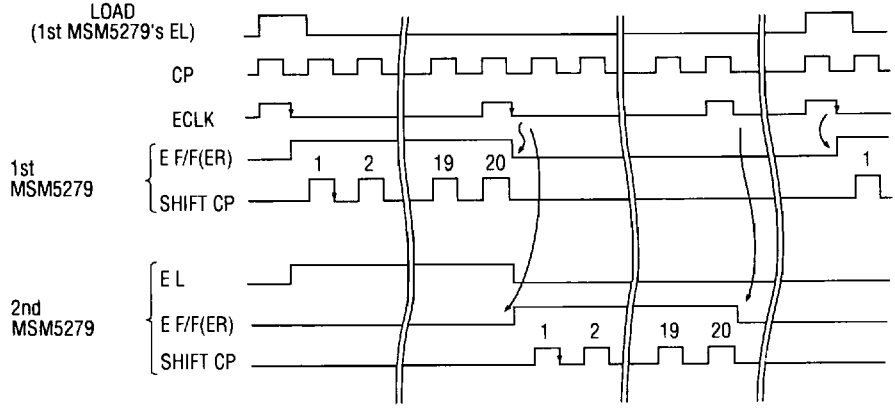


Interface with MSM6255

POWER SAVE FUNCTION

When more than two MSM5279s are connected in series, cascade connection,the power save function of MSM5279 can be utilized with the ENABLE F/F (flip-flop circuit) in individual MSM5279s. (Regarding the internal circuit configuration of MSM5279, refer to the figure below.) The display data is processed only in the MSM5279 where the ENABLE F/F is being activated by setting its ER or EL at high level. While the display data is not processed in the MSM5279 where the ENABLE F/F is not being activated and the low power consumption condition (I_{DD} SBY) is being held. The active condition of this ENABLE F/F is being shifted to next MSM5279 one after another so that the ENABLE F/F of only one MSM5279 out of the cascade-connected MSM5279s should be being activated.





SHL = "H" (EL = Input ER = Output)
First MSM5279's ER should be
connected to second MSM5279's EL

Timing chart in the case of cascade connection

APPLICATION CIRCUIT