LATTICE

LAT **SR64K8**

HIGH-SPEED 64K STATIC RAM (8K×8)

FEATURES

- **FULLY STATIC**
  - — No Clocks Required
- **FAST ACCESS TIME = CYCLE TIME**
  - — SR64K8-35: 35ns Max
  - — SR64K8-40: 40 ns Max
  - — SR64K8-45: 45ns Max
  - — SR64K8-55: 55ns Max
- **SINGLE POWER SUPPLY**
  - — 5V ± 10%
- **OUTPUT ENABLE**
  - — Improved bus control
- **CMOS FOR LOW POWER**
  - — I_{CC} Standby = 20mA Max
- **STANDARD PINOUT**
  - — JEDEC-Approved
  - — 28-Pin, 0.3 inch SB DIP
  - — 28-Pin, 0.6 inch SB DIP
  - — 32-Lead, LCC
  - — 32-Lead, PLCC
- **TTL LOGIC LEVELS ON ALL PINS**
- **THREE STATE I/O**

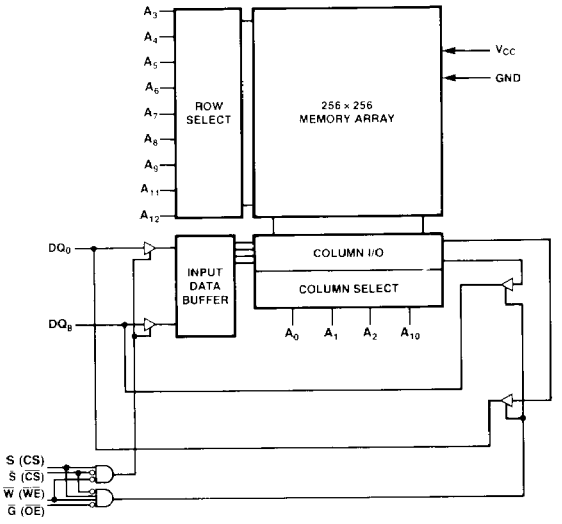
DESCRIPTION

The SR64K8 is a 65,536-bit high-speed static RAM organized as 8K x 8. It is fabricated using LATTICE's high-performance, high-reliability CMOS technology: UltraMOS® . This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

Access times as fast as 35ns are available. The output enable function eliminates any potential bus contention.

All of the inputs and outputs of the SR64K8 are completely TTL-compatible and the device operates from the a single 5V supply. Fully static asynchronous circuitry is used, which required no clocks for refreshing for operation, thus providing equal access and cycle times for ease of use.

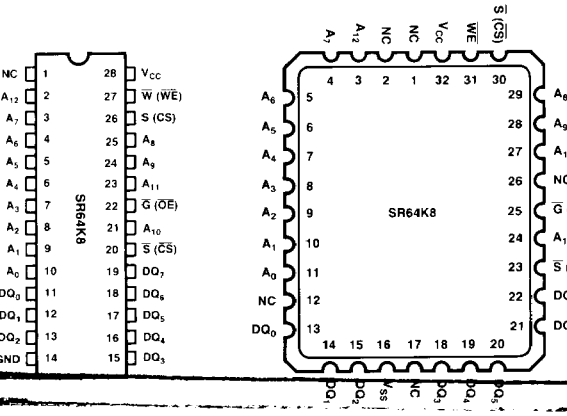
FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESS INPUTS	W (WE)	WRITE ENABLE
DQ_0-DQ_7	DATA INPUT/OUTPUT	V_{CC}	+5V
S(CS)	CHIP SELECT	GND	GROUND
G (OE)	OUTPUT ENABLE	NC	NO CONNECT

PIN CONFIGURATIONS



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August, 1986

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APPLICATIONS HOTLINE: 1-800-FASTMEM

SR64K8 HIGH-SPEED 64K STATIC RAM (8K×8)

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−3.0 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	°C
T_{STG}	Storage Temperature	−65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	10	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open Cycle Time = 50ns	—	—	170	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH}	—	20	35	mA
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.0mA	2.4	—	—	V
V_{IH}	Input High Voltage		2.0	—	V_{CC} MAX + .5V	V
V_{IL}(2)	Input Low Voltage		−2.0	—	0.8	V

1. V_{CC} = 5V, T_A = 25°C.
2. $V_{IL_{MIN}}$ = −2.0V for pulse widths less than 20 ns.

TRUTH TABLE

MODE	$\overline{CS}$	CS	$\overline{OE}$	$\overline{WE}$	DQn	POWER
Standby	H	X	X	X	High-Z	Standby
Standby	X	L	X	X	High-Z	Standby
Read	L	H	H	H	High-Z	Active
Read	L	H	L	H	Q_{OUT}	Active
Write	L	H	X	L	D_{IN}	Active

AC TEST CONDITIONS(1)

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

1. Operation to specifications guaranteed 2ms after V_{CC} applied.

CAPACITANCE(1) (T_A = 25°C, f = 1.0 MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

1. This parameter is sampled and not 100% tested.

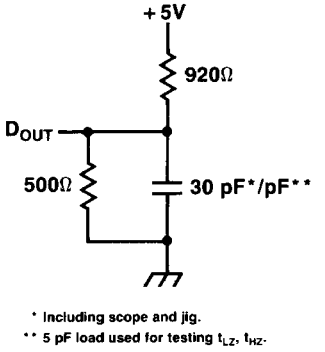
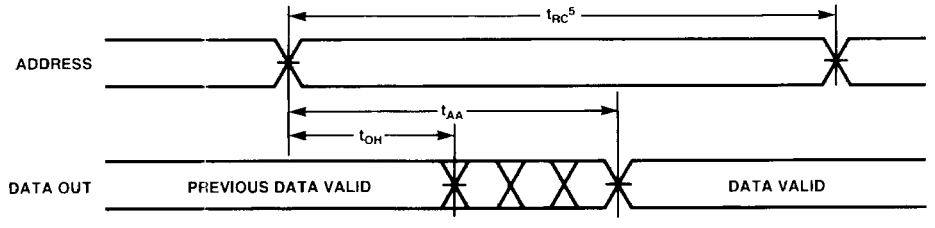


Figure 1. Output Load

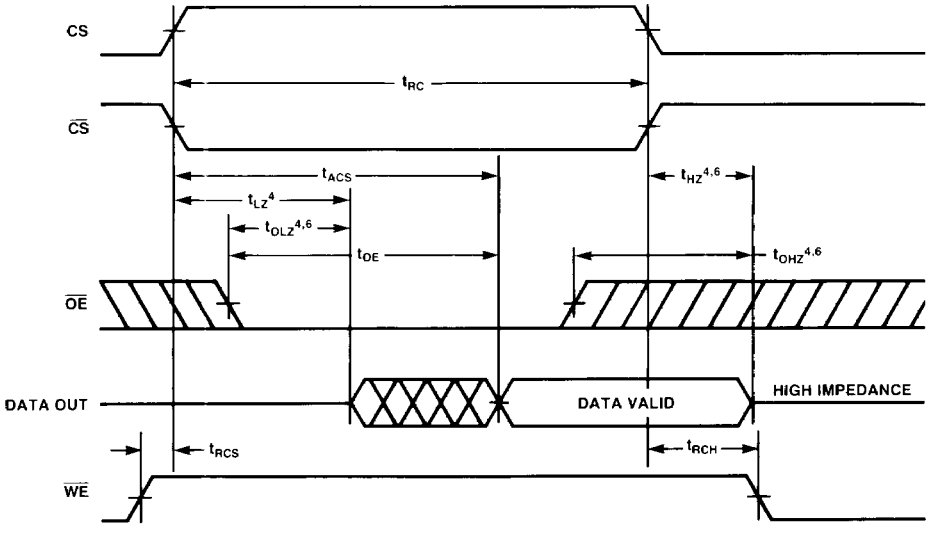
AC ELECTRICAL CHARACTERISTICS (READ CYCLE) (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		SR64K8-35		SR64K8-40		SR64K8-45		SR64K8-55		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNITS
t_{RC}	Read Cycle Time	35	—	40	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	40	—	45	—	55	ns
t_{ACS}	Chip Select Access Time	—	35	—	40	—	45	—	55	ns
t_{OH}	Output Hold From Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ}	Time to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselection to Output in High Z	—	20	—	25	—	25	—	25	ns
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	0	—	ns
t_{RCH}	Read Command Hold Time	-5	—	-5	—	-5	—	-5	—	ns
t_{OE}	Output Enable to Data Valid	—	20	—	25	—	25	—	25	ns
t_{OHZ}	Output Enable to High Z	—	20	—	20	—	25	—	25	ns
t_{OLZ}	Output Enable to Low Z	0	—	5	—	5	—	5	—	ns

TIMING OF READ CYCLE NO. 1[1,2]



TIMING OF READ CYCLE NO. 2[1,3]

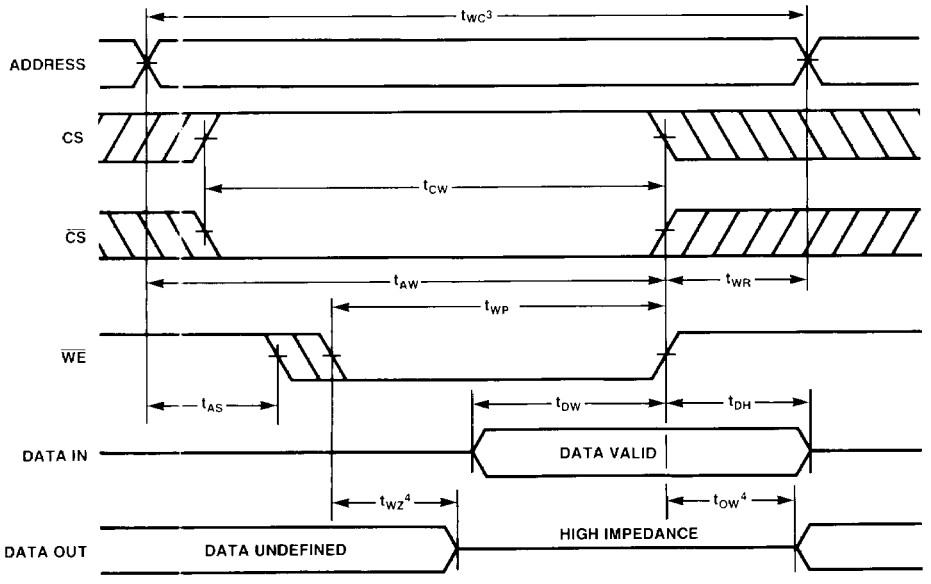


NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ and $\overline{OE}$ are low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 1. This parameter is sampled and not 100% tested.
5. READ cycle timing #1 is referenced from the last valid address to the first transitioning address.
6. For any given speed grade, operating voltage, and temperature, t_{HZ} will be less than or equal to t_{LZ}.

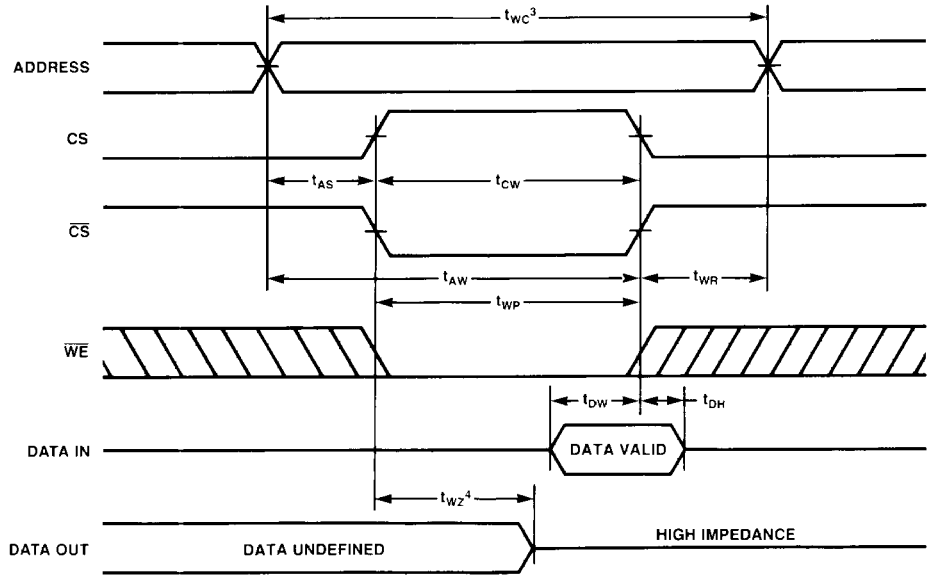
AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE) (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		SR64K8-35		SR64K8-40		SR64K8-45		SR64K8-55		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNITS
t_{WC}	Write Cycle Time	35	—	40	—	45	—	55	—	ns
t_{CW}	Chip Selection to End of Write	25	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	35	—	40	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	30	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	15	—	20	—	30	—	ns
t_{DH}	Data Hold Time	5	—	5	—	5	—	5	—	ns
t_{WZ}	Write Enable to Output in High Z	—	15	—	20	—	20	—	25	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	ns

TIMING OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1,2]



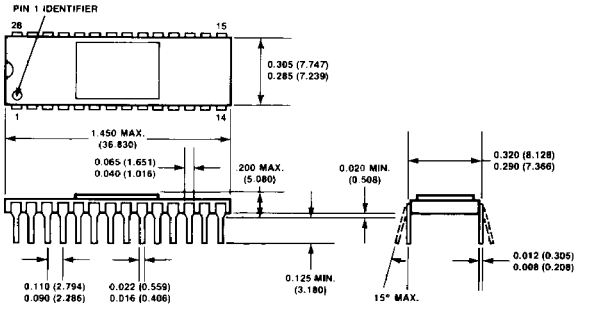
TIMING OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1,2]



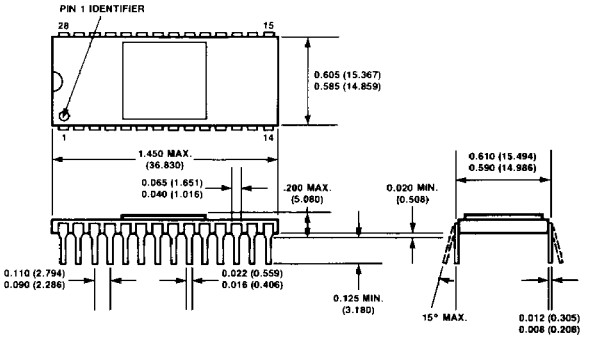
NOTES:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 1. This parameter is sampled and not 100% tested.

PACKAGE INFORMATION

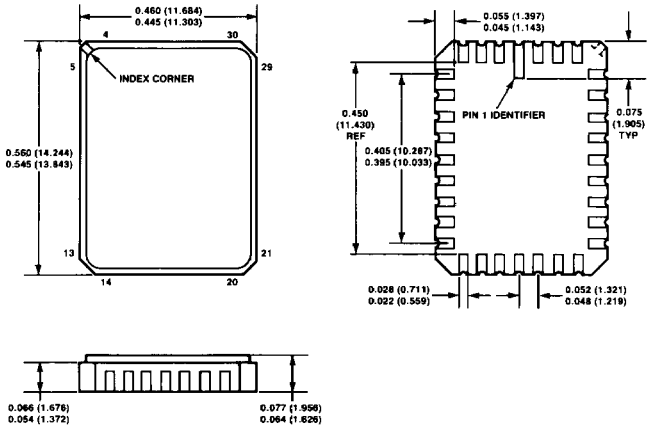
28-PIN CERAMIC SIDE-BRAZED DIP (300 MIL)



28-PIN CERAMIC SIDE-BRAZED DIP (600 MIL)



32-LEAD .450 x .550 LCC (CERAMIC LEADLESS CHIP CARRIER)



ORDERING INFORMATION

SR64K8 – 40 R M B

BURN IN	BLANK	NO ADDITIONAL BURN IN
	B	ADDITIONAL BURN IN
TEMPERATURE	BLANK	COMMERICIAL (0°C TO 70°C)
	M	MILITARY (–55°C TO +125°C)
PACKAGE	P	PLASTIC DIP
	C	SIDEBRAZED DIP
	J	PLCC (J-LEAD)
	R	CERAMIC LCC
	U	DIE
SPEED	–35 = 35ns	
	–40 = 40ns	
	–45 = 45ns	
	–55 = 55ns	
DEVICE NAME	SR64K8	

C4 = .3 pcc 24T
C6 = .6