NEC

MOS INTEGRATED CIRCUIT

MC-428000F32

8 M-WORD BY 32-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-428000F32 is a 8,388,608 words by 32 bits dynamic RAM module on which 16 pieces of 16 M DRAM: μPD4217405 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 8,388,608 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-428000F32-60	60 ns	104 ns	25 ns	5,170 mW	88 mW (CMOS level input)
MC-428000F32-70	70 ns	124 ns	30 ns	4,730 mW	

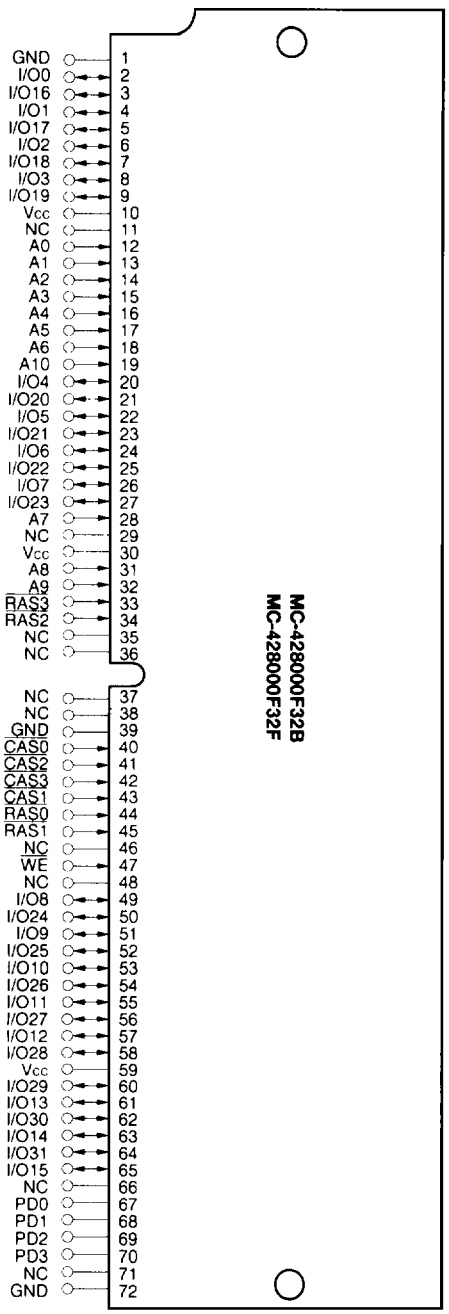
- 2,048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-428000F32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	16 pieces of μPD4217405LA (300 mil SOJ) [Double side]
MC-428000F32B-70	70 ns		
MC-428000F32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-428000F32F-70	70 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)

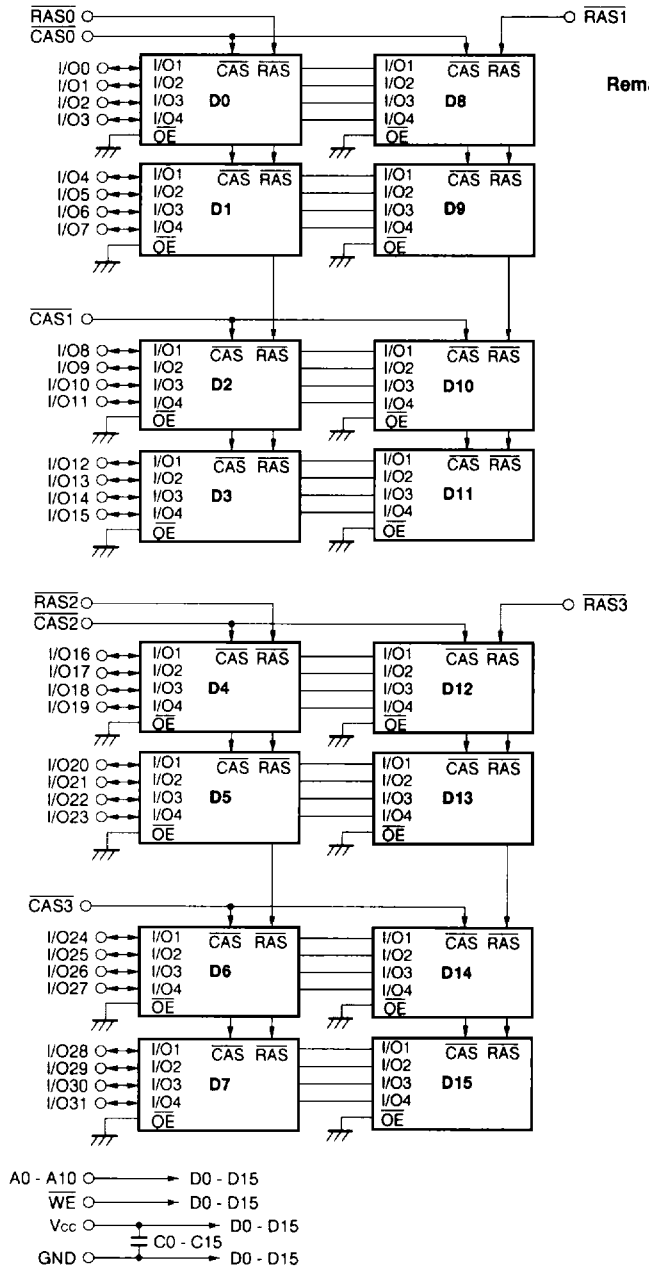


A0 - A10	:	Address Inputs
I/O0 - I/O31	:	Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	:	Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$	:	Row Address Strobe
$\overline{WE}$	:	Write Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD0	67	NC	NC
PD1	68	GND	GND
PD2	69	NC	GND
PD3	70	NC	NC

Block Diagram



Remark D0 - D15: μPD4217405

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		16	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			121	pF
	C_{I2}	$\overline{WE}$			137	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			48	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			48	
Data input/output capacitance	$C_{I/O}$	I/O0 - I/O31			29	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 60 ns		940	mA	1, 2, 3
		$t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		860		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, I_O = 0 mA			32	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			16		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH(MIN.)}$	t_{RAC} = 60 ns		940	mA	1, 2, 3 ,4
		$t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		860		
Operating current (Hyper page mode (EDO))	I_{CC4}	$\overline{RAS} \leq V_{IL(MAX.)}$, $\overline{CAS}$ Cycling	t_{RAC} = 60 ns		780	mA	1, 2, 5
		$t_{HPC} = t_{HPC(MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		700		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 60 ns		940	mA	1, 2
		$t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		860		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.

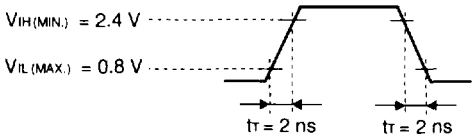
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

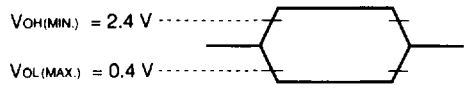
AC Characteristics (Recommended operating conditions unless otherwise noted)

AC Characteristics Test Conditions

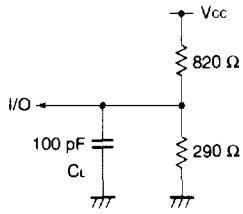
(1) Input timing specification



(2) Output timing specification



(3) Output load conditions



Common to Read, Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	104	–	124	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10,000	12	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	10	–	12	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	–	5	–	ns	2
Row Address Setup Time	t_{ASR}	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	10	–	10	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	10	–	12	–	ns	
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0	–	0	–	ns	
Transition Time (Rise and Fall)	t_T	1	50	1	50	ns	
Refresh Time	t_{REF}	–	32	–	32	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	15	–	18	ns	1
Access Time from Column Address	t_{AA}	–	30	–	35	ns	1
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	ns	2
Data-in Setup Time	t_{DS}	0	–	0	–	ns	3
Data-in Hold Time	t_{DH}	10	–	10	–	ns	3

Notes 1. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	–	35	–	40	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	–	40	–	ns	
Data Output Hold Time	t_{DHC}	5	–	5	–	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	2, 3
$\overline{WE}$ Pulse Width	t_{WPZ}	10	–	10	–	ns	3
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	2, 3
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	2, 3

Notes 1. $t_{HPC(MIN.)}$ is applied to $\overline{CAS}$ access.

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)

$\overline{WE}$: inactive

t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)

$\overline{WE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

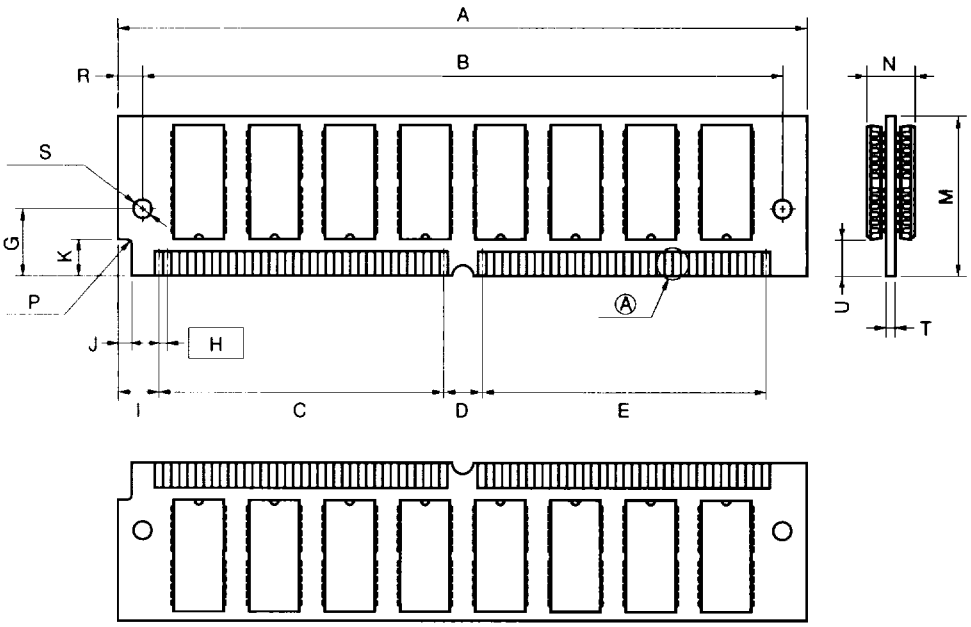
Refresh Cycle

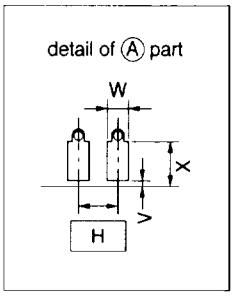
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	–	5	–	ns	
$\overline{WE}$ Setup Time	t_{WSR}	10	–	10	–	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	–	15	–	ns	

Timing Chart
Please refer to Timing Chart 8, page 457.

Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	$3.984^{+0.005}_{-0.006}$
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
R	3.38±0.13	$0.133^{+0.006}_{-0.005}$
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.5 MIN.	0.216 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A55