HSDLink Transmitter/Receiver

1. Introduction

The TSS923 Transmitter and TSS933 Receiver are point to point communications building blocks that transfer data over high speed serial links at 160 up to 400 Mbauds/s (depending on the data encoder/decoder selection).

Eight bits of user data or protocol information are loaded into the Transmitter and are encoded within the 8B10B or 8B16B mode and then serialized. Serial data is shifted out of the three differential positive ECL (PECL) serial ports at the bit rate. The bit rate is 10 times or 16 times the byte rate (depends on the encoded mode). The Receiver accepts the serial bit stream at its differential line inputs and, using an on chip PLL, recovers the serial bit rate information for a correct data retiming. The bit stream is deserialized, decoded within the 8B10B or 8B16B mode and checked for transmission errors. Recovered bytes are presented in parallel to the receiving host along with a byte rate clock. The 8B/10B or 8B/16B encoder/decoder can be disabled in systems that already encode or scramble the transmitted data. HSDLink chipset are ideal for a variety of applications where a parallel interface can be replaced with a high speed point to point serial link. Applications include,

- Interconnecting workstations
- Servers
- Mass storage
- Video transmission equipment.

2. Features

- Fibre Channel compliant
- IBM ESCON[1] compliant
- ATM compliant
- HOTLink[2] package and pinout compatible
- Case Temperature range: -55 ºC up to 125 ºC
- 190 up to 400 Mbaud/s link data rate
- TTL synchronous I/O
- 8B/10B encoded mode[3]
- 8B/16B Hamming encoded mode
- 160 up to 400 Mbaud/s link data rate (8B/16B)
- 160 up to 330 Mbaud/s link data rate (8B/10B)
- Hardened design for SEU tolerance (8B/16B)
- Bypass mode
- Built In Self Test
- Dose Rate $\geq$ 30 krad
- Triple PECL 100K serial outputs
- Dual PECL 100K serial inputs
- On-chip Phase Locked Loop
- Single +5V power supply
- 28-pin MQFPJ/LCC(*)/SOIC(*)/PLCC(*)
- 0.8µm BiCMOS (Radiation Tolerant for “E” versions)

1. ESCON is a registered trademark of IBM
2. HOTLink is a trademark of Cypress Semiconductor Corporation
3. US Patent 4,488,739 “8B/10B Partitioned Block Transmission Code” Dec 4,1984

(*) Preview

Figure 1. TSS923 Transmitter Logic Block Diagram

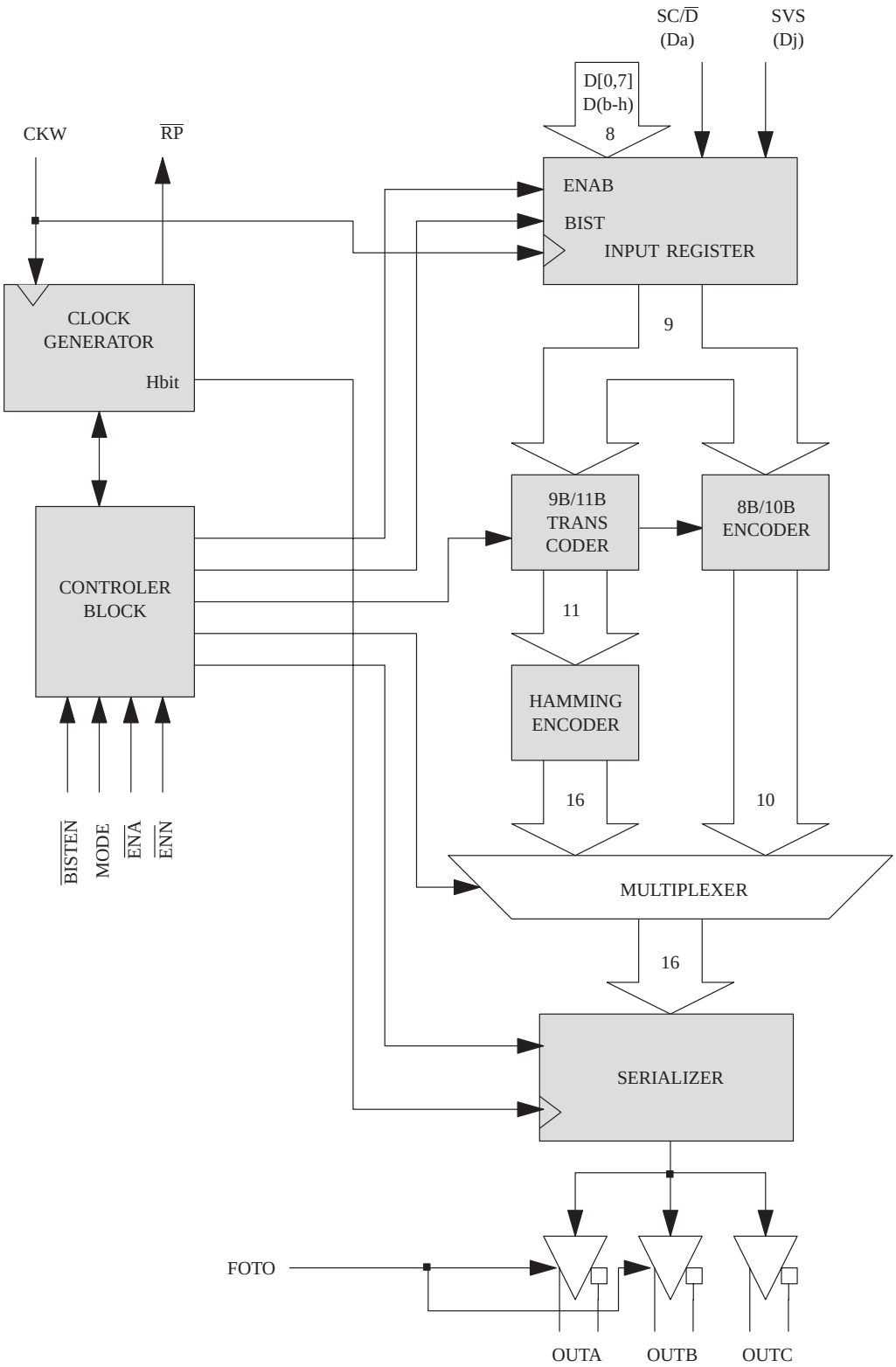


Figure 2. TSS933 Receiver Logic Block Diagram

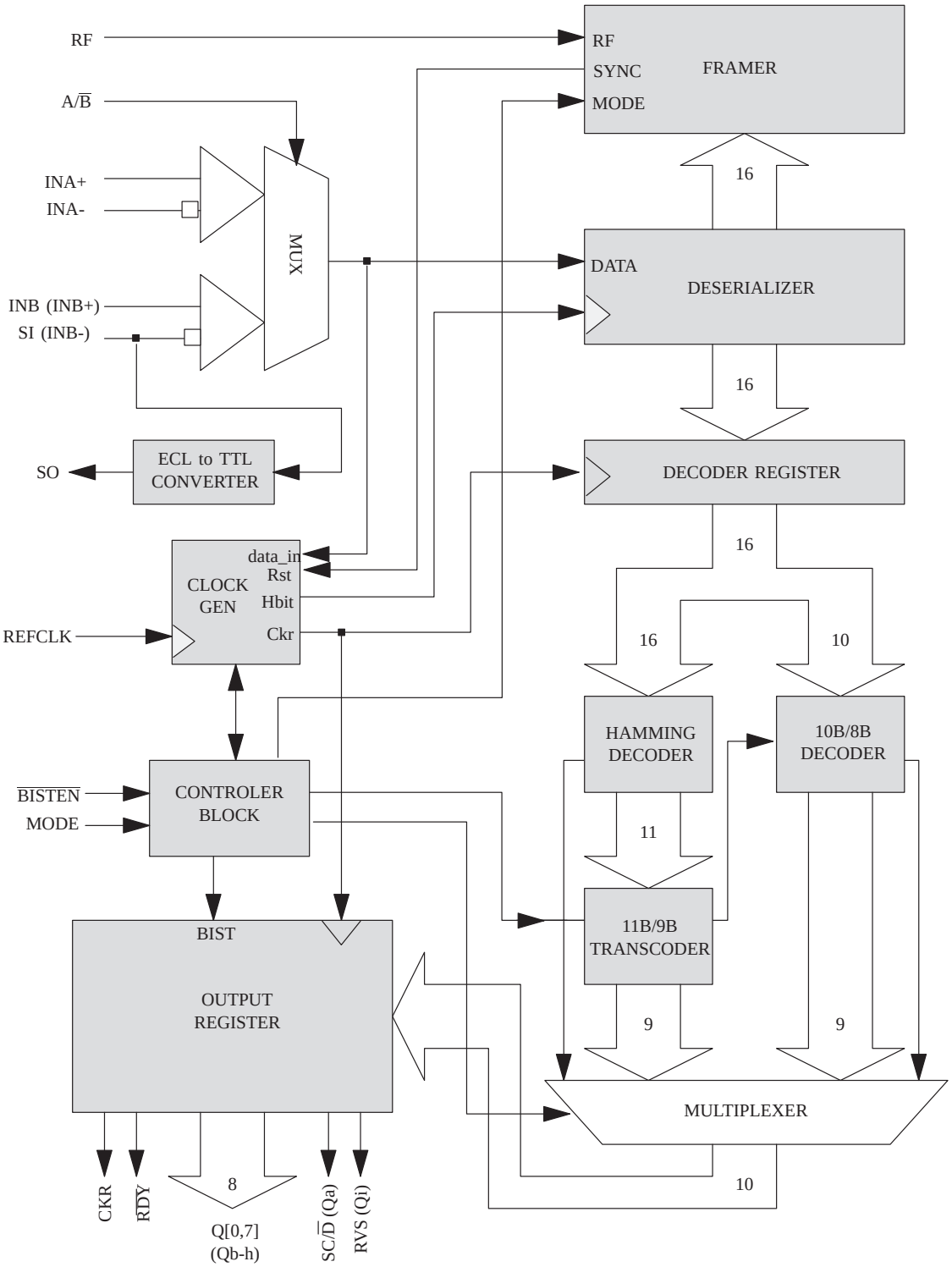
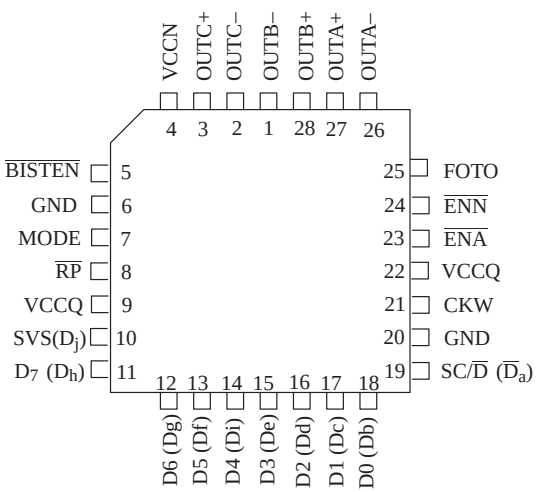


Figure 3. TSS923 Transmitter Pin Configurations

MQFPJ28/LCC28(*)/PLCC28(*)



SOIC28(*)

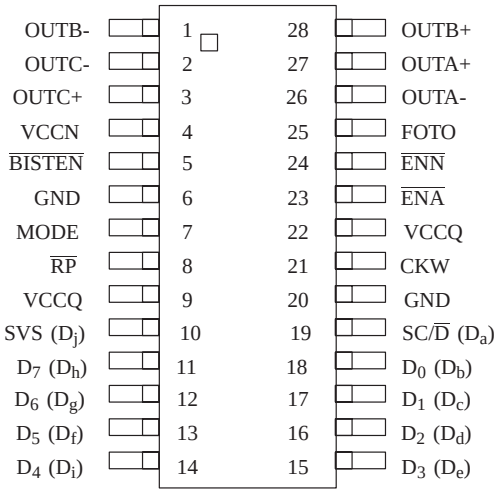
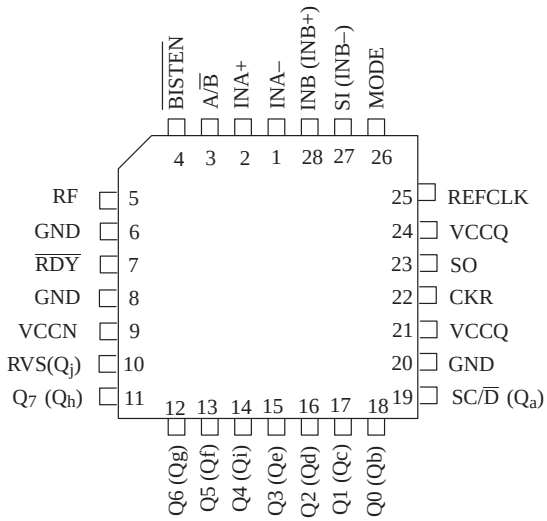
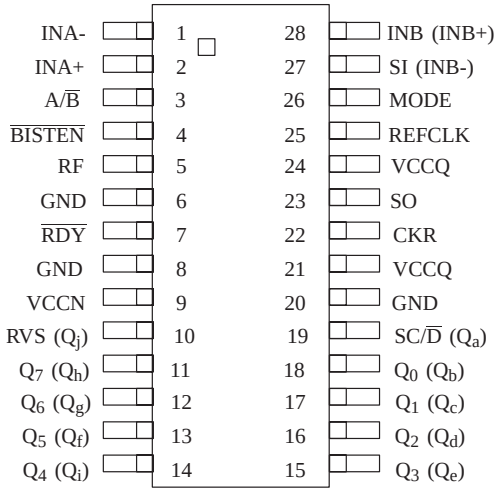


Figure 4. TSS933 Receiver Pin Configuration

MQFPJ28/LCC28(*)/PLCC28(*)



SOIC28(*)



(*) Preview

Table 1: Frequency and Data rate ranges

	8B/10B Mode	8B/16B Mode
Data Rate (Mbit/s)	128 up to 264	80 up to 200
Byte rate Clock (MHz)	16 up to 33	10 up to 25
Serial Link Data rate (Mbaud/s)	160 up to 330	160 up to 400

Table 2: TSS923 Transmitter Temperature Range & Associated Packages

Operating Range	Temperature	Package
Commercial	Ambient Temperature Range = 0 ºC up to 70 ºC	SOIC28(*)/PLCC28(*)
Industriel	Ambient Temperature Range = -40 º C up to 85 ºC	PLCC28(*)
Military	Case Temperature range = -55 ºC up to 125 ºC	MQFPJ28/LCC28(*)

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3. Transmitter Pin Description

Table 4: TSS923 Transmitter

Name	I/O	Description (valid for 8B10B or 8B16B encoding)
$D_{0..7}$ ($D_{b..h}$)	TTL In	Parallel Data Input $\overline{ENA}$=0, data are clocked into the input register on the rising edge of CKW. $\overline{ENA}$=1 and $\overline{ENN}$=0, data are clocked into the input register on the next rising edge of CKW. $\overline{ENA}$=$\overline{ENN}$=1, a SYNC character is sent. When the BYPASS mode is choosen, $D_{0..7}$ become $D_{b,c,d,e,i,f,g,h}$.
SC/$\overline{D}$ (Da)	TTL In	Special Character / Data Select SC/$\overline{D}$=1, when CKW rises causes the transmitter to encode the pattern on $D_{0..7}$ as a protocol or control code (Special Character). SC/$\overline{D}$=0, when CKW rises causes the transmitter to encode the pattern on $D_{0..7}$ as a data pattern (8B/10B or 8B/16B). When the BYPASS mode is selected, SC/$\overline{D}$ becomes D_a.
SVS (Dj)	TTL In	Send Violation Symbol SVS=1, when CKW rises, a Violation symbol is encoded and sent while the data on the parallel inputs is ignored. SVS=0, $D_{0..7}$ and SC/$\overline{D}$ are encoded. SVS pin overrides the GPA BIST, and forces the transmission of a Violation code and reset the sequence. When the BYPASS mode is selected, SVS becomes D_j.

Name	I/O	Description (valid for 8B10B or 8B16B encoding)
$\overline{ENA}$	TTL In	Enable Parallel Data $\overline{ENA}$=0, when CKW rises, the data inputs are loaded. $\overline{ENA}$=1 and $\overline{ENN}$=1, when CKW rises, the data inputs are ignored and a SYNC character is sent in order to keep the receiver synchronization.
$\overline{ENN}$	TTL In	Enable Next Parallel Data $\overline{ENA}$=1 and $\overline{ENN}$=0, data inputs are clocked into the input register on the next rising edge of CKW. $\overline{ENA}$=1 and $\overline{ENN}$=1, when CKW rises, the data inputs are ignored and a SYNC character is sent in order to keep the receiver synchronization.
CKW	TTL In	Clock Write CKW is both the clock frequency reference for the multiplying PLL that generates the high speed bit rate clock, and the byte rate write signal that synchronizes the parallel data input. CKW have to be connected to a crystal controlled time base that runs within the specified frequency range of the Transmitter and Receiver.
FOTO	TTL In	Fiber Optic Transmitter Off FOTO determines the function of two of the three PECL transmitter output pairs. FOTO='0', the data encoded will appear at the output continuously. FOTO='1', OUTA$\pm$ and OUTB$\pm$ are forced to their PECL logic zero state (OUT+='0' and OUT-=1), causing a fiber optic transmit module to extinguish its light output. OUTC$\pm$ are unaffected by the level on FOTO, and can be used as a loop-back signal source for board-level diagnostic testing.
OUTA$\pm$ OUTB$\pm$ OUTC$\pm$	PECL Out	Differential Serial Data Outputs These PECL 100K outputs (+5V referenced) are capable of driving terminated transmission lines or commercial fiber optic transmitter modules. Unused pairs of output can be wired to VCC (or left open) to reduce power consumption. OUTC$\pm$ are unaffected by the level on FOTO
MODE	3-state In	Encoder Mode Select (see below TSS923 Transmitter Control Pin Selection) "Encode 8B/16B" Mode: the data appearing on $D_{0..7}$ and SC/$\overline{D}$ are encoded using the complete Hamming code alphabet. "BYPASS 8B/16B" Mode: the word of ten bits appearing on $D_{a..j}$ is sent at the input of the Hamming encoder. "Encode 8B/10B" Mode: the data appearing on $D_{0..7}$ and SC/$\overline{D}$ are encoded using the 8B/10B data alphabet. "BYPASS 8B/10B" Mode: the word of ten bits appearing on $D_{a..j}$ is directly serialized. When MODE is left open (internal bias holds the input at VCC/2) the internal bit clock generator is disabled and OUTA+/OUTB+ become the differential bit test clock input. In typical applications MODE is wired to VCC or GND.
$\overline{BISTEN}$	3-state In	Built In Self Test Enable (see below TSS923 Transmitter Control Pin Selection) BIST Mode active,$\overline{ENA}$=$\overline{ENN}$='1': the transmitter sends an alternating 1-0 pattern. BIST Mode active,$\overline{ENA}$ or $\overline{ENN}$='0': the transmitter begins a repeating test sequence (BIST) that allow the Transmitter and Receiver to work together to test the function of the entire link. SVS pin overrides the GPA BIST, and forces the transmission of a Violation code and reset the sequence. In typical applications $\overline{BISTEN}$ is wired to VCC or GND.
$\overline{RP}$	TTL Out	Read Pulse $\overline{RP}$ is a 60% low duty-cycle byte-rate pulse train suitable for the read pulse in FIFOs. The frequency on $\overline{RP}$ is the same as CKW when enabled by $\overline{ENA}$, and duty-cycle is independent of the CKW duty-cycle. "GPA BIST" Mode: $\overline{RP}$ will remain '1' for all but the last byte of a test loop. $\overline{RP}$ will pulse '0' one byte time per BIST loop
VCCN		Power for PECL output drivers
VCCQ		Power for internal circuitry
GND		Ground

Note: TSS923 start condition
To avoid unpredictable behavior of the Transmitter during and after the power up, it's strongly recommanded to keep low ("0") and static all input signals during the ramping of the power supply. This means the power ramping have to be completed before any input signal is activated.

4. Receiver Pin Description

Table 5: TSS933 Receiver

Name	I/O	Description (valid for 8B10B or 8B16B encoding)
$Q_{0..7}$ ($Q_{b..h}$)	TTL Out	Parallel Data Output $Q_{0..7}$ contain the last received data. These outputs change synchronously with a rising edge of CKR. When the BYPASS mode is selected, $Q_{0..7}$ become $Q_{b,c,d,e,i,f,g,h}$.
SC/$\overline{D}$ (Qa)	TTL Out	Special Character / Data Select SC/$\overline{D}$ indicates the context of received data. SC/$\overline{D}$=1, the word $Q_{0..7}$ is a Control Character SC/$\overline{D}$=0, the word $Q_{0..7}$ is a Data Character When the BYPASS mode is selected, SC/$\overline{D}$ becomes Q_a.
RVS (Dj)	TTL Out	Receive Violation Symbol RVS=1 indicates that a code rule violation has been detected in the received data stream. RVS=0 indicates that no error has been detected. When the BIST mode is selected, RVS allows to check the correct functioning. When the BYPASS mode is selected, RVS becomes Q_j.
$\overline{RDY}$	TTL Out	Data Output Ready A '0' pulse on $\overline{RDY}$ indicates that new data has been received and is ready to be delivered. A missing pulse on $\overline{RDY}$ shows that a SYNC character has been received. However, the last received SYNC character of the sequence, generates a '1' pulse on $\overline{RDY}$. When RF=1, if a SYNC character has not been received then $\overline{RDY}$ is inhibited. When the BYPASS mode is selected, a pulse on $\overline{RDY}$ indicates that a SYNC character has been received When the BIST mode is selected, a '1' pulse on $\overline{RDY}$ is generated per BIST loop.
CKR	TTL Out	Clock Read This byte rate clock output is phase and frequency aligned to the incoming serial data stream. $\overline{RDY}$, Q0..7, SC/$\overline{D}$ and RVS all switch synchronously with the rising edge of this output.
A/$\overline{B}$	PECL In	Serial Data Input Select This PECL 100K (+5V referenced) input selects INA or INB as the active data input. A/$\overline{B}$='1', INA is connected to the shifter and signals connected to INA will be decoded. A/$\overline{B}$='0', INB is selected. If left open, A/$\overline{B}$ is internally grounded
INA$\pm$	Diff In	Serial Data Differential Input A The differential signal at the receiver end of the communication link may be connected to the differential input pairs INA$\pm$ or INB$\pm$. Either the INA or INB pair can be used as the main data input and the other can be used as a loopback channel or as an alternative data input selected by the state of A/$\overline{B}$. If left open, INA$\pm$ are internally biased at approximately 2V which acts as a low input ECL voltage.
INB (INB+)	PECL In (Diff In)	Serial Data Input B This pin is either a single-ended PECL data receiver (INB) or half of the INB of the differential pair. If SO='1', then INB$\pm$ can be used as differential line receiver interchangeably with INA$\pm$. If SO is normally connected and loaded, INB becomes a single-ended PECL 100K (+5V referenced) serial data input. INB is used as the test bit clock while in Test H mode. If left open, INB+ is internally biased at approximately 2V which acts as a low input ECL voltage.
SI (INB-)	PECL In (Diff In)	Status Input This pin is either a single-ended PECL status monitor input (SI) or half of the INB of the differential pair. If SO='1', then INB$\pm$ can be used as differential line receiver interchangeably with INA$\pm$. If SO is normally connected and loaded, SI becomes a single-ended PECL 100K (+5V referenced) status monitor input, which is converted into a TTL level signal at the SO output pin. If left open, SI is internally biased at approximately 2V which acts as a low input ECL voltage
SO	TTL Out	Status Output SO is the TTL converted output of SI. It's typically used to translate the Carrier Detect output from a fiber optic receiver connected to SI. When SO is normally connected and loaded (without any external and single pull-up resistor), SO will assume the same logical level as SI and INB will become a single ended PECL serial data input. If the status monitor translation isn't desired, then SO may be wired to VCC and the INB$\pm$ pair may be used as a differential serial data input.

Name	I/O	Description (valid for 8B10B or 8B16B encoding)
RF	TTL In	Reframe Enable RF controls the Framer logic in the Receiver. If RF='1', each SYNC word detected will frame the data that follows. If RF is '1' for greater than 2048 consecutive bytes, the internal logic switches to double-byte mode. When RF='0', the reframing logic is disabled. The incoming data stream is then continuously deserialized and decoded using byte boundaries set by the internal byte counter. Bit errors in the data stream will not cause alias SYNC character to reframe the data erroneously.
REFCLK	TTL In	Reference Clock REFCLK is the clock frequency reference for the clock/data synchronizing PLL. REFCLK sets the approximate center frequency for the internal PLL to track the incoming bit stream. REFCLK have to be connected to a crystal-controlled time base that runs within the frequency limits of the Tx/Rx pair, and the frequency have to be the same as the transmitter CKW frequency (within CKW$\pm$0.1%)
MODE	3-state In	Decoder Mode Select (see below TSS933 Receiver Control Pin Selection) "Decode 8B/16B" Mode: the complete Hamming code alphabet is selected. "BYPASS 8B/16B" Mode: registered shifter contents bypass the decoder and are sent directly on $Q_{a..j}$ outputs. "Decode 8B/10B" Mode: the 10B/8B decoder is selected. "BYPASS 8B/10B" Mode: registered shifter contents bypass the decoder and are sent directly on $Q_{a..j}$ outputs. When MODE is left open (internal bias holds the input at VCC/2) the internal bit clock generator is disabled and INB becomes the bit rate test clock input. In typical applications MODE is wired to VCC or GND.
$\overline{\text{BISTEN}}$	3-state In	Built In Self Test Enable (see below TSS933 Receiver Control Pin Selection) When BIST mode is active, the Receiver awaits a D0.0 character (sent once per BIST loop) and begins a continuous test sequence that tests the functionality of the Transmitter, the Receiver, and the link connected them. The status of the test is then monitored with $\overline{\text{RDY}}$ and RVS outputs. In typical applications $\overline{\text{BISTEN}}$ is wired to VCC or GND.
VCCN		Power for PECL output drivers
VCCQ		Power for internal circuitry
GND		Ground

Note: TSS933 start condition
To avoid unpredictable behavior of the Receiver during and after the power up, it's strongly recommanded to keep low ("0") and static all input signals during the ramping of the power supply. This means the power ramping have to be completed before any input signal is activated.

5. TSS923 Transmitter Control Pin Selection

Table 6: Tx Control Pin Selection

MODE	$\overline{\text{BISTEN}}$	(ENA + ENN)	Mode Selection
0	0	X	8B/16B Encoder
	Left Open	0	PBIST 8B/16B
		1	GPA 8B/16B
	1	X	8B/10B Encoder
Left Open	0	X	Test H + 8B/16B Encoder
	Left Open	0	Test H + PBIST 8B/10B
		1	Test H + GPA 8B/10B
	1	X	Test H + 8B/10B Encoder
1	0	X	Bypass 8B/16B
	Left Open	0	PBIST 8B/10B
		1	GPA 8B/10B
	1	X	Bypass 8B/10B

6. TSS933 Receiver Control Pin Selection

Table 7: Rx Control Pin Selection

MODE	$\overline{\text{BISTEN}}$	Mode Selection
0	0	8B/16B Decoder
	Left Open	GPA 8B/16B
	1	8B/10B Decoder
Left Open	0	Test H + 8B/16B Decoder
	Left Open	Test H + GPA 8B/10B
	1	Test H + 8B/10B Decoder
1	0	Bypass 8B/16B
	Left Open	GPA 8B/10B
	1	Bypass 8B/10B

Note:
- GPA means the GPA Mode of the BIST selection. All Test Mode are selected when the Control Input pins are left open (grey space).

7. TSS923 Transmitter Block Diagram Description

The Transmitter circuit is built with several blocks: Input register, 9B/11B transcoder, Hamming encoder, 8B/10B encoder, Serial shifter, Three serial output ports, Clock generator and finally a Controller block.

7.1. Input Register

7.1.1.Normal Mode

The Input register holds the data to be processed by the transmitter and allows the input timing to be made with synchronous or asynchronous FIFOs. The input register is clocked by CKW and loaded with information on the $D_{0..7}$, SC/$\overline{D}$, and SVS pins. Two enable inputs ($\overline{ENN}$ and $\overline{ENA}$) allow the user to choose when data is loaded in the register.

$\overline{ENA}$=0, data are clocked into the input register on the rising edge of CKW.

$\overline{ENA}$=1 and $\overline{ENN}$=0, data are clocked into the input register on the next rising edge of CKW.

$\overline{ENA}$=$\overline{ENN}$=1, a SYNC character is sent.

When the BYPASS mode is choosen, $D_{0..7}$ become $D_{b,c,d,e,i,f,g,h}$.

SC/$\overline{D}$=1, when CKW rises causes the transmitter to encode the pattern on $D_{0..7}$ as a protocol or control code (Special Character).

SC/$\overline{D}$=0, when CKW rises causes the transmitter to encode the pattern on $D_{0..7}$ as a data pattern (8B/10B or 8B/16B).

7.1.2. BIST Mode

The input register does not take into account the data appearing at the Transmitter input, and runs in GPA of 9 bits. During this mode, only SVS input is active.

7.2. 9B/11B Transcoder

The transcoder and its associated Hamming encoder transform the input data held by the Input register into a form more suitable for transmission into on a serial interface link. The transcoder processes D0..7 and SC/D and creates an 11-bit wide word. This word is encoded in the Hamming encoder block and then transformed in a 16-bit wide word which presents the following characteristics:

- The maximum run lenght of the output serial data stream is equal to four consecutive ’1’ (or ’0’)

- For each generated word, the disparity is null (low DC spectral component)

In BYPASS Mode, the transcoder is disabled.

7.3. HAMMING Encoder

The encoder transforms the data coming from the 9B/11B Transcoder to 15-bit wide word. This 15-bit wide word allow the correction of 1 error and the detection of 2 errors. A sixteen bit is then added in order to keep null the total word disparity. The principle used is based on a Hamming encoding function. Main advantages of the encoder are its ability to detect and correct 1 error for every generated word and to detect also 2 errors for every generated word. In addition the maximum run length is kept less than four, and all generated word exhibit a null disparity. However, the available data rate becomes lower comparing to other encoder technics and is equal to half the bit rate clock.

In BYPASS Mode, this encoder is directly used from the circuit inputs. In that case, an eleven bit is added and it represents the complemented tenth bit.

7.4. 8B/10B Encoder

This other encoder transforms also the input data held by the Input register into a form more suitable for transmission on a serial interface link. Only the code used is different. This code is specified by ANSI X3.230 (Fibre Channel) and the IBM ESCON channel (US Patent 4,488,739 ”8B/10B Partitioned Block Transmission Code” Dec 4,1984).

The 8B/10B coding function of the Encoder can be bypassed for systems that include an external coder or scrambler function.

7.5. Serial Shifter

The Shifter accepts parallel data from the Encoder once each byte time shifts it to the serial interface output buffers using a PLL multiplied bit clock that runs at ten or sixteen times the byte rate clock. Timing for the parallel transfer is controlled by an internal counter and is not affected by signal levels or timing at the input pins.

7.6. OutA, OutB, OutC

The serial interface PECL output buffers (ECL100K referenced to +5V) are the drivers for the serial media. They are all connected to the Shifter and contain the same serial data. Two of the output pairs (OUTA± and OUTB±) are controllable by the FOTO input and can be disabled to force a logical zero (ie, "light off") at the outputs. The third output pair (OUTC±) is not affected by FOTO and will supply a continuous data stream suitable for loop-back testing of the subsystem. In wire-based systems, control of the outputs may not be required, and FOTO can be strapped at '0' level. The three outputs are intended to add system and architectural flexibility by offering identical serial bit stream with separate interfaces for redundant connections or for multiple destinations. Unneeded outputs can be wired to VCC to disable and power down the unused output circuitry.

7.7. Clock Generator

The clock generator is an embedded Phase Locked Loop that takes a byte rate reference clock (CKW) and multiplies it by ten or sixteen to create the bit rate clock for driving the serial shifter. The byte rate reference comes from CKW, the rising edge of which clocks data into the Input register. This clock have to be a crystal referenced pulse stream that has a frequency between the minimum and maximum specified for the Transmitter/Receiver pair. Signals controlled by this block form the bit clock and the timing signals that control internal data transfers between the Input register and the serial shifter.

The Read Pulse $\overline{RP}$ is derived from the internal counter used. It is a byte-rate pulse stream with the proper phase and pulse width to allow transfer of data from an asynchronous FIFO. Pulse width is independant of CKW duty cycle, since proper phase and duty cycle is maintained by the PLL. The $\overline{RP}$ pulse stream will insure correct data transfers between asynchronous FIFOs and the transmitter input latch with no external logic.

7.8. Controller Block

The Controller Block includes the initialization and control for the BIST generator, the Test mode clock distribution and the control logic to properly select the data encoding.

7.8.1. Normal Mode (Encoding)

When the byte rate clock CKW rises and if no data are loaded ($\overline{ENA}$=$\overline{ENN}$='1'), the encoder will send a SYNC character allowing to keep the synchronization. SVS input forces the transmission of a Violation code.

In the 8B/10B mode, data that appear on $D_{0..7}$ and SC/$\overline{D}$ inputs are encoded. In the 8B/16B mode, data that appear on $D_{0..7}$ and SC/$\overline{D}$ inputs are encoded (Hamming code).

7.8.2. BYPASS Mode

When the byte rate clock CKW rises and if no data are loaded ($\overline{ENA}$=$\overline{ENN}$='1'), the encoder will send a SYNC character allowing to keep the synchronization. BIST mode and TEST H mode override the BYPASS mode and switch the circuit in an encoding mode.

When the 8B/10B mode is selected, the 8B/16B encoder is disabled. The serializer receives directly ten bits corresponding to the following inputs:

- $D_{b,c,d,e,i,f,g,h}$ equivalent to $D_{0..7}$
- D_a equivalent to SC/$\overline{D}$
- D_j equivalent to SVS

The letters a,b,c,d,e,i,f,g,h,j correspond to the denomination used in the official 8B/10B protocol (see US Patent 4,488,739 "8B/10B Partitioned Block Transmission Code Dec 4,1984)

When the 8B/16B mode is selected, the 9B/11B transcoder is disabled and the Hamming encoder receives directly the following inputs:

- $D_{b,c,d,e,i,f,g,h}$ equivalent to $D_{0..7}$
- D_a equivalent to SC/D
- D_j equivalent to SVS

- D_k equivalent to $\overline{D_j}$

In that case, the letters a,b,c,d,e,i,f,g,h,j have no special denomination and the word 'abcdeifghj' is presented at the input of the Hamming encoder (bit 'a' is the Most Significant Bit).

7.8.3. Test BIST Mode

When $\overline{ENN}$=$\overline{ENA}$='1', the transmitter sends an alternating 1-0 serial data output which correspond to the maximum frequency on the link.

When $\overline{ENN}$ or $\overline{ENA}$='0', the transmitter generates a pseudo random cyclic sequence of 511 9-bit-wide-words. Then the Receiver can check and compare the received data to its own BIST generator which runs synchronously with the BIST generator of the Transmitter. In that configuration, the signal $\overline{RP}$ is pulsed at '0' level one time per BIST loop. The 511 word sequence distributes all the Data characters, Control and Protocol characters, and invalid characters. SVS input overrides the BIST mode and forces the transmission of a Violation code and resets the BIST sequence.

7.8.4. TEST H Mode

When the TEST H mode is selected, the internal bit rate clock is disabled and replaced by an external bit rate clock through the OUTA+ and OUTB+ pins.

8. TSS933 Receiver Block Diagram Description

The Receiver circuit is built with several blocks: Serial Data Inputs, PECL-TTL convertor, Clock Synchronization, Framer, Shifter, Decode Register, Decoder, Output Register and finally a Controller block.

8.1. Serial Data Inputs

Two pairs of differential line receivers are the inputs for the serial data stream. INA$\pm$ or INB$\pm$ can be selected with the A/$\overline{B}$ input. INA$\pm$ is selected with A/$\overline{B}$='1' and INB$\pm$ is selected with A/$\overline{B}$='0'. The threshold of A/B is compatible with the ECL 100K signals from PECL fiber optic interface modules. The differential threshold of INA+ and INB+ will accomodate wire interconnect with filtering losses or transmission line attenuation greater than 20dB (Vdiff > 50mV) or can be directly connected to fiber optic interface modules (any ECL logic family, not limited to ECL 100K). The common mode voltage tolerance will also accomodate a wide range of signal termination voltage (from GND +2.0V up to VCC).

8.2. PECL-TTL Converter

The function of the INB(INB+) input and the SI(INB-) input is defined by the connections on the SO output pin. If the PECL/TTL converter function is not required, the SO output is wired to VCC. If the converter is required, the SO output have to be connected to a normal TTL load (without any pull-up resistor) and the INB+ input becomes INB (single-ended, ECL 100K serial data input) and the INB- input becomes SI (single-ended, ECL 100K status input).

This positive-referenced PECL to TTL converter is provided to eliminate external logic between a PECL fiber-optic interface module "carrier detect" output and the TTL input in the control logic. The input threshold is compatible with ECL 100K levels (+5V referenced). It can also be used as part of the link status indication logic for wire connected systems.

8.3. Clock Synchronization

The Clock Synchronization function is performed by an embedded Phase Locked Loop that tracks the frequency of the incoming bit stream and aligns the phase of its internal bit rate clock to the serial data transitions. This block contains the logic to transfer the data from the Shifter to the Decode register once every word. The counter that controls this transfer is initialized by the Framer logic. CKR is a buffered output derived from the bit counter used to control the Decode register and the output register transfers.

Reframing may stretch the period of CKR by up to 90%, and either CKR pulse width high or pulse width low may be stretched, depending on when reframe occurs.

The REFCLK input provides a byte-rate reference frequency to improve PLL acquisition time and limit

unlocked frequency excursion of the CKR when no data is present at the serial inputs. The frequency of REFCLK is required to be within ±0.1% of the frequency of the clock that drives the transmitter CKW pins.

8.4. Framer

Framer logic checks the incoming bit stream for the pattern that defines the byte boundaries. This combinatorial logic filter looks for the X3.230 symbol defined as a Special Character Comma (K28.5 for the 8B/10B encoder). When the SYNC character is found, the internal free-running bit counter is synchronously reset to its initial state, thus framing the data correctly on the correct byte boundaries.

Random errors that occur in the serial data can corrupt some data patterns into a bit pattern identical to a SYNC character, and thus cause an erroneous data framing error. The RF input prevents this by inhibiting reframing during times when normal message data is present.

If RF='1', each SYNC word detected will frame the data that follows.

If RF is '1' for greater than 2048 consecutive bytes, the internal logic switches to double-byte mode. Double-byte framing greatly reduces the possibility of erroneously reframing to an aliased SYNC character.

When RF='0', the reframing logic is disabled. The incoming data stream is then continuously deserialized and decoded using byte boundaries set by the internal byte counter. Bit errors in the data stream will not cause alias SYNC character to reframe the data erroneously.

In the particular 8B/10B mode and when RF='1', it is also possible that an error could cause misframing, after which all data will be corrupted. Likewise, a K28.7 followed by D11.x, D20.x, or an SVS (C0.7) followed by D11.x will create alias K28.5 characters and cause erroneous framing. These sequences must be avoided while RF='1'.

8.5. Shifter

The Shifter accepts serial inputs from the Serial Data inputs one bit at a time, as clocked by the Clock Synchronisation logic block. Data is transferred to the Framer on each bit, and to the Decode register once per word.

8.6. Decode Register

The 16-bit parallel register is loaded by the deserializer at the word frequency. In the 8B/10B mode, only 10 bits are used. It is presented to the Decoder and held until it is transferred to the output latch.

8.7. HAMMING Corrective Decoder

The corrective decoder transforms the 16-bit wide word that appears at the output of the Decode Register in an 11-bit wide word. The decoding and the error detection is made by using the "syndrome" bits technic. In addition, a parity and disparity verification is made on every word. This allow to correct one error and to signal out two errors.

When the 8B/16B mode is selective (in BYPASS mode or not) the Decoder is always active.

8.8. 11B/9B Transcoder

The 11-bit Data that are coming from the corrective Hamming decoder are transformed in Data or Control character: an 8-bit wide word $Q_{0..7}$ and a state bit on SC/$\overline{D}$ output.

If SC/$\overline{D}$='1', $Q_{0..7}$ is a Control Character, if SC/$\overline{D}$='0', $Q_{0..7}$ is a Data character.

The use of this Transcoder is directly due to the code used in the Transmitter in the 8B/16B mode.

When the BYPASS mode is selected, the transcoder function is disabled and the 10-bit wide word that appears at the output of the Hamming decoder is directly sent to the $Q_{a..j}$ outputs.

8.9. 10B/8B Decoder

Parallel data are transformed from ANSI-specified X3.230 (Fibre Channel) 8B/10B codes back to "raw data" in the Decoder. This block uses the standard decoder patterns shown in the Valid Data Character and Valid Special Character Codes document(See US Patent 4,488,739 "8B/10B Partitioned Block Transmission Code" Dec 4,1984). Data patterns are signaled by a '0' on the SC/$\overline{D}$ output and Special Character are signaled by a '1' on the SC/$\overline{D}$ output. Unused patterns or disparity errors are signaled as errors by a '1' on the RVS output and by specific Special Character codes. In the BYPASS mode, this decoder is not used.

8.10. Output Register

The Output register holds the recovered data ($Q_{0..7}$, SC/$\overline{D}$ and RVS) and aligns it with the recovered byte clock (CKR). This synchronization insures proper timing to match a FIFO interface or other logic that requires glitch free and specified output behavior. Outputs change synchronously with the rising edge of CKR.

When the BIST mode is selected, the Output register is transformed in 9-bit GPA and it presents the BIST sequence at the $Q_{0..7}$ and SC/$\overline{D}$ outputs.

8.11. Controller Block

The Controller Block includes the initialization and control for the BIST generator, the Test mode clock distribution and the control logic to properly select the data decoding.

8.11.1. Normal Mode (Encoding)

In the 8B/10B mode, the decoder circuit decodes the received word on the $Q_{0..7}$ and SC/$\overline{D}$ outputs.

In the 8B/16B mode, the Hamming decoder decodes the received word on the $Q_{0..7}$ and SC/$\overline{D}$ outputs.

8.11.2. BYPASS Mode

BIST mode and TEST H mode override the BYPASS mode and switch the circuit in decoding mode.

In the 8B/10B mode, the 10B/8B decoder is disabled. The Output Register receives directly the 10 received bits:

$Q_{b,c,d,e,i,f,g,h}$ equivalent to $Q_{0..7}$

Q_a equivalent to SC/$\overline{D}$

Q_j equivalent to RVS

The letters a,b,c,d,e,i,f,g,h,j correspond to the denomination used in the official 8B/10B protocol (see US Patent 4,488,739 ”8B/10B Partitioned Block Transmission Code Dec 4,1984)

In the 8B/16B mode, the 11B/9B Transcoder is disabled and the Output Register receives directly the 10 bits that are coming from the Hamming corrective decoder (the eleventh bit represents the complement of the tenth bit):

$Q_{b,c,d,e,i,f,g,h}$ equivalent to $Q_{0..7}$

Q_a equivalent to SC/$\overline{D}$

Q_j equivalent to RVS

In that case, the letters a,b,c,d,e,i,f,g,h,j have no special denomination and the word ’abcdeifghj’ is presented at the input of the Hamming encoder (bit ’a’ is the Most Significant Bit).

8.11.3. Test BIST Mode

In that configuration, the Transmitter is also supposed to be in its own BIST mode. Thus, the Receiver is supposed to receive a cyclic word sequence. The initialisation character of this sequence is the D0.0 character:

The Receiver awaits for the D0.0 character which is sent one time per BIST loop ($\overline{RDY}$ is pulsed at ’1’ level). When the D0.0 character is detected, $\overline{RDY}$ is pulsed at level ’0’ and an internal generator synchronises the Receiver sequence with the Transmitter sequence. Then each received word is compared with the homonyme word of the internal generator. When the RVS output is pulsed at ’1’ level then a difference has been detected. $\overline{RDY}$ is pulsed at ’1’ level one time per BIST loop.

In that mode, the $Q_{0..7}$, RVS and SC/$\overline{D}$ do not give any information on the received data, but only on the state of the current Test. Word data that have been generated are available on the Output Register ($Q_{0..7}$). The initial function of RVS is also inhibited.

8.11.4. TEST H Mode

When the TEST H mode is selected, the internal bit rate clock is disabled and replaced by an external bit rate clock through the INB+ input.

9. TSS933 Preliminary Electrical Characteristics

Parameter	Description	Test conditions	Min	Max	Unit
TTL-Compatible OUT pins = Transmitter ($\overline{RP}$) / Receiver (Q0..7, SC/D, RVS, RDY, CKR, SO) TTL-Compatible IN pins = Transmitter (D0..7, SC/D, SVS, ENA, ENN, CKW, FOTO) / Receiver (RF, REFCLK)					
V_{OHT}	Output high voltage	I_{OH} = -10mA	2.4	-	V
V_{OLT}	Output low voltage	I_{OL} = 10mA	-	0.4	V
V_{IHT}	Input high voltage		2.0	Vcc	V
V_{ILT}	Input low voltage		-0.5	0.8	V
I_{IHT}	Input high current	V_{IN} = Vcc	-	10	uA
I_{ILT}	Input low current	V_{IN} = 0v	-10	-	uA
Tri-State pins = Transmitter ($\overline{BISTEN}$, MODE) / Receiver ($\overline{BISTEN}$, MODE)					
V_{IHT}	Input high voltage		Vcc-0.77	Vcc	V
V_{ILT}	Input low voltage		-0.5	0.52	V
V_{INM}	Open-input noise margin	V_{IN} = open	1.0	-	V
I_{ILT}	Input high current	V_{IN} = Vcc	-	100	uA
I_{ILT}	Input low current	V_{IN} = 0v	-100		uA
Receiver single PECL-Compatible input pins: (A/$\overline{B}$, SI, INB)					
V_{IHE}	Input high voltage		Vcc-1.10	Vcc	V
V_{ILE}	Input low voltage		2.0	Vcc-1.44	V
$I_{IHE}^{(1)}$	Input high current	V_{IN} = V_{IHE} Max.	-	500	uA
$I_{ILE}^{(1)}$	Input low current	V_{IN} = V_{ILE} Min.	+0.5	-	uA
Receiver differencial PECL-Compatible input pins: (INA±, INB±)					
V_{DIFF}	Input differential voltage		50	-	mV
V_{IHH}	Highest input high voltage		-	Vcc	V
V_{ILL}	Lowest input low voltage		2.0	-	V
I_{IHH}	Input high current	V_{IN} = V_{IHH} Max.	-	750	uA
$I_{ILL}^{(2)}$	Input low current	V_{IN} = V_{ILL} Min.	-200	-	uA
Transmitter PECL-Compatible output pins: (OUTA±, OUTB±, OUTC±)					
V_{OHE}	Output high voltage	Load=50Ω to Vcc-2v	Vcc-1.23	Vcc-0.87	V
V_{OLE}	Output low voltage	Load=50Ω to Vcc-2v	Vcc-1.95	Vcc-1.56	V
V_{ODIF}	Output differential voltage	Load=50Ω to Vcc-2v	0.61	-	V

Note:
1. Applies to A/$\overline{B}$ only
2. Input currents are always positive at all voltages above Vcc/2

10. Maximum Ratings

Storage Temperature: -60 ºC to + 150 ºC

Supply Voltage to Ground Potential: -0.5V to +6.5V

DC Input Voltage: -0.5V to 6.5V

Static Discharge Voltage: > 2001V

11. TSS923/TSS933 Preliminary Power Consumption

Transmitter Typical Power Consumption Configuration VCC=+5V, 25 °C					
Power Supply Type	Description & Test Conditions		Typ	Max	Unit
P[Total]_10B	Total Power Supply (example 1) • 8B10B Mode / 33MHz • TTL load=30pf • 1 PECL output used • PECL load=50Ω to Vcc-2v		470		mW
P[Total]_16B	Total Power Supply (example 2) • 8B16B Mode / 25MHz • TTL load=30pf • 1 PECL output used • PECL load=50Ω to Vcc-2v		440	-	mW
Receiver Typical Power Consumption Configuration VCC=+5V, 25 °C					
Power Supply Type	Description & Test Conditions		Typ	Max	Unit
P[Total]_10B_0	Total Power Supply (example 1) • 8B10B Mode / 33MHz • TTL load=30pf • RF='0'		700	-	mW
P[Total]_10B_1	Total Power Supply (example 2) • 8B10B Mode / 33MHz • TTL load=30pf • RF='1'		750	-	mW
P[Total]_16B_0	Total Power Supply (example 3) • 8B16B Mode / 25MHz • TTL load=30pf • RF='0'		730	-	mW
P[Total]_16B_1	Total Power Supply (example 4) • 8B16B Mode / 25MHz • TTL load=30pf • RF='1'		780	-	mW

12. Preliminary TSS923 Transmitter Switching Characteristics

Parameter	Description	Encoder Mode	Min	Max	Unit
t_{CKW}	Write Clock Cycle	8B/10B	30.3	62.5	ns
		8B/16B	40	100	
t_B	Bit Time	8B/10B	3.03	6.25	ns
		8B/16B	2.50	6.25	ns
t_{CPWH}	CKW Pulse Width HIGH	-	5		ns
t_{CPWL}	CKW Pulse Width LOW	-	5		ns
t_{SD}	Data Set-Up Time	-	tbd		ns
t_{HD}	Data Hold Time	-	0		ns
t_{SENP}	$\overline{ENA}$ Set-Up Time	8B/10B	$6t_B + 8$	$10t_B$	ns
		8B/16B	$10t_B + 8$	$16t_B$	bs
t_{HENP}	$\overline{ENA}$ Hold Time	-	0		ns
t_{PDR}	Read Pulse Rise Alignment / CKW	-	4	15	ns
t_{PPWH}	Read Pulse HIGH	8B/10B	$4t_B - 3$		ns
		8B/16B	$6t_B - 3$		ns
t_{PDF}	Read Pulse Fall Alignment / CKW	8B/10B	$6t_B - 3$		ns
		8B/16B	$10t_B - 3$		ns
t_{RISE}	PECL Output Rise Time (20%-80%)	-		tbd	ns
t_{FALL}	PECL Output Fall Time (20%-80%)	-		tbd	ns

13. Preliminary TSS933 Receiver Switching Characteristics

Parameter	Description	Encoder Mode	Min	Max	Unit
t_{CKR}	Read Clock Pulse (No Serial Data Input), REFCLK as reference)	8B/10B	-1	+1	%
		8B/16B	-1	+1	
t_B	Bit Time	8B/10B	3.03	6.25	ns
		8B/16B	2.50	6.25	ns
t_{CPRH}	Read Clock Pulse HIGH	8B/10B	$5t_B$ - 3		ns
		8B/16B	$8t_B$ - 3		ns
t_{CPRL}	Read Clock Pulse LOW	8B/10B	$5t_B$ - 3		ns
		8B/16B	$8t_B$ - 3		ns
t_{RH}	$\overline{RDY}$ Hold Time	-	t_B - 3		ns
t_{PRF}	$\overline{RDY}$ Pulse Fall to CKR Rise	8B/10B	$5t_B$ - 3		ns
		8B/16B	$8t_B$ - 3		ns
t_{PRH}	$\overline{RDY}$ Pulse Width HIGH	8B/10B	$4t_B$ - 3		ns
		8B/16B	$7t_B$ - 3		ns
t_A	Data Access Time (1, 2)	-	$2t_B$ + 2	$2t_B$ + 5	ns
t_H	Data Hold Time from CKR rise (1, 2)	-	$2t_B$ - 3		ns
t_{ROH}	Data Hold Time (1, 2)	-	t_B - 3		ns
t_{CKX}	REFCLK Clock Period Referenced to CKW of Transmitter	-	-0.1	+0.1	%
t_{CPXH}	REFCLK Clock Pulse HIGH	-	5		ns
t_{CPXL}	REFCLK Clock Pulse LOW	-	5		ns
t_{DS}	Propagation Delay SI to SO	-		tbd	ns

Notes :
1. Data includes Q_{0-7}, SC/$\overline{D}$ and RVS.
2. t_A, t_H and t_{ROH} specifications are only valid if all outputs (CKR, $\overline{RDY}$, Q_{0-7}, SC/$\overline{D}$ and RVS) are loaded with similar DC and AC loads.

Figure 5. Preliminary Switching Waveforms for the TSS923 Transmitter

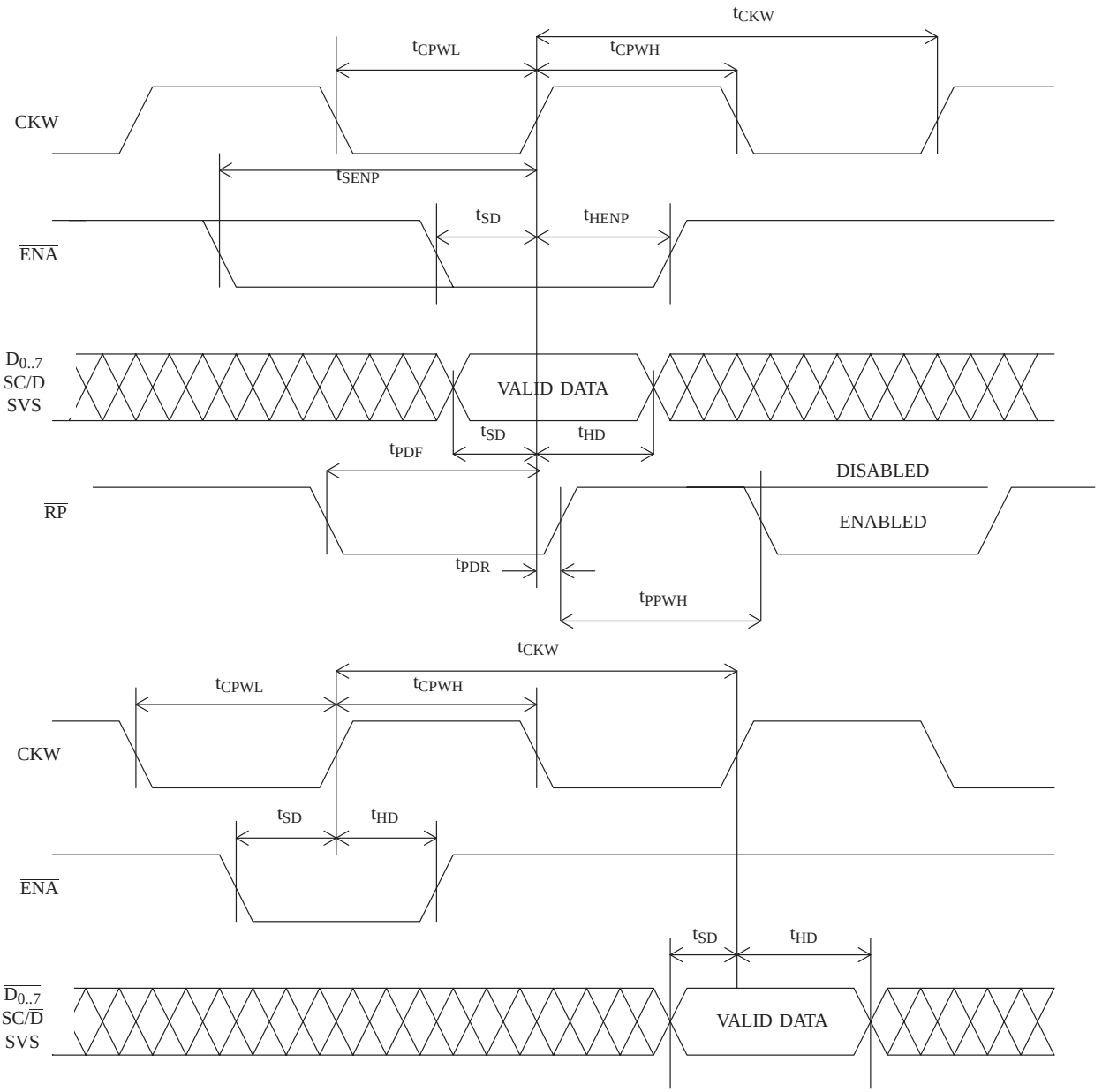
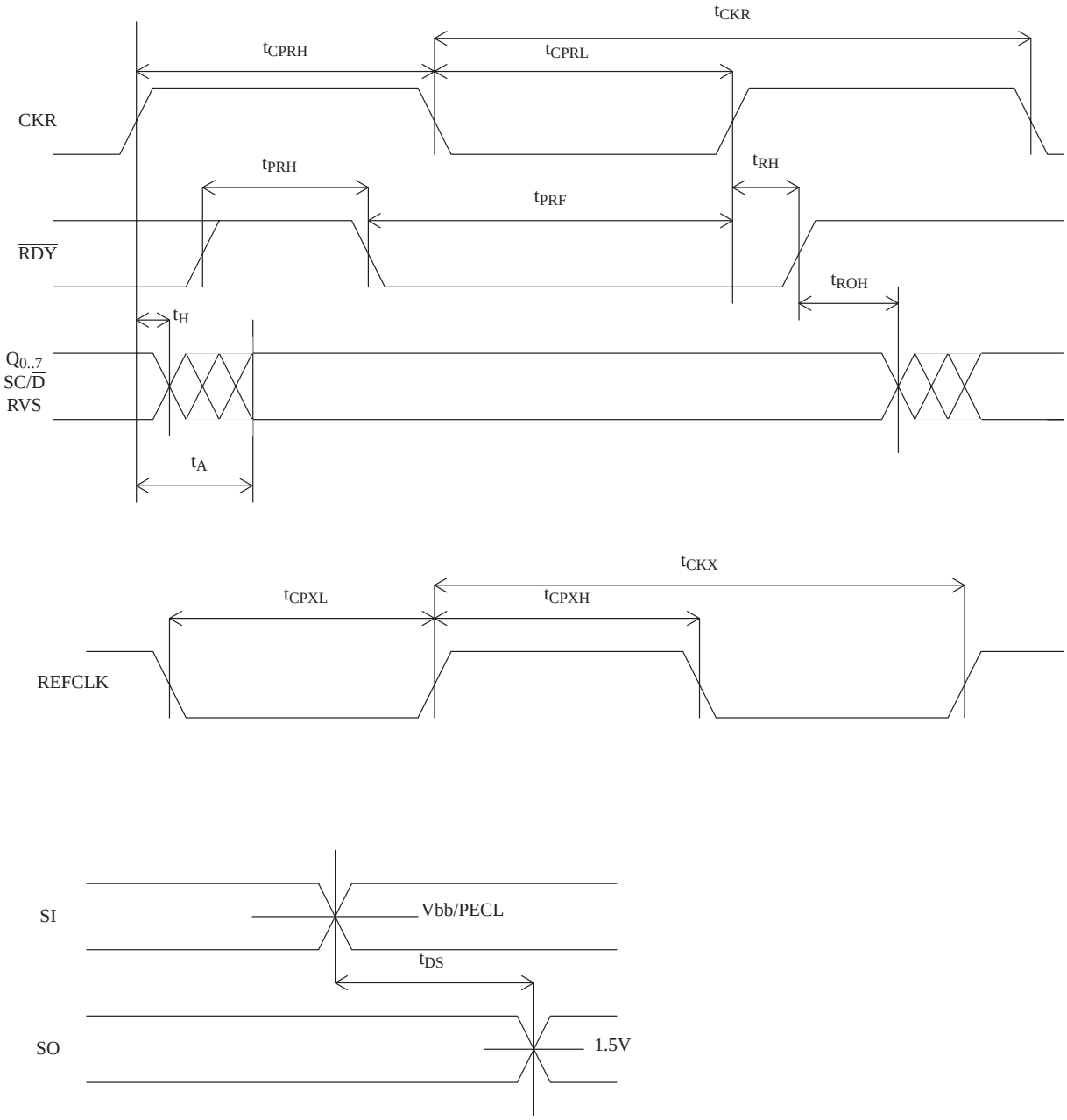
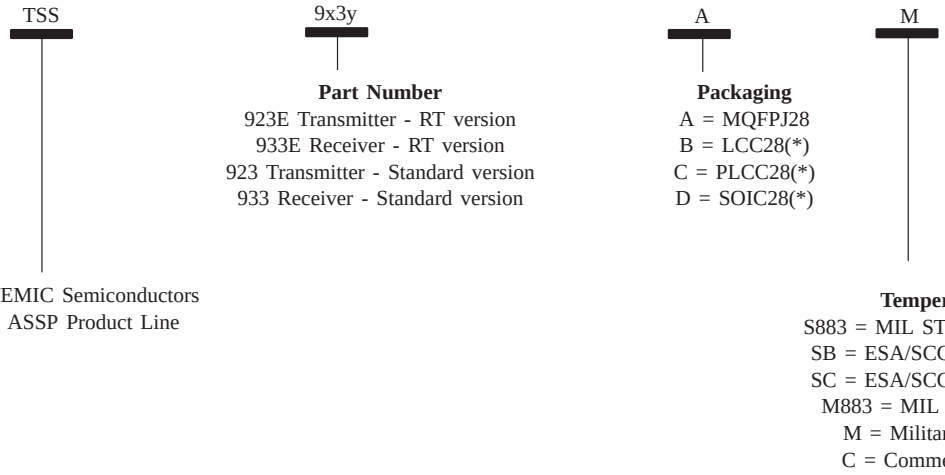


Figure 6. Preliminary Switching Waveforms for the TSS933 Receiver



14. Ordering Information



(*) Preview
(**) Only for E versions