Dynamic Shift Registers

* MM400/MM500 series dynamic shift registers

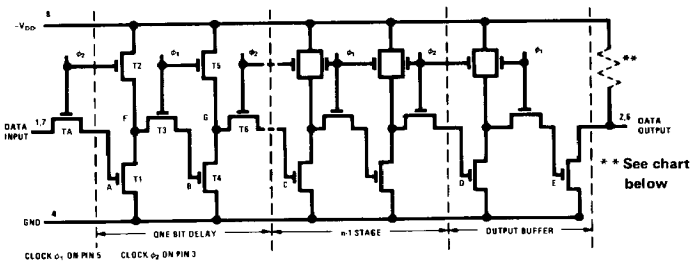
general description

The National Semiconductor line of dynamic shift registers are built on a single silicon chip utilizing MOS P channel enhancement mode transistors. Designed to operate over a wide frequency spectrum, these devices can be used in any sequential digital system that employs a two phase clocking system. The low threshold transistors used permit operation with a V_{DD} supply voltage of −10V and a −16V clock amplitude to obtain these device features:

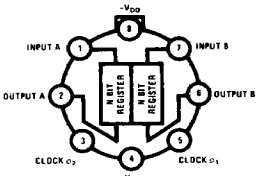
- Direct DTL or TTL compatibility
- High Frequency Operation — 1 MHz guaranteed
- Low Power Consumption — 0.8 mW/bit @ 1 MHz
- Minimum Operating Frequency Guarantee — 600Hz @ 25°C
- Military and Commercial Temperature Ranges
  - MM400 Series — −55°C to +125°C
  - MM500 Series — 0°C to +70°C
- Low Output Impedance (V_{OH}) — 500 ohms
- Clock inputs directly compatible with MH0009, two phase clock driver

The power dissipation of the device decreases as the operating frequency is decreased; at 10 kHz typical dissipation is 6 μW/bit. The minimum operating frequency is also reduced substantially at lower temperatures; typical minimum frequency of operation at 25°C is 100 Hz.

schematic and connection diagrams



Metal Can Package

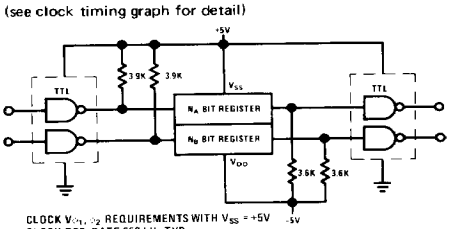


Note: Pin 4 connected to case.
TOP VIEW

Order Number MM400H, MM500H, MM401H, MM501H, MM402H, MM502H, MM403H, MM503H, MM406H, MM506H, MM407H or MM507H
See Package 23

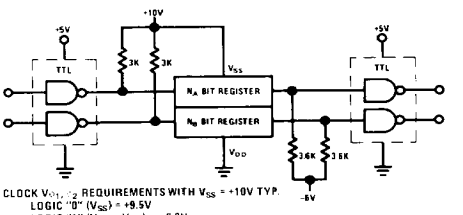
typical applications

FIGURE 1 – TTL/MOS Interface – Low Frequency
(see clock timing graph for detail)



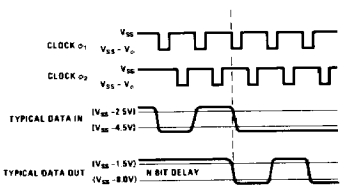
CLOCK V_{ϕ_1, ϕ_2} REQUIREMENTS WITH V_{SS} = +5V
CLOCK REP. RATE 650 kHz TYP.
LOGIC "0" (V_{SS}) = +4.5V
LOGIC "1" ($V_{SS} - V_{\phi L}$) = −10V

FIGURE 2 – TTL/MOS Interfaces



CLOCK V_{ϕ_1, ϕ_2} REQUIREMENTS WITH V_{SS} = +10V TYP.
LOGIC "0" (V_{SS}) = +9.5V
LOGIC "1" ($V_{SS} - V_{\phi L}$) = −6.0V

Waveforms for Applications



Standard Register Configurations †

CONFIGURATION	OPEN DRAIN OUTPUT		20 KΩ OUTPUT	
	−55°C to +125°C	−25°C to +70°C	−55°C to +125°C	−25°C to +70°C
Dual 25 bit	MM400	MM500	MM401	MM501
Dual 50 bit	MM402	MM502	MM403	MM503
*Dual 100 bit	MM406	MM506	MM407	MM507

†For other length registers consult your National representative.
*For New Designs, See MM4006A/MM5006A Data Sheet.

absolute maximum ratings

Drain Voltage ($-V_{DD}$)	+0.5V to −25V
Clock Inputs ($V\phi_1$, $V\phi_2$)	+0.5V to −25V
Data Inputs	+0.5V to −25V
Power Dissipation (Note 1)	500 mW
Operating Temperature	
MM400 Series	−55°C to +125°C
MM500 Series	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Repetition Rate	See Fig. 2	See Note 5		1.0	MHz
	See Fig. 1	See Note 5		0.5	MHz
Clock Input Capacitance (Pins 3 & 5)	f = 1.0 MHz, 0V Bias				
	MM400, 401, 500, 501		22	40	pF
	MM402, 403, 502, 503		40	60	pF
	MM406, 407, 506, 507		85	100	pF
	−20V Bias				
	MM400, 401, 500, 501		18	25	pF
	MM402, 403, 502, 503		32	40	pF
	MM406, 407, 506, 507		55	65	pF
Data Output Voltage Levels					
MOS to MOS	V_{DD} = −10V, V_{SS} = GND				
Logic "0" (V_{OH})	freq = 1 MHz max. Input (d.c.)			V_{SS} −1.5	V
Logic "1" (V_{OL})		V_{SS} −8.0V			V
MOS to TTL (Fig. 1)	V_{DD} = GND, V_{SS} = +10V freq = 1 MHz max. Input (d.c.)				
Logic "0" (V_{OH})	I_L = 2.5 mA } See Note 6	2.5			V
Logic "1" (V_{OL})	I_L = −1.6 mA } See Note 6			0.4	V
MOS to TTL (Fig. 2)	V_{DD} = −5V, V_{SS} = +5V (V_{SS} = 4.75 min) freq = 0.5 MHz max.				
Logic "0" (V_{OH})	I_L = 2.5 mA } See Note 6	2.5			V
Logic "1" (V_{OL})	I_L = −1.6 mA } See Note 6			0.4	V
Breakdown Voltage	1.0 μA Test Current T_A = 25°C				
On Pin 1	GND on Pins 2, 3, 4, 5, 6, 7 −8V on Pin 8	−25			V
On Pin 2 (Note 3)	GND on Pins 1, 4, 6, 7, 8 −8V on Pins 3, 5	−25			V
On Pin 6 (Note 3)	GND on Pins 1, 2, 4, 7, 8 −8V on Pins 3, 5	−25			V
On Pin 7	GND on Pins 1, 2, 3, 4, 5, 6 −8V on Pin 8	−25			V
Leakage Current	T_A = 25°C				
Pin 1	V_1 = −18V, V_8 = −8V All Other Pins at GND			0.5	μA
Pin 2 (Note 4)	V_2 = −18V, V_3 = V_5 = −8V All Other Pins at GND			0.5	μA
Pin 6 (Note 4)	V_6 = −18V, V_3 = V_5 = −8V All Other Pins at GND			0.5	μA
Pin 7	V_7 = −18V, V_8 = −8V All Other Pins at GND			0.5	μA
Pin 8 (Note 4)	V_8 = −8V All Other Pins at GND			0.5	μA
Power Supply Current Drain	Outputs at Logic "1" 1 MHz Operations, T_A = 25°C (ϕ_1 = 0.4 μs, ϕ_2 = 0.2 μs)				
	MM400,401,500,501		4.5	9.0	mA
	MM402,403,502,503		9.0	14.0	(Average)
	MM406,407,506,507		18.0	30.0	

electrical drive requirements

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Pulse Width	See Timing Diagram				
ϕ_1 Clock pw		0.4		10.0	μs
ϕ_2 Clock pw		0.2		10.0	μs
Clock Delay, ϕ_d	See Definition	0.1			μs
Clock Pulse Transition $t_{r\phi}$, $t_{f\phi}$	1 MHz, ϕ_{pw} = 0.2 μs			0.05	μs
	100 kHz, ϕ_{pw} = 0.2 μs			0.5	μs
	10 kHz, ϕ_{pw} = 10 μs			5.0	μs
Clock Input Level (V_ϕ)					
Logic "0" ($V_{\phi H}$)			V_{SS} −0.5	V_{SS} −1.5	V
Logic "1" ($V_{\phi L}$)		V_{SS} −14.5	V_{SS} −16.0	V_{SS} −18.0	V
Data Pulse Width t_{dw}		0.4			μs
Data Setup Time t_{ds}		0.1			μs
Data Input Voltage Levels					
MOS to MOS					
Logic "0" (V_{IH})	V_{DD} = −10V, V_{SS} = GND			2.0	V
Logic "1" (V_{IL})	freq = 1 MHz max.	−7.0			V
TTL to MOS (Fig. 1)					
Logic "0" (V_{IH})	V_{DD} = GND, V_{SS} = +10V			V_{SS} 2.0	V
Logic "1" (V_{IL})	freq = 1 MHz max.	V_{SS} −7.0			V
TTL to MOS (Fig. 2)					
Logic "0" (V_{IH})	V_{DD} = −5V, V_{SS} = +5V			V_{SS} 1.5	V
Logic "1" (V_{IL})	(V_{SS} = 4.75 min)				
	freq = 0.5 MHz max.	V_{SS} −4.2			V

Note 1: For operating at elevated temperatures, the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +150°C/W junction to ambient. The full rating applies for case temperatures to +125°C for MM400 Series and +70°C for MM500 Series units.

Note 2: These specifications apply over the indicated operating temperature ranges for V_{SS} = 0V and −11V < V_{DD} < −9.5V and 20 kΩ connected between pins 2 and 8 and between pins 6 and 8 without measurement load of less than 10 pF in parallel with 10 MΩ to ground unless otherwise specified. On the MM401/MM501, MM403/MM503, and MM407/MM507 optional versions which include 20 kΩ pull-up resistors internal to package, the external 20 kΩ resistors are not used in measurement circuits.

Note 3: For the odd number devices, MM401, MM403 and MM407, the output of pins 2 and 6 will exhibit a resistance when measured with the following bias conditions: pins 1, 6 and 8 = GND; pins 3 and 5 = −16V; pin 4 = open; measure pins 2 and 6 = 25k ≤ R_{OUT} ≤ 15 kΩ.

Note 4: Not for internal resistor devices.

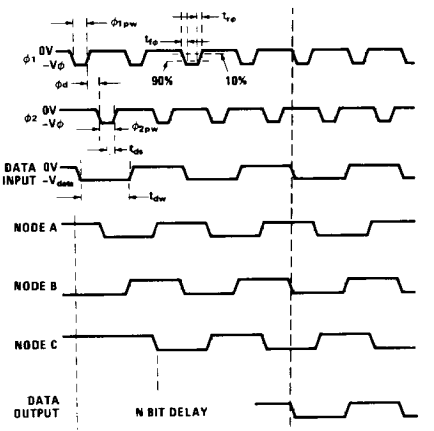
Note 5: See minimum operating frequency graph.

Note 6: In the logic "0" (V_{OH}) level the MOS register output will be sourcing 2.5 mA into the load combination of the pull-down resistors and the gate leakage current. In the logic "1" V_{OL} level I_L represents the current that the pull-down resistor and the internal 20k resistor combination will sink in order to insure current sinking capability for one gate.

operation

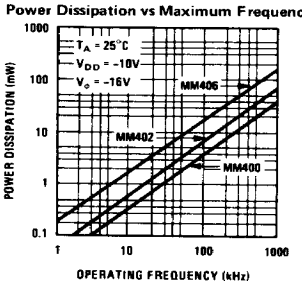
Each bit of delay shown in the circuit schematic consists of two inverters T1 and T4 accompanied by clocked load resistors T2 and T5 and two coupling devices T3 and T6. The circuit functions as follows: When ϕ_2 goes negative (one state) the coupling unit TA and the load resistor T2 are clocked ON allowing information at the input to be transferred to node A turning T1 ON or OFF depending on the state of the input. For example, if a negative potential (near $-V_{DD}$ level) is transferred from the input to the gate to source capacitance at node A, then T1 turns ON allowing node F to be at $\frac{-V_{DD}}{2}$. When ϕ_2 returns to its zero state (ground level) T2 turns OFF allowing node F to discharge to zero volts. When ϕ_1 goes negative (one state) the coupling unit T3 and the load resistor T5 are clocked ON allowing information at node F to be transferred to node B. T4 is held OFF if node F was at ground potential and is turned ON if node F had been at $-V_{DD}$ potential. Continuing the example above, T4 is held OFF and node G is at $-V_{DD}$ since T5 is ON during ϕ_1 clock pulse. When ϕ_1 returns to its zero state, node G maintains a $-V_{DD}$ voltage level. This voltage level is maintained at node G until the ϕ_2 clock appears. The bit delay demonstrated in this example is repeated through each half of the dual register.

timing diagram

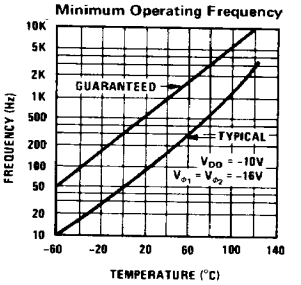


performance characteristics

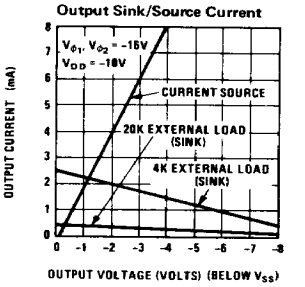
Power Dissipation vs Maximum Frequency



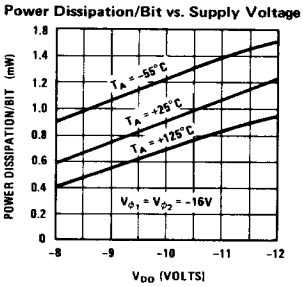
Minimum Operating Frequency



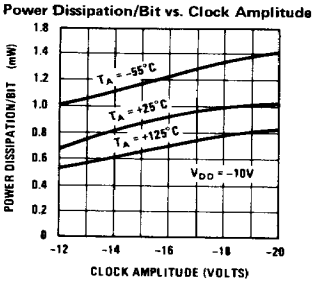
Output Sink/Source Current



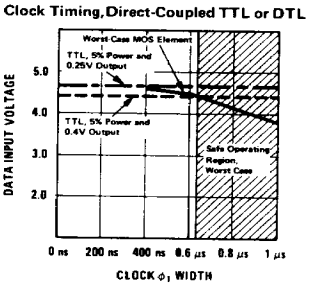
Power Dissipation/Bit vs. Supply Voltage



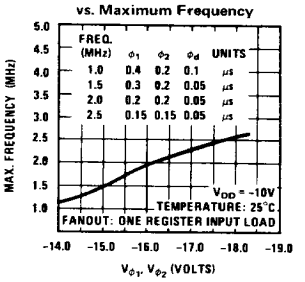
Power Dissipation/Bit vs. Clock Amplitude



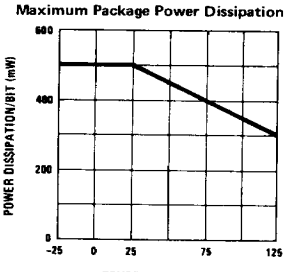
Clock Timing, Direct-Coupled TTL or DTL



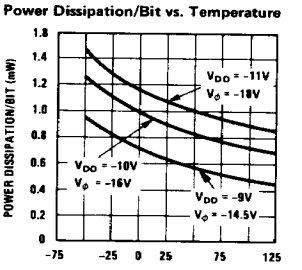
Clock Amplitude V_{ϕ_1}, V_{ϕ_2} vs. Maximum Frequency



Maximum Package Power Dissipation



Power Dissipation/Bit vs. Temperature



Note: All typical performance data is gathered with ϕ_{pw} = 0.4 μ; ϕ_{2pw} = 0.2 μs; ϕ_d = 0.1 μs; f = 1 MHz; except as otherwise noted.