

16-CHANNEL 12-BIT DELTA-SIGMA DIGITAL-TO-ANALOG CONVERTER

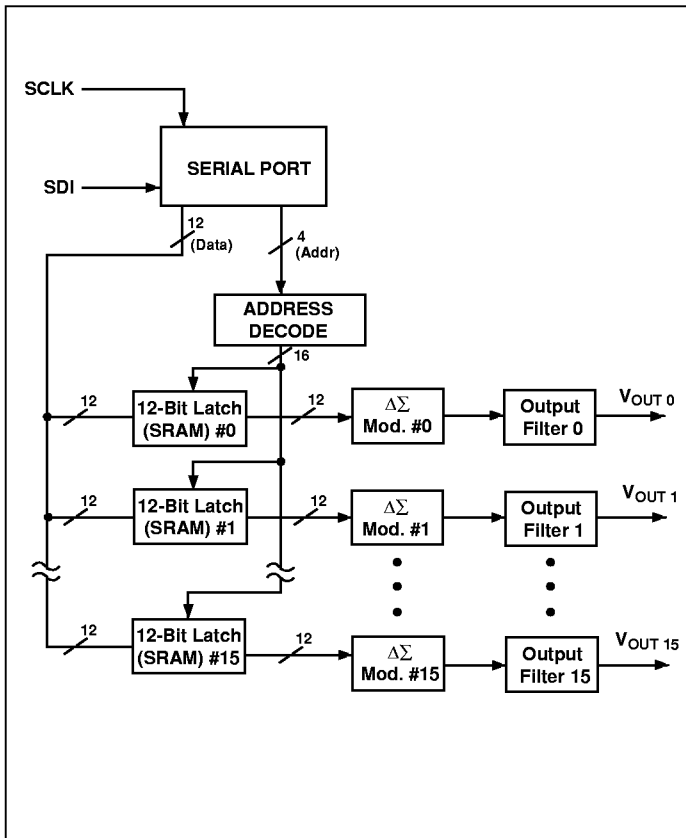
FEATURES

- 3-Wire Serial Interface Port
- 12 Bit Resolution
- 16 Randomly Addressable Channels
- 3mA Source/Sink Voltage Mode Outputs
- Bipolar Output Voltage

TYPICAL APPLICATIONS

- Digital Control Systems
- Function Generators
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM



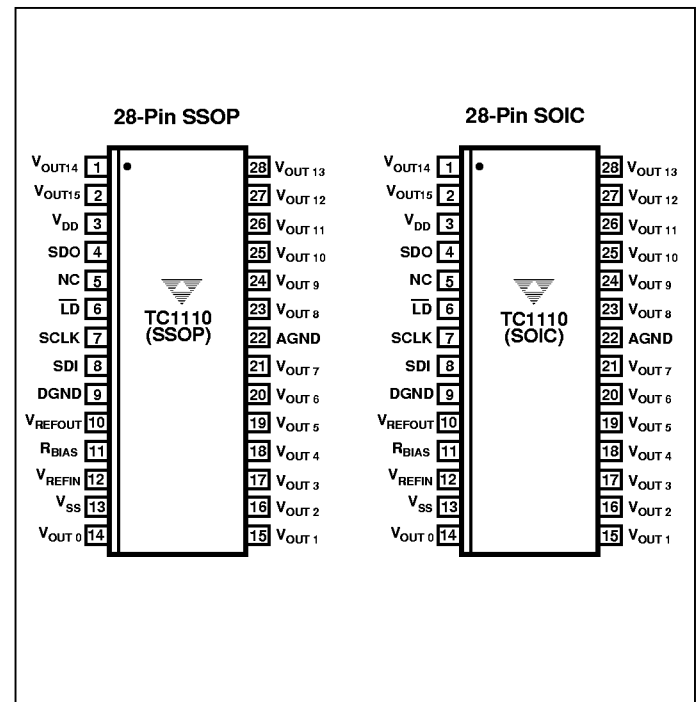
GENERAL DESCRIPTION

The TC1110 is a serial, 16-channel, 12-bit, Delta-Sigma digital-to-analog converter (DAC) intended for use in automatic calibration and other low frequency applications. Data is transferred from the host to the TC1110 via a 3-wire serial port in a 16-bit address/data format (12 data bits plus 4 address bits), allowing any one of the 16 DAC channels to be selected and loaded in a single serial port access cycle. Once latched in, the output voltage settles in 100 μ s (max), then data is continuously converted at a 7.5 MHz rate. The TC1110 is available in 28-pin SSOP and SOIC packages and operates from ± 5 V supplies.

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC1110CSI	28-Pin SSOP	0°C to 70°C
TC1110COI	28-Pin SOIC	0°C to 70°C

PIN CONFIGURATION



16-CHANNEL 12-BIT SERIAL-INPUT VOLTAGE-OUTPUT DIGITAL-TO- ANALOG CONVERTER

TC1110

ABSOLUTE MAXIMUM RATINGS*

Positive Supply Voltage (V_{DD} to GND)	+5.5V, -0.3V
Negative Supply Voltage (V_{SS} to GND)	-5.5V, +0.3V
Input Voltage (Any Pin to GND) ...	$V_{DD} + 0.3V$, $V_{SS} - 0.3V$
Output Voltage (Any Pin to GND)	$V_{DD} + 0.3V$, $V_{SS} - 0.3V$
Output Current	+10/-50 mA
Short-Circuit Duration (V_{OUT} to GND)	Indefinite
Operating Temperature Range	0°C to +70°C
Storage Temperature (Unbiased)	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Power Dissipation

SOIC-28	1000 mW
SSOP-28	940 mW

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Values	Unit
V_{DD}	Positive Operating Voltage		$5.0 \pm 5\%$	V
V_{SS}	Negative Operating Voltage		$-5.0 \pm 5\%$	V
T_A	Ambient Operating Temperature		0°C to 70°C	°C
ESD	Electrostatic Discharge Into Any Pin	Tested Per MIL-STD-883, Method 3015.2	± 1500	V
I_{MAX}	Current Into Any Pin To Avoid Latchup		± 50	mA

ELECTRICAL CHARACTERISTICS:

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DC Electrical Characteristics						
V_{DD}	Positive Supply Voltage		4.75	5	5.25	V
V_{SS}	Negative Supply Voltage		-5.25	-5	-4.75	V
I_{SS}	Power Supply Current, Outputs Without Load		10	—	20	mA
I_{DD}			5	—	10	mA
V_{IL}	Low-Level Input Logic Voltage		$V_{SS} - 0.3$	—	1.5	V
V_{IH}	High-Level Input Logic Voltage		3.5	—	$V_{DD} + 0.3$	V
V_{OL}	Low-Level Output Voltage at SDO		—	—	400	mV
V_{OH}	High-Level Output Voltage at SDO		4.0	—	—	V
I_{IL}	Input Leakage Current at SCLK, SDI, LDB, and V_{REFIN}		-10	—	10	μA
C_{IN}	Input Capacitance, Analog and Digital Inputs		—	—	10	pF

DAC Section

	Resolution		12	12	12	Bits
INL	Integral Non-Linearity	$T_A = 0^\circ C$ to $70^\circ C$, $I_{OUT} \leq 1$ mA (Note 5)	-2	—	+2	LSB
DNL	Differential Non-Linearity	All Codes	-0.8	—	+0.8	LSB
V_{OUT}	Output Voltage	At Code = 7FF _H	-2.48	-2.46	-2.44	V
		At Code = FFF _H	2.44	2.46	2.48	V
		At Code = 800 _H	-20	0	20	mV
$\Delta V_{OUT}/\Delta T$	Output Voltage Offset Change Referred to Ground, Over Temperature (Note 2)		-125	—	125	$\mu V/^\circ C$
V_{REFOUT}	Reference Output Voltage with Respect to Analog Ground		-2.55	-2.50	-2.45	V

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ELECTRICAL CHARACTERISTICS (Cont.):

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OUT}	Reference Output Current		200	—	—	μA
PSRR	Power Supply Rejection Ratio	V_{DD}, V_{SS} at DC	45	—	—	dB
		V_{DD}, V_{SS} at 100 KHz	35	—	—	dB
Crosstalk		(Note 3)	65	—	—	dB
Z_{OUT}	Dynamic Output Resistance	Ohmic Component of Z_{OUT} (Note 1, 2)	—	—	5.0	Ω
		Non-Linear Component of Z_{OUT} (Note 1, 2)	—	—	1.0	Ω
I_{SC}	Output Short-Circuit Current (Note 4)	Source	10	—	—	mA
		Sink	40	—	—	mA
$\tau_{SETTLE(FS+)}$	Output Voltage Full-Scale Settling Time	Positive Transition	—	—	100	μsec
$\tau_{SETTLE(FS-)}$	Output Voltage Full-Scale Settling Time	Negative Transition	—	—	100	μsec
AC Timing Characteristics						
τ_{ds}	Data Setup Time (Note 2)	Required Delay Before Rising Edge of SCLK	50	—	—	nsec
τ_{dh}	Data Hold Time (Note 2)	Required Delay After Rising Edge of SCLK	50	—	—	nsec
τ_{wld}	Load Pulse Width		80	—	—	nsec
τ_r	Input Rise Time	All Logic Inputs	—	—	50	nsec
τ_f	Input Fall Time	All Logic Inputs	—	—	50	nsec
T_{SCLK}	Serial Clock Period		200	—	—	nsec
f_{SCLK}	Serial Clock Frequency		—	—	5	MHz
$\tau_{pd(SDO)}$	Serial Data Output Delay from SCLK		—	—	150	nsec
τ_{id}	Setup Time After the Last Data Bit into the Shift Register Before LDB Falling Edge		50	—	—	nsec
f_i	Internal Clock Frequency		—	7.5	—	MHz

- NOTES:**
1. Unless otherwise specified, $V_{REF} = -2.500V$, $V_{DD} = +5.00V$, $V_{SS} = -5.00V$, $T_A = 25^\circ C$, and Channel Output Load = 1 mA/Ch.
 2. Guaranteed by design.
 3. Crosstalk is measured by having one output channel swing between minus full scale and positive full scale and measuring the change(s) on any other channel.
 4. Package power dissipation limits must be observed. Do not short more than four outputs simultaneously.
 5. INL measured using "Best Fit" method.

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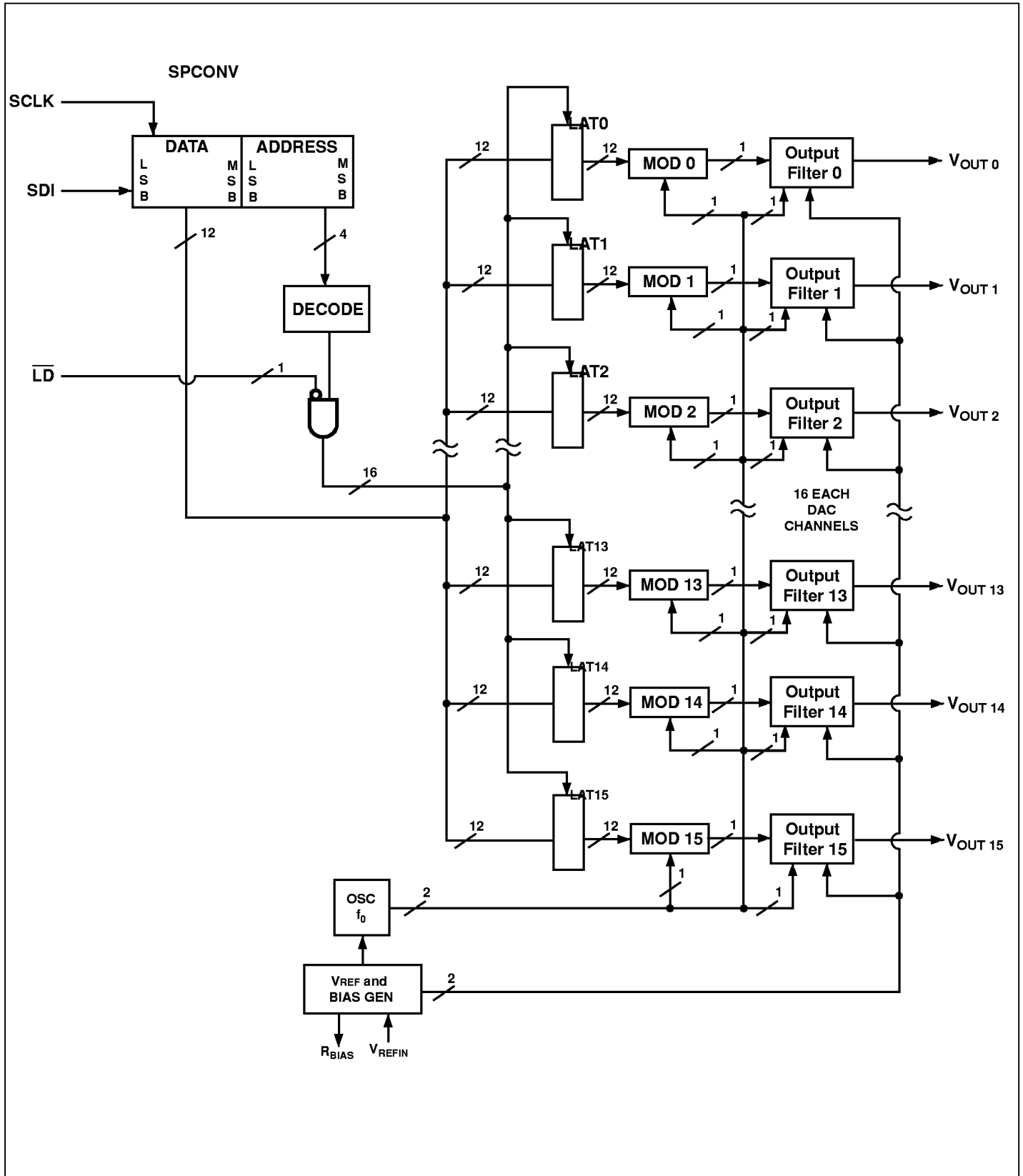
PIN DESCRIPTION

Pin Number	Name	Description
1	V _{OUT14}	Analog Voltage Output Channel 14
2	V _{OUT15}	Analog Voltage Output Channel 15
3	V _{DD}	Positive 5.0V ±5% Supply
4	SDO	Digital CMOS Level Serial Data Output
5	NC	Not Connected
6	$\overline{\text{LD}}$	Digital CMOS Level Load Register Input (Active Low)
7	SCLK	Digital CMOS Level Serial Data Clock Input
8	SDI	Digital CMOS Level Serial Data Input
9	DGND	0 Volt Digital Ground
10	R _{BIAS}	Analog Bias Resistor Pin
11	V _{REFOUT}	Analog Internal Voltage Reference
12	V _{REFIN}	Analog Reference Voltage Input
13	V _{SS}	Negative 5.0V ±5% Supply
14	V _{OUT0}	Analog Voltage Output Channel 0
15	V _{OUT1}	Analog Voltage Output Channel 1
16	V _{OUT2}	Analog Voltage Output Channel 2
17	V _{OUT3}	Analog Voltage Output Channel 3
18	V _{OUT4}	Analog Voltage Output Channel 4
19	V _{OUT5}	Analog Voltage Output Channel 5
20	V _{OUT6}	Analog Voltage Output Channel 6
21	V _{OUT7}	Analog Voltage Output Channel 7
22	AGND	0 Volt Analog Ground
23	V _{OUT8}	Analog Voltage Output Channel 8
24	V _{OUT9}	Analog Voltage Output Channel 9
25	V _{OUT10}	Analog Voltage Output Channel 10
26	V _{OUT11}	Analog Voltage Output Channel 11
27	V _{OUT12}	Analog Voltage Output Channel 12
28	V _{OUT13}	Analog Voltage Output Channel 13

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DETAILED FUNCTIONAL BLOCK DIAGRAM



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DETAILED DESCRIPTION

Digital to Analog conversion is accomplished using Delta-Sigma modulators operating at a nominal 7.5 MHz frequency. Each modulator converts input data stored in its latch into a 1-bit wide, 7.5 MHz bit stream, (the average DC analog value of which equals that of the input data). The bit stream from each modulator is integrated by a low-pass output filter, then amplified and buffered.

DAC Input Codes

Each DAC output (V_{OUT0} - V_{OUT15}) generates $-0.984 V_{REF}$ to $+0.984 V_{REF}$ for the set of input codes shown in Figure 1 (where "x" is the 4-bit DAC address). V_{REF} is a negative reference voltage applied to V_{REFIN} . The reference can have any value between $-2V$ and $-3V$. Note that bits D10 – D0 (inclusive) determine the magnitude of the output voltage, while bit D11 determines its polarity. As shown, positive output voltages are generated when D11 = 1, and negative output voltages are generated when D11 = 0. An output voltage of 0V is generated when D10 – D0 = 000, regardless of the state of D11.

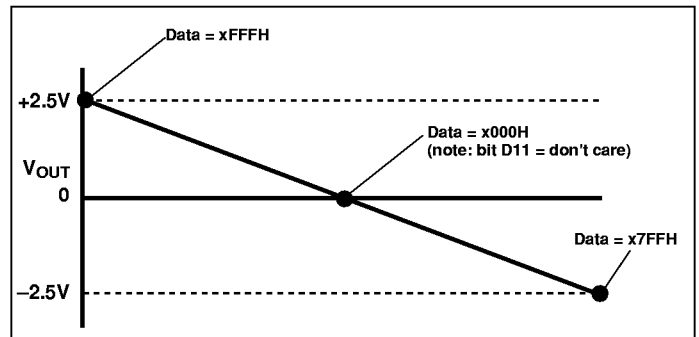


Figure 1. DAC Input Codes

Reference Voltage and Bias Resistor

Either the internal reference voltage (Pin 11) or an external voltage reference must be connected from the V_{REFIN} input (Pin 12) to the analog ground as shown in Figure 2. This voltage is used as the \pm full-scale reference for the DAC. It is also used with an external resistor connected between R_{BIAS} (Pin 10) and AGND (Pin 22) to set the bias conditions for the internal circuitry. The value of the external resistor, R_{BIAS} , must be equal to $R_{BIAS} = IV_{REFI}/5\mu A$. If $V_{REF} = -2.500V$, $R_{BIAS} = 500K$ (499K is close enough).

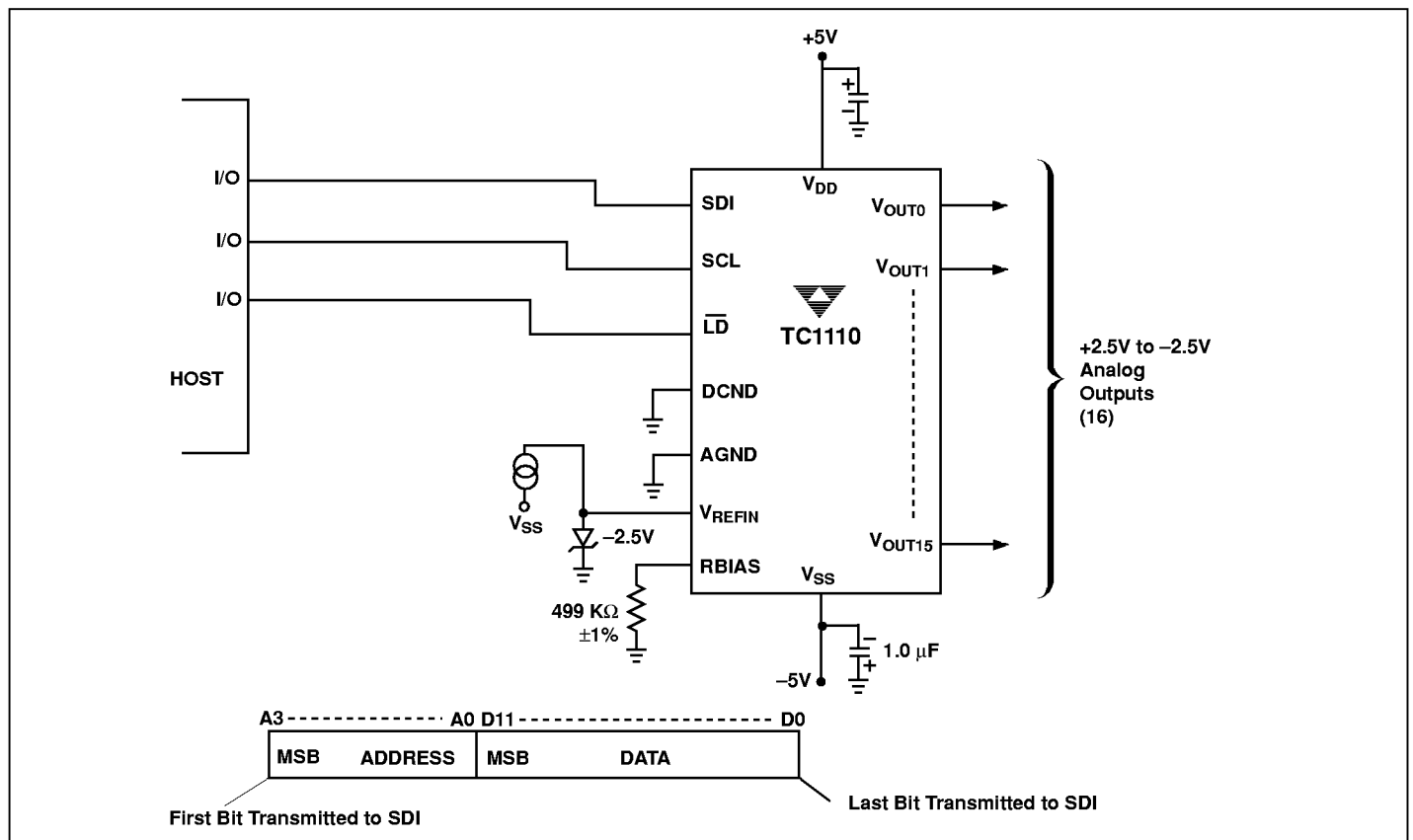


Figure 2. TC1110 Application

16-CHANNEL 12-BIT SERIAL-INPUT VOLTAGE-OUTPUT DIGITAL-TO- ANALOG CONVERTER

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Serial Port

The serial port consists of a clock input (SCLK), serial data input (SDI), and a load input (\overline{LD}). The serial data output pin (SDO, Pin 4) is the output of the 16th flip-flop in the receive register. When \overline{LD} goes low, the value of SDO is the value of the address MSB of the 16-bit word that is being loaded. The entire word can be read out by strobing SCLK 15 more times for diagnostic purposes or to daisy-chain multiple TC1110s.

\overline{LD} is kept high, except when shifting data into the DAC registers. With \overline{LD} maintained high, the host places data on

SDI and clocks it into the serial port with SCLK (data is clocked into SDI on the rising edge of SCLK). The 16-bit address/data word from the host must be in the format shown in Figure 2 (i.e. 4-bit address followed by 12-bit data, each with the most significant bit first). After the address/data word is transferred, the host brings \overline{LD} low, which transfers input data from the serial port receive register into the appropriate DAC input register, (on the falling edge of \overline{LD}).

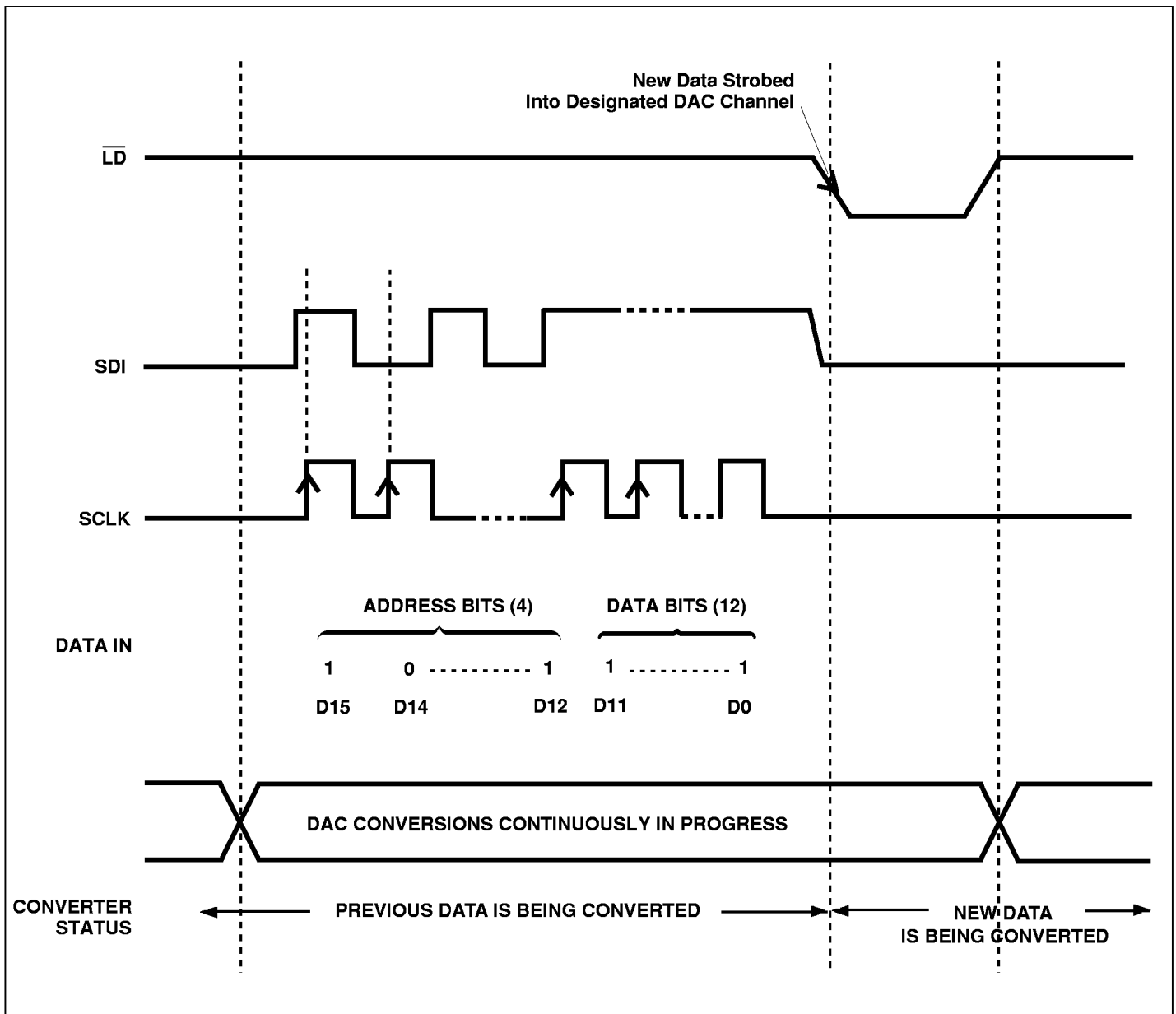
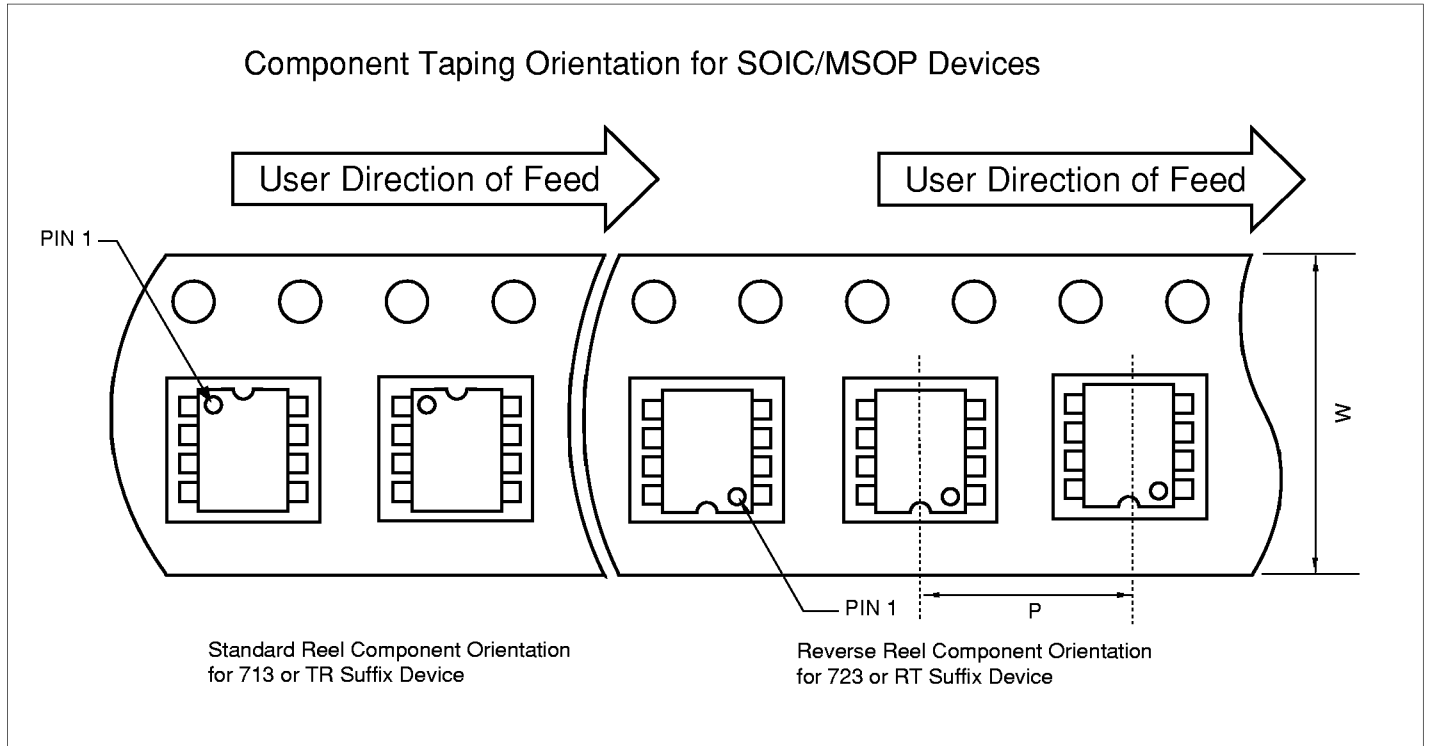


Figure 3. Serial Port Access Cycle

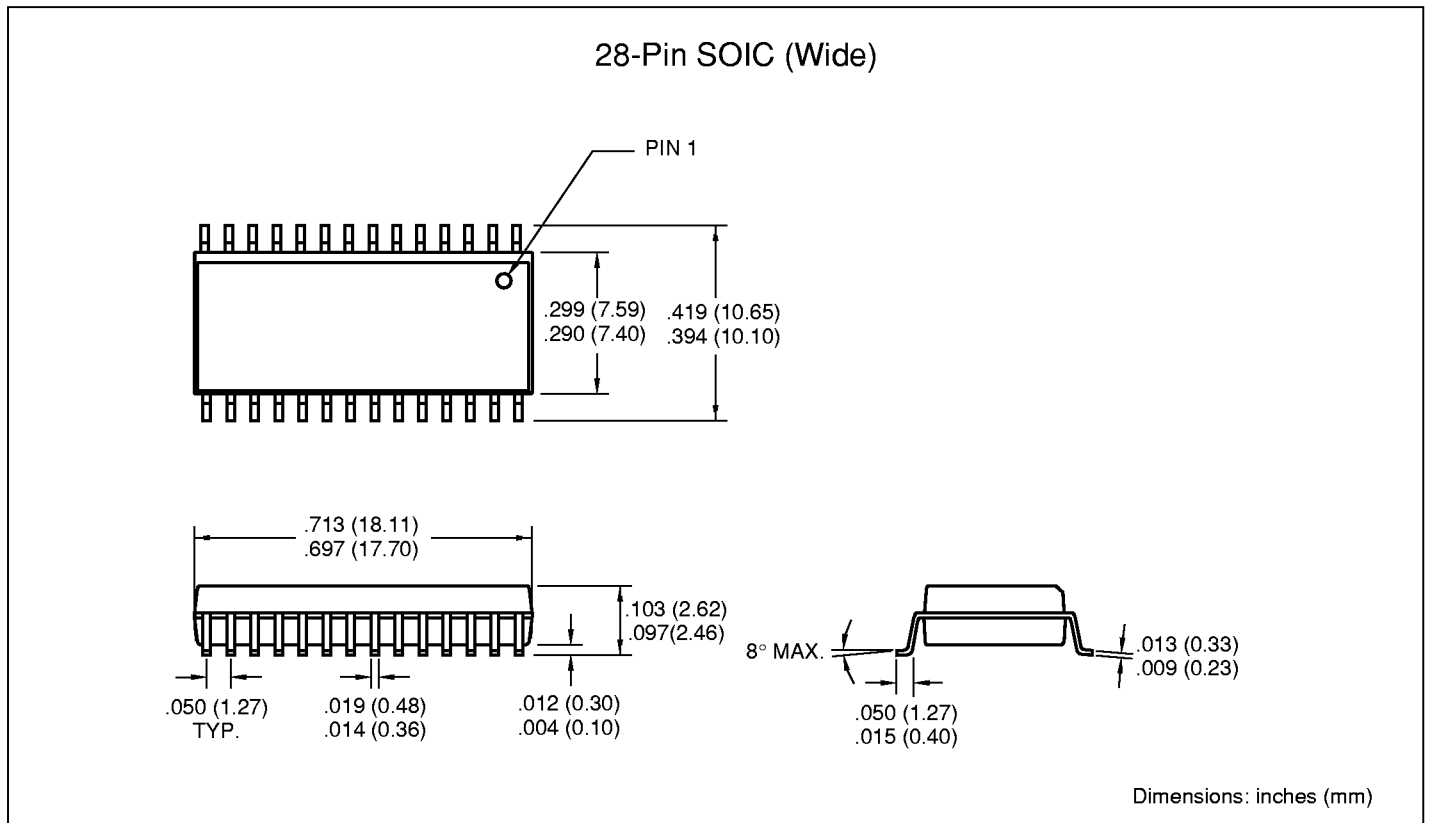
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TAPING FORM



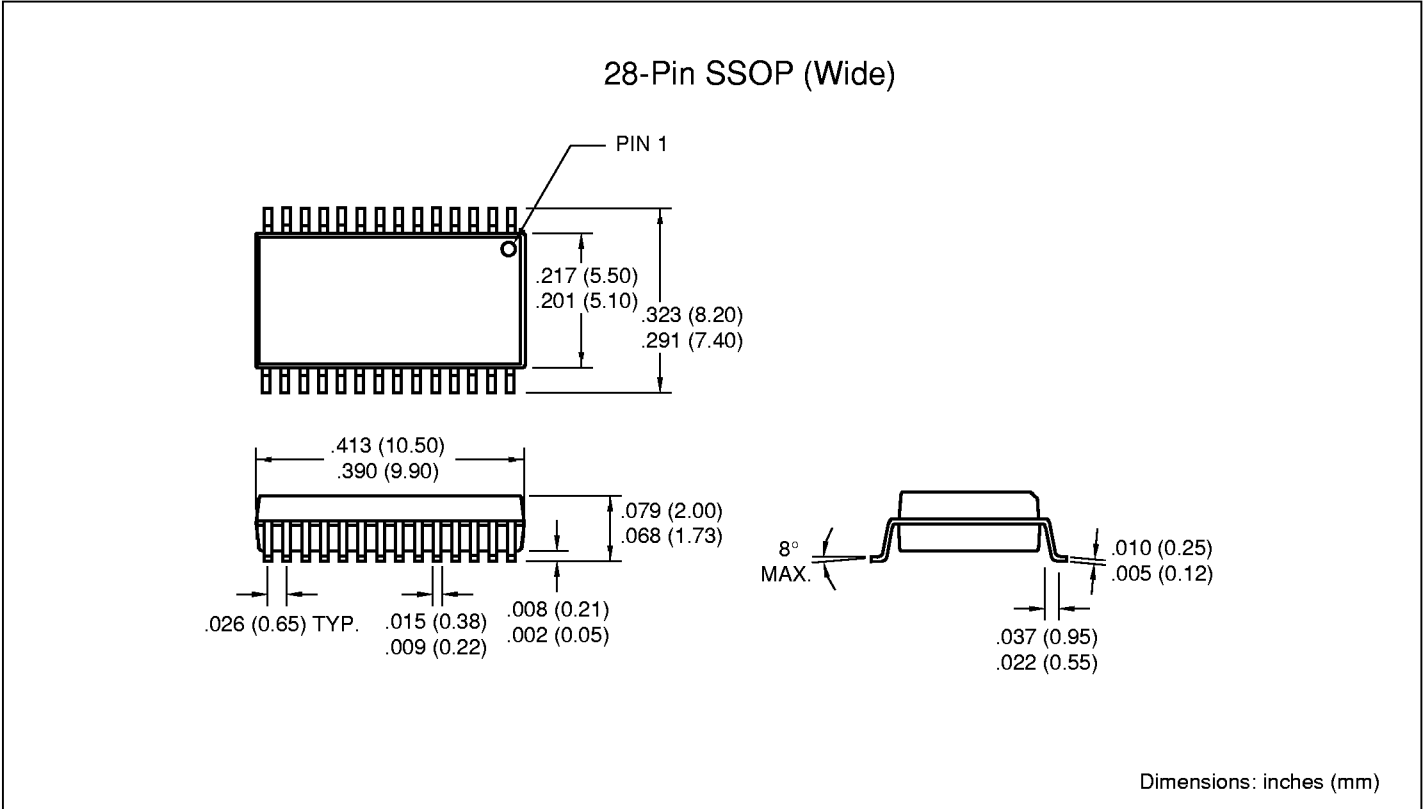
PACKAGE DIMENSIONS



16-CHANNEL 12-BIT SERIAL-INPUT VOLTAGE-OUTPUT DIGITAL-TO- ANALOG CONVERTER

TC1110

PACKAGE DIMENSIONS



Sales Offices

TelCom Semiconductor, Inc.
1300 Terra Bella Avenue
P.O. Box 7267
Mountain View, CA 94039-7267
TEL: 650-968-9241
FAX: 650-967-1590
E-Mail: liter@telcom-semi.com

TelCom Semiconductor, GmbH
Lochhamer Strasse 13
D-82152 Martinsried
Germany
TEL: (011) 49 89 895 6500
FAX: (011) 49 89 895 6502 2

TelCom Semiconductor H.K. Ltd.
10 Sam Chuk Street, Ground Floor
San Po Kong, Kowloon
Hong Kong
TEL: (011) 852-2350-7380
FAX: (011) 852-2354-9957