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INFRARED REMOTE CONTROL TRANSMITTER RC-5

GENERAL DESCRIPTION

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The keyboard interconnection is illustrated by Fig.3.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section **"KEYBOARD OPERATION"**.

Features

- Low voltage requirement
- Biphase transmission technique
- Single pin oscillator
- Test mode facility

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{DD}	2	–	7	V
Input voltage range*	V_I	−0.5	–	V_{DD}+0.5	V
Input current	I_I	–	–	±10	mA
Output voltage range*	V_O	−0.5	–	V_{DD}+0.5	V
Output current	I_O	–	–	±10	mA
Operating ambient temperature range	T_{amb}	−25	–	85	°C

* V_{DD}+0.5 V must not exceed 9 V.

The use of this device must conform with the Philips Standard number URT-0421.

PACKAGE OUTLINES

28-lead DIL plastic; (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

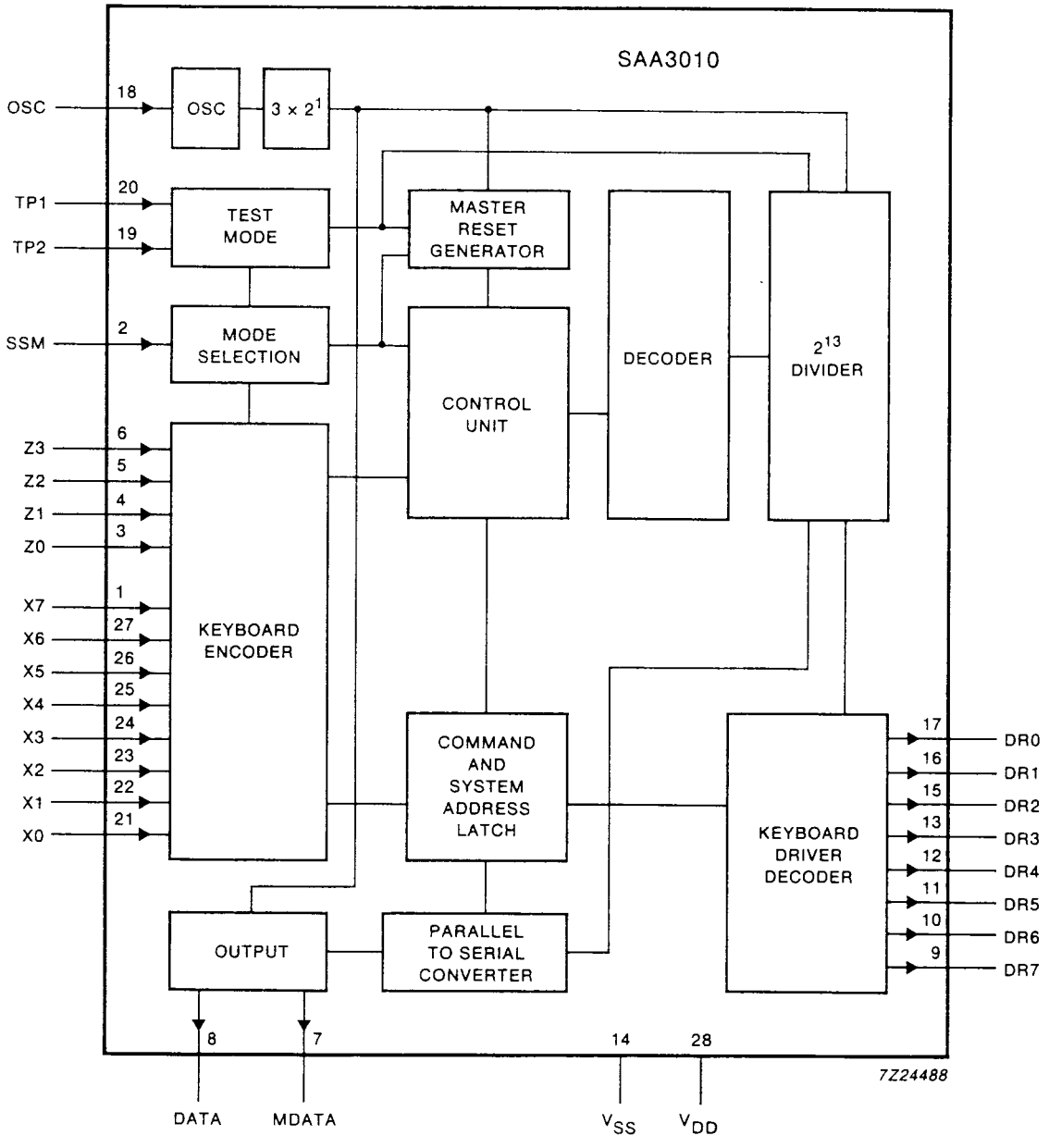


Fig.1 Block diagram.

PINNING

pin	mnemonic	function
1	X7 (IPU)	sense input from key matrix
2	SSM (I)	system mode selection input
3-6	Z0-Z3 (IPU)	sense inputs from key matrix
7	MDATA (OP3)	generated output data modulated with 1/12 the oscillator frequency at a 25% duty factor
8	DATA (OP3)	generated output information
9-13	DR7-DR3 (ODN)	scan drivers
14	V_{SS}	ground (0 V)
15-17	DR2-DR0 (ODN)	scan drivers
18	OSC (I)	oscillator input
19	TP2 (I)	test point 2
20	TP1 (I)	test point 1
21-27	X0-X6 (IPU)	sense inputs from key matrix
28	V_{DD} (I)	voltage supply

(I) = input
(IPU) = input with p-channel pull-up transistor
(ODN) = output with open drain n-channel transistor
(OP3) = output 3-state

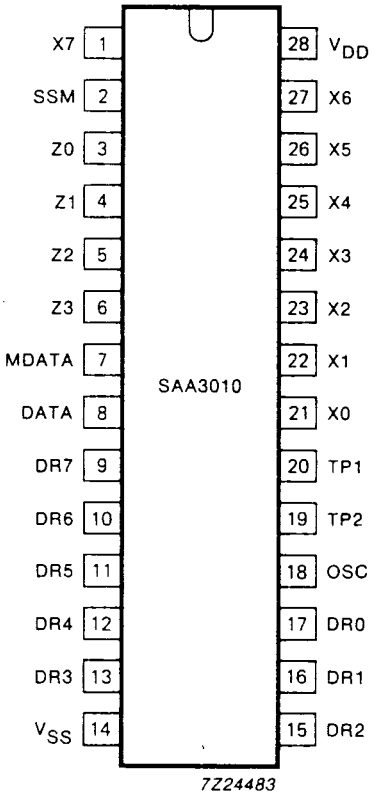


Fig.2 Pinning diagram.

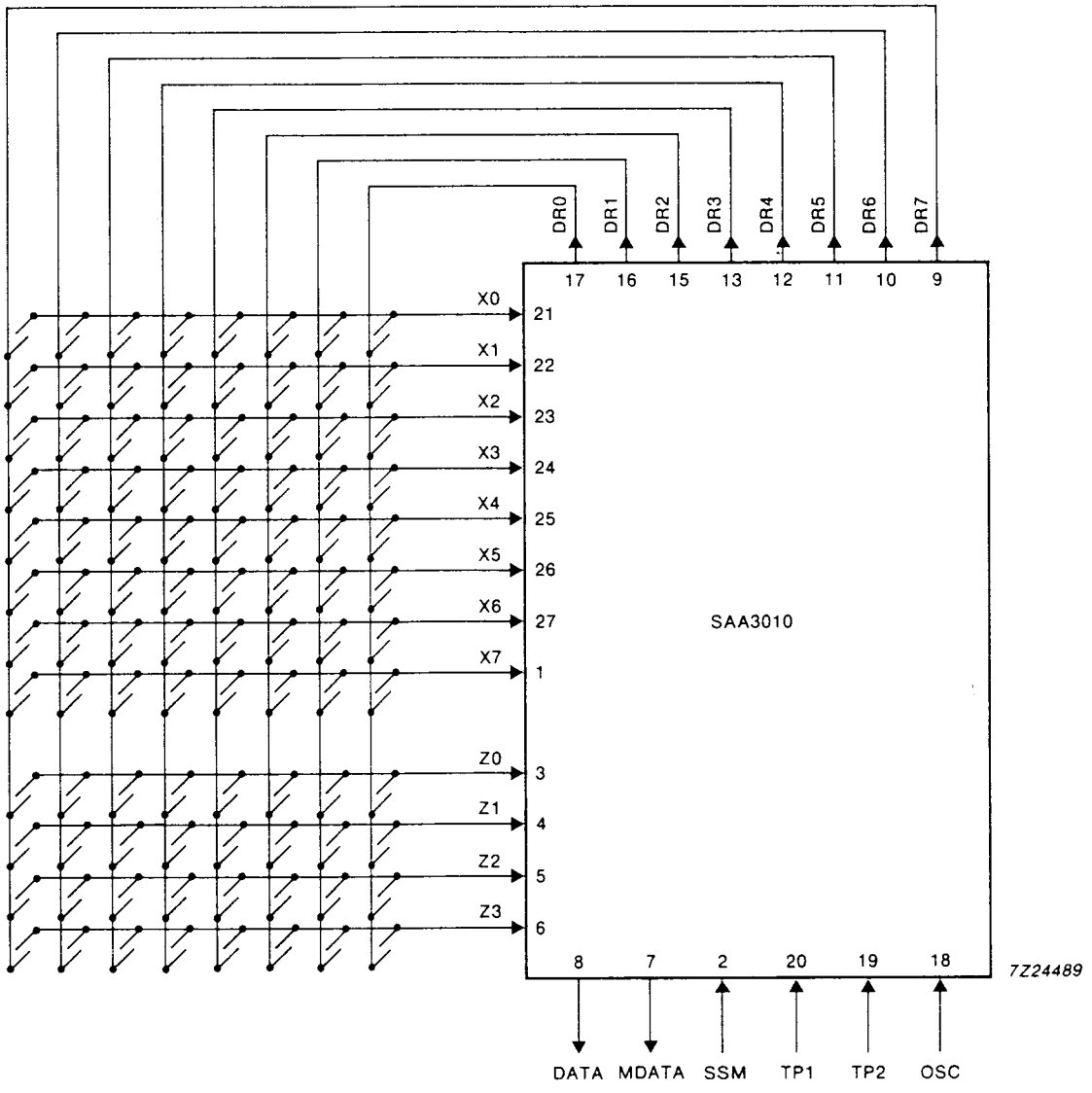


Fig.3 Keyboard interconnection.

FUNCTIONAL DESCRIPTION

Keyboard operation

Every connection of one X-input and one DR-output will be recognized as a legal key operation and will cause the device to generate the corresponding code. The same applies to every connection of one Z-input to one DR-output with the proviso that SSM must be LOW. When SSM is HIGH a wired connection must exist between a Z-input and a DR-output. If no connection is present the system number will not be generated. Activating two or more X-inputs, Z-inputs or Z-inputs and X-inputs at the same time is an illegal action and inhibits further activity (oscillator will not start).

When one X- or Z-input is connected to more than one DR-output, the last scan signal will be considered as legal.

The maximum value of the contact series resistance of the switched keyboard is 7 kΩ.

Inputs

In the quiescent state the command inputs X0 to X7 are held HIGH by an internal pull-up transistor. When the system mode selection (SSM) input is LOW and the system is quiescent, the system inputs Z0 to Z3 are also held HIGH by an internal pull-up transistor. When SSM is HIGH the pull-up transistor for the Z-inputs is switched off, in order to prevent current flow, and a wired connection in the Z-DR matrix provides the system number.

Outputs

The output signal DATA transmits the generated information in accordance with the format illustrated by Fig.4 and Tables 1 and 2. The code is transmitted using a biphase technique as illustrated by Fig.5. The code consists of four parts:

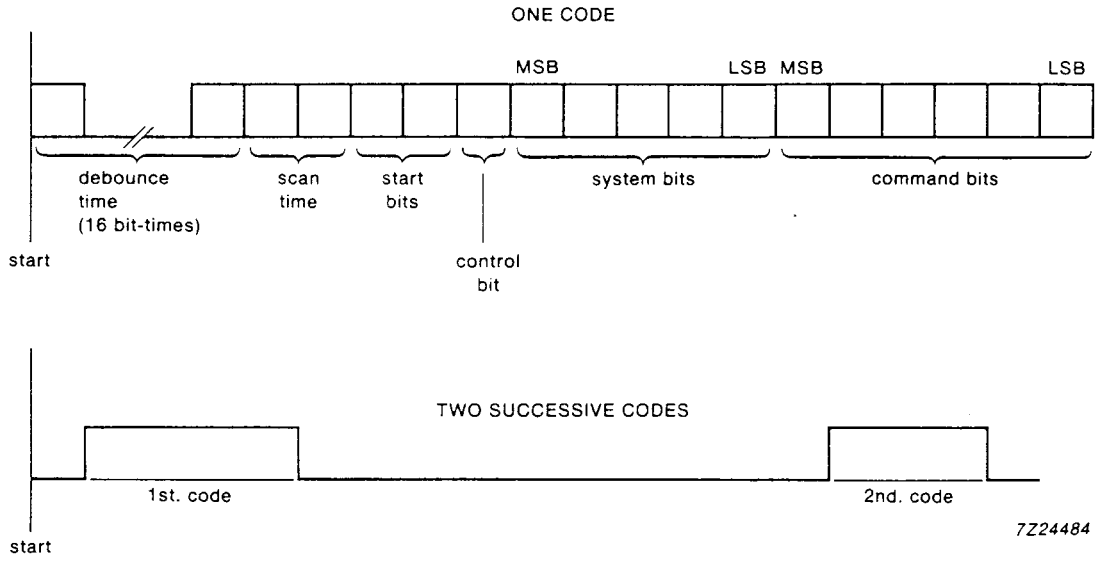
- Start part — 1.5 bits (2 x logic 1)
- Control part — 1 bit
- System part — 5 bits
- Command part — 6 bits

The output signal MDATA transmits the generated information modulated by 1/12 of the oscillator frequency with a 50% duty factor.

In the quiescent state both DATA and MDATA are non-conducting (3-state outputs).

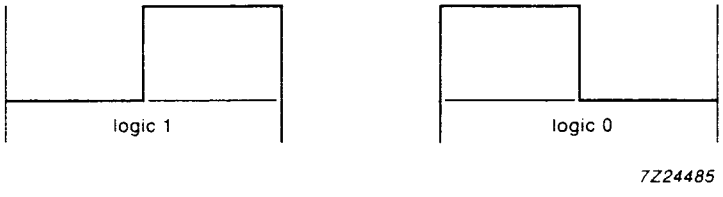
The scan driver outputs DR0 to DR7 are open drain n-channel transistors and conduct when the circuit is quiescent. After a legal key operation the scanning cycle is started and the outputs switched to the conductive state one by one. The DR-outputs were switched off at the end of the preceding debounce cycle.

FUNCTIONAL DESCRIPTION (continued)



Where: debounce time + scan time = 18 bit-times
repetition time = 4 x 16 bit-times

Fig.4 Data output format.



Where: 1 bit-time = $3.2^8 \times T_{OSC}$ = 1.778 ms (typ.)

Fig.5 Biphase transmission technique.

Table 1 Command matrix (X-DR)

code no.	X-lines 0 1 2 3 4 5 6 7	DR-lines 0 1 2 3 4 5 6 7	command bits 5 4 3 2 1 0
0	●	●	0 0 0 0 0 0
1	●	●	0 0 0 0 0 1
2	●	●	0 0 0 0 1 0
3	●	●	0 0 0 0 1 1
4	●	●	0 0 0 1 0 0
5	●	●	0 0 0 1 0 1
6	●	●	0 0 0 1 1 0
7	●	●	0 0 0 1 1 1
8	●	●	0 0 1 0 0 0
9	●	●	0 0 1 0 0 1
10	●	●	0 0 1 0 1 0
11	●	●	0 0 1 0 1 1
12	●	●	0 0 1 1 0 0
13	●	●	0 0 1 1 0 1
14	●	●	0 0 1 1 1 0
15	●	●	0 0 1 1 1 1
16	●	●	0 1 0 0 0 0
17	●	●	0 1 0 0 0 1
18	●	●	0 1 0 0 1 0
19	●	●	0 1 0 0 1 1
20	●	●	0 1 0 1 0 0
21	●	●	0 1 0 1 0 1
22	●	●	0 1 0 1 1 0
23	●	●	0 1 0 1 1 1
24	●	●	0 1 1 0 0 0
25	●	●	0 1 1 0 0 1
26	●	●	0 1 1 0 1 0
27	●	●	0 1 1 0 1 1
28	●	●	0 1 1 1 0 0
29	●	●	0 1 1 1 0 1
30	●	●	0 1 1 1 1 0
31	●	●	0 1 1 1 1 1

FUNCTIONAL DESCRIPTION (continued)

Table 1 Command matrix (X-DR) (continued)

code no.	X-lines 0 1 2 3 4 5 6 7	DR-lines 0 1 2 3 4 5 6 7	command bits 5 4 3 2 1 0
32	●	●	1 0 0 0 0 0
33	●	●	1 0 0 0 0 1
34	●	●	1 0 0 0 1 0
35	●	●	1 0 0 0 1 1
36	●	●	1 0 0 1 0 0
37	●	●	1 0 0 1 0 1
38	●	●	1 0 0 1 1 0
39	●	●	1 0 0 1 1 1
40	●	●	1 0 1 0 0 0
41	●	●	1 0 1 0 0 1
42	●	●	1 0 1 0 1 0
43	●	●	1 0 1 0 1 1
44	●	●	1 0 1 1 0 0
45	●	●	1 0 1 1 0 1
46	●	●	1 0 1 1 1 0
47	●	●	1 0 1 1 1 1
48	●	●	1 1 0 0 0 0
49	●	●	1 1 0 0 0 1
50	●	●	1 1 0 0 1 0
51	●	●	1 1 0 0 1 1
52	●	●	1 1 0 1 0 0
53	●	●	1 1 0 1 0 1
54	●	●	1 1 0 1 1 0
55	●	●	1 1 0 1 1 1
56	●	●	1 1 1 0 0 0
57	●	●	1 1 1 0 0 1
58	●	●	1 1 1 0 1 0
59	●	●	1 1 1 0 1 1
60	●	●	1 1 1 1 0 0
61	●	●	1 1 1 1 0 1
62	●	●	1 1 1 1 1 0
63	●	●	1 1 1 1 1 1

Table 2 System matrix (Z-DR)

syst. no.	Z-lines 0 1 2 3 4 5 6 7	DR-lines 0 1 2 3 4 5 6 7	system bits 4 3 2 1 0
0	●	●	0 0 0 0 0
1	●	●	0 0 0 0 1
2	●	●	0 0 0 1 0
3	●	●	0 0 0 1 1
4	●	●	0 0 1 0 0
5	●	●	0 0 1 0 1
6	●	●	0 0 1 1 0
7	●	●	0 0 1 1 1
8	●	●	0 1 0 0 0
9	●	●	0 1 0 0 1
10	●	●	0 1 0 1 0
11	●	●	0 1 0 1 1
12	●	●	0 1 1 0 0
13	●	●	0 1 1 0 1
14	●	●	0 1 1 1 0
15	●	●	0 1 1 1 1
16	●	●	1 0 0 0 0
17	●	●	1 0 0 0 1
18	●	●	1 0 0 1 0
19	●	●	1 0 0 1 1
20	●	●	1 0 1 0 0
21	●	●	1 0 1 0 1
22	●	●	1 0 1 1 0
23	●	●	1 0 1 1 1
24	●	●	1 1 0 0 0
25	●	●	1 1 0 0 1
26	●	●	1 1 0 1 0
27	●	●	1 1 0 1 1
28	●	●	1 1 1 0 0
29	●	●	1 1 1 0 1
30	●	●	1 1 1 1 0
31	●	●	1 1 1 1 1

FUNCTIONAL DESCRIPTION (continued)

Combined system mode (SSM is LOW)

The X and Z sense inputs have p-channel pull-up transistors, so that they are HIGH, until pulled LOW by connecting them to an output as the result of a key operation. Legal operation of a key in the X-DR or Z-DR matrix will start the debounce cycle, once key contact has been established for 18 bit-times without interruption, the oscillator enable signal is latched and the key may be released. An interruption within the 18 bit-time period resets the device.

At the end of the debounce cycle the DR-outputs are switched off and two scan cycles are started, that switch on the DR-lines one by one. When a Z- or X-input senses a low level, a latch enable signal is fed to the system (Z-input) or command (X-input) latches.

After latching a system number the device will generate the last command (i.e. all command bits logic 1) in the chosen system for as long as the key is operated. Latching of a command number causes the chip to generate this command together with the system number memorized in the system latch. Releasing the key will reset the device if no data is to be transmitted at the time. Once transmission has started the code will complete to the end.

Single system mode (SSM is HIGH)

In the single system mode, the X-inputs will be HIGH as in the combined system mode. The Z-inputs will be disabled by having their pull-up transistors switched off; a wired connection in the Z-DR matrix provides the system code. Only legal key operation in the X-DR matrix will start the debounce cycle, once key contact has been established for 18 bit-times without interruption the oscillator enable signal is latched and the key may be released. An interruption within the 18 bit-time period resets the internal action.

At the end of the debounce cycle the pull-up transistors in the X-lines are switched off and those in the Z-lines are switched on for the first scan cycle. The wired connection in the Z-matrix is then translated into a system number and memorized in the system latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again; the pull-up transistors in the X-lines are switched on. The second scan cycle produces the command number which, after being latched, is transmitted together with the system number.

Key release detection

An extra control bit is added which will be complemented after key release; this indicates to the decoder that the next code is a new command. This is important in the case where more digits need to be entered (channel numbers of Teletext or Viewdata pages). The control bit will only be complemented after the completion of at least one code transmission. The scan cycles are repeated before every code transmission, so that even with "take over" of key operation during code transmission the right system and command numbers are generated.

Reset action

The device will be reset immediately a key is released during:

- debounce time
- between two codes.

When a key is released during matrix scanning, a reset will occur if:

- a key is released while one of the driver outputs is in the low ohmic state (logic 0)
- a key is released before that key has been detected
- there is no wired connection in the Z-DR matrix when SSM is HIGH.

Oscillator

The OSC is the input/output for a 1-pin oscillator. The oscillator is formed by a ceramic resonator, TOKO CRK429, order code, 2422 540 98069 or equivalent. A resistor of 6.8 kΩ must be placed in series with the resonator. The resistor and resonator are grounded at one side.

Test

Initialization of the circuit is performed when TP1, TP2 and OSC are HIGH. All internal nodes are defined except for the LATCH. The latch is defined when a scan cycle is started by pulling down an X- or Z-input while the oscillator is running.

If the debounce cycle has been completed, the scan cycle can be completed 3×2^3 faster, by setting TP1 HIGH.

If the scan cycle has been completed, the contents of the latch can be read 3×2^7 faster by setting TP2 HIGH.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	8.5	V
Input voltage range *	V_I	−0.5	V_{DD}+0.5	V
Output voltage range *	V_O	−0.5	V_{DD}+0.5	V
Input current	I_I	−	±10	mA
Output current	I_O	−	±10	mA
Maximum power dissipation				
OSC output	P_O	−	50	mW
other outputs	P_O	−	100	mW
Total power dissipation	P_{tot}	−	200	mW
Operating ambient temperature range	T_{amb}	−25	+ 85	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

* V_{DD}+0.5 V must not exceed 9.0 V.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DC CHARACTERISTICS

T_{amb} = −25 °C to + 70 °C; V_{DD} = 2.0 to 7.0 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2.0	–	7.0	V
Quiescent supply current	note 1 T_{amb} = 25 °C; I_O = 0 mA at all outputs. X0 to X7 and Z0 to Z3 at V_{DD} TP1, TP2, OSC at V_{SS} SSM at V_{SS} or V_{DD}	I_{DD}	–	–	10	μA
INPUTS						
Keyboard inputs X and Z with p-channel pull-up transistor						
Input current at each input	V_I = 0 V; TP1 = TP2 = SSM = LOW	$-I_I$	10	–	600	μA
Input voltage HIGH	note 2	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW	note 2	V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current	T_{amb} = 25 °C; V_I = 7 V; TP1 = TP2 = HIGH	I_{LI}	–	–	1	μA
Input leakage current	T_{amb} = 25 °C; V_I = 0 V; TP1 = TP2 = HIGH	$-I_{LI}$	–	–	1	μA
OSC						
Input leakage current	T_{amb} = 25 °C; V_I = 0 V; TP1 = TP2 = HIGH	$-I_{LI}$	–	–	2	μA
Input current	T_{amb} = 25 °C; V_I = V_{DD}	I_{OSC}	4.5	–	30	μA
SSM, TP1, TP2						
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW		V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current	T_{amb} = 25 °C; V_I = 7.0 V	I_{LI}	–	–	1	μA
Input leakage current	T_{amb} = 25 °C; V_I = 0 V	$-I_{LI}$	–	–	1	μA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
OUTPUTS						
DATA, MDATA						
Output voltage HIGH	$I_{OH} = -0.4$ mA	V_{OH}	$V_{DD}-0.3$	–	–	V
Output voltage LOW	$I_{OL} = 0.6$ mA	V_{OL}	–	–	0.3	V
Output leakage current	$V_O = 7.0$ V	$+I_{LO}$	–	–	10	μA
	$V_O = 7.0$ V; $T_{amb} = 25\ ^oC$	$+I_{LO}$	–	–	1	μA
	$V_O = 0$ V	$-I_{LO}$	–	–	20	μA
	$V_O = 0$ V; $T_{amb} = 25\ ^oC$	$-I_{LO}$	–	–	2	μA
DR0 to DR7						
Output voltage LOW	$I_{OL} = 0.3$ mA	V_{OL}	–	–	0.3	V
Output leakage current	$V_O = 7.0$ V	$+I_{LO}$	–	–	10	μA
	$V_O = 7.0$ V; $T_{amb} = 25\ ^oC$	$+I_{LO}$	–	–	1	μA

Notes to the DC characteristics

1. Quiescent supply current measurement must be preceded by the initialization procedure described in the **TEST** section.
2. This DC test condition protects the AC performance of the output. The DC current requirements in the actual application are lower.

AC CHARACTERISTICS

T_{amb} = −25 to + 85 °C; V_{DD} = 2.0 to 7.0 V unless otherwise stated

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency	C_L = 160 pF; Figs 6 and 7					
operational		f_{OSC}	–	–	450	kHz
free-running		f_{OSC}	10	–	120	kHz

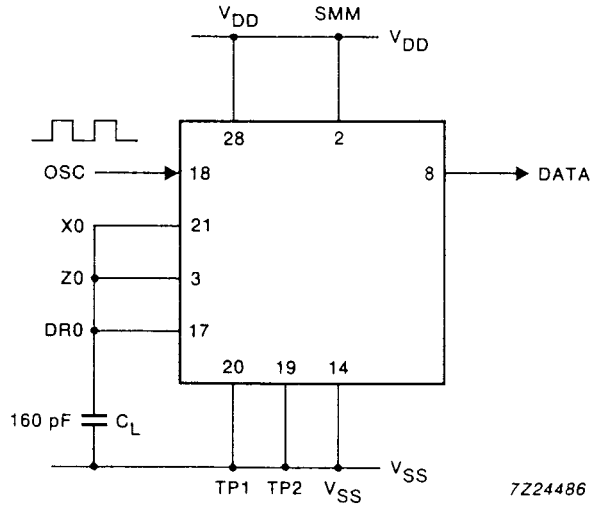


Fig.6 Test set-up for maximum f_{OSC} measurement.

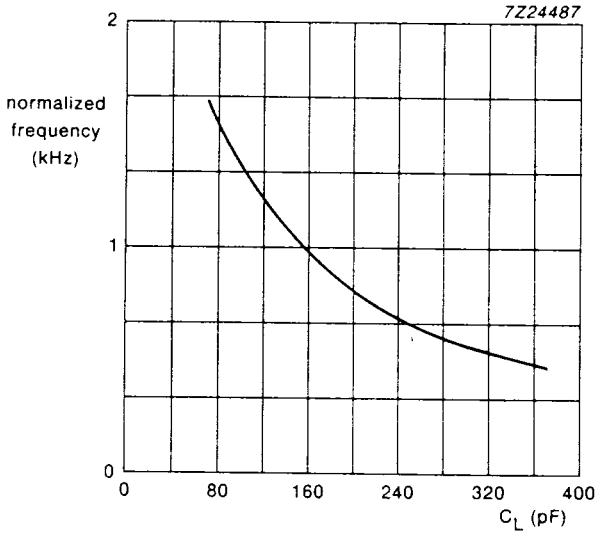


Fig.7 Typical normalized frequency as a function of keyboard load capacitance.