VTC Inc.
Value the Customer™

VM7750/VM7750F

2, 4, 6 OR 8-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER WITH MULTIPLE SERVO WRITE CAPABILITY

950801

PRELIMINARY

August, 1995

FEATURES

- High Performance
  - Read Gain = 300 V/V Typical
  - Input Noise = 0.49nV/$\sqrt{Hz}$ Typical
  - Head Inductance Range = 0.2 – 1 µH (0.54 µH Typical)
  - IW Rise/Fall Times = 3.5 ns (L_H = 0.54 µH, I_W = 10 mA b-p)
  - Write Current Range 5 - 20 mA
  - Low Input Capacitance = 11 pF Typical
- PECL Write Data Inputs
- Multi-Channel Servo Write
- Very Low Power Dissipation = 3 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Single Power Supply = 5 V ± 10%
- Write Unsafe Detection
- Reduced Write-to-Read Recovery Time
- Write Data Flip-Flop Optional
- Available in 2, 4, 6 or 8-Channels

DESCRIPTION

The VM7750/VM7750F is a high-performance read/write preamplifier designed for use in high-end disk drives. It provides write current control, data protection circuitry, and a low-noise read preamplifier for up to eight channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 3mW.

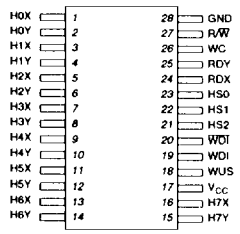
Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in write mode.

Very low-power dissipation from the +5V supply is achieved through use of high-speed bipolar processing and innovative circuit design techniques.

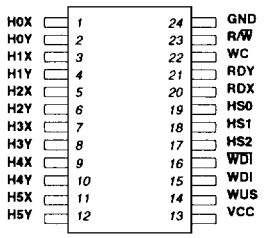
In multi-channel servo write mode, multiple heads can be written simultaneously. The VM7750/VM7750F servo mode is activated via the WUS line and, when active, write all heads simultaneously.

The VM7750/VM7750F is available in several different packages. Please contact VTC for package availability.

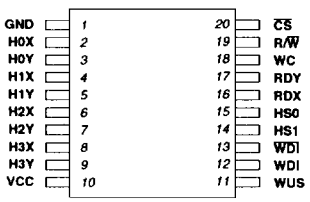
CONNECTION DIAGRAMS



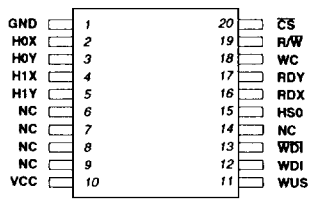
8-Channel
28-lead SSOP



6-Channel
24-lead SSOP

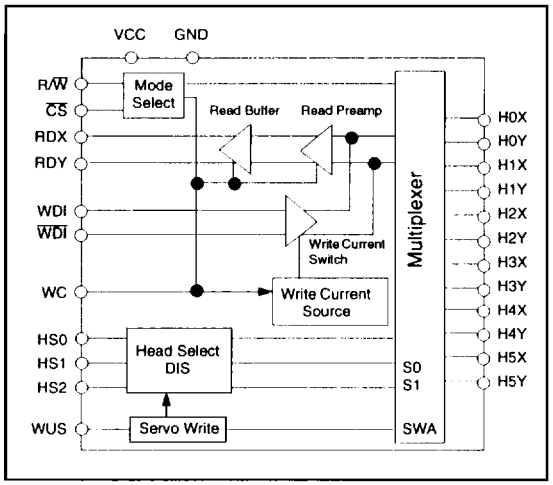


4-Channel
20-lead SOIC, SSOP



2-Channel
20-lead SSOP

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current I_W 30mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature Tstg ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 20-lead SOIC ..... 90°C/W
- 20-lead SSOP ..... 110°C/W
- 24-lead SSOP ..... 100°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%

Write current (I_W) ..... 5 to 20mA

Head Inductance (L_H) ..... 0.2 to 1µH

Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM7750/VM7750F addresses up to eight two-terminal thin-film heads, providing write drive or read amplification. Mode control is accomplished with pins $\overline{CS}$ and R/$\overline{W}$, as shown in Table 1. Table 2 shows the head select during normal (single head) write mode. Internal resistor pull-high provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

VM7750F: The write mode configures this part as a current switch and activates the write unsafe (WUS) detection circuitry.

On the VM7750F (no write data flip-flop), write current is toggled between the X and Y direction of a selected head on each transition on pins WDI (write data inputs). On the high-to-low transition of WDI, current goes into H0Y. On the high-to-low transition of $\overline{WDI}$, current goes into H0X.

VM7750: On the VM7750 (with write data flip-flop on chip), write current is toggled with the rising edge of WDI-$\overline{WDI}$ (see Figure 2)

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally-generated 2.5 V reference voltage is present at the WC pin. The magnitude of the write current (0-pk ±10%) is:

$$I_W = K_W/R_{WC} + 0.3mA = (50/R_{WC}) + 0.3mA \quad \textit{(eq. 2)}$$

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power-up. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin WUS. Two transitions on pin WDI, after the fault is corrected,may be required to clear the WUS flag.

- No write current
- WDI frequency too low
- Device in read or sleep mode

Multi-Channel Servo Write Mode

In this mode, the operation is the same as described above except that multiple channels are written at the same time (see tables 1 - 3). Servo mode is controlled using the WUS pin. To initiate servo mode the following procedure is used:

1. Enter read mode via R/$\overline{W}$ high
2. Select Head 1
3. Pull WUS pin to VCC + 1.9V thru 1k resistor
4. Drop the R/$\overline{W}$ line to low

The device is now in servo mode with all heads writing at the same time. If any other head is selected during servo the part will only write selected head. (i.e. part will fall out of servo.) To return to normal operations the following sequence is used:

1. Enter read mode
2. Drop the WUS pin (the device is in normal read mode)
3. Will also occur if any head except head 1 is selected, but will return to servo mode if HDI is reselected

Read Mode

The read mode configures the VM7750/VM7750F as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC-coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between the write mode and the read mode, thereby substantially reducing the recovery time delay to the subsequent pulse detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to 3mW typical for sleep mode, In sleep mode, the reader outputs are high impedance. This allows multiple chip connection by simply wiring the reader outputs together.

Table 21: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
0	0	Servo
1	0	Read
X	1	Idle

Table 22: Head Selection

HS2	*HS1*	*HS0*	*HEAD*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS2	I*	Head Select: selects one of up to six heads
H0X - H5X H0Y - H5Y	I/O	X, Y Head Terminals
WDI, $\overline{WDI}$	I*	Write Data Inputs: PECL input signal, rising edge toggles direction of head current. (every transition on "F" option)
$\overline{CS}$	I	Chip select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write select: high level selects read mode, low-level indicates write mode
WUS	O*	Write unsafe: open collector output, high level indicates writes unsafe condition/also used during servo
WC		Write Current Adjust: a resistor adjusts level of write current
RDX-RDY	O*	Read Data Output: differential output data
VCC		+5 volt supply
GND		Ground

* May be wire-OR'ed for multi-chip usage.

DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Voltage	V_{CC}	Servo Mode	4.5	5.0	5.5	mA
VCC Supply Current	I_{CC}	Read Mode		$28 + 0.05I_W$	40	mA
		Write Mode, I_W = 10mA, Normal		$26 + 1.05I_W$	43	
		Write Mode, Servo (4-Channel)		$55 + 4.3I_W$	115	
		Write Mode, Servo (6-Channel)		$70 + 6.5I_W$	155	
		Sleep Mode		0.5	3	
Power Supply Power Dissipation	PD	Read Mode		155	210	mW
		Write Mode, I_W = 10mA, Normal		200	240	
		Write Mode, Servo, I_W = 10mA (4-Channel)		490	633	
		Write Mode, Servo, I_W = 10mA (6-Channel)		675	853	
		Sleep Mode		3	16.5	
Input High Voltage	V_{IH}		2		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3		0.7	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160			µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.5		V_{CC} - 0.5	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{IH} - 1.5		V_{IH} - 0.5	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	$V_{IH} = V_{CC}$ - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	$V_{IH} = V_{CC}$ - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.3	3.6	4.0	V
WUS Servo Enable				V_{CC} +1.9		

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WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; L_H = 0.54µH, R_H = 20Ω, I_W = 10mA, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* (Note 1)	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}		2.2	2.5	2.9	V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	V_{CC} = 5V ±10%	46	50	54	V
Write Current Range	I_W	10.64ΩK > R_{WC} > 2.54KΩ	5		20	mA
Write Current Tolerance	ΔI_W	V_{CC} ±10%	-10		+10	%
Write Current Tolerance Servo	ΔI_W	V_{CC} ±10%	-14		+14	
Differential Head Voltage Swing	V_{DH}	Open head	5.7	6.4		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
Unselected Head Current	I_{UH}	I_W = 20mA		0.15	0.5	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

Servo Write

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Matching Between Channels	ΔI_W	5mA < I_W < 20mA			10	%
Duty Cycle (15mA/head)					20	%
WUS Input Current During Servo Write	I_{WUSS}	Thru 1k resistor			20	mA

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	SYM	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	258	300	342	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	35			MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p	65			
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.49	0.65	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		11	15	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	380	700		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45			dB
Channel Separation	CS	Unselected channels: V_{IN} = 20mVp-p @ 5MHz V_{IN} = 0 on selected head	45			dB
Output Offset Voltage	V_{OS}	Steady state read	-250		250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read/Write Mode		V_{CC} - 2.7		
RDX, RDY Common Mode Output Voltage Difference Between Modes	ΔV_{OCM}		-350		+350	mV
Single-Ended Output Resistance	R_{SEO}	f = MHz			35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 10mA, f_{DATA} = 5MHz, L_H = 0.54µH, R_H = 20Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	SYM	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.1	0.3	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.3	0.5	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W			0.6	µs
HS0 - HS3 any Head Delay	t_{HS}	HS0 - HS3 to 90% of 100mV, 10MHz read signal envelope			0.6	µs

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 10mA, f_{DATA} = 5MHz, L_H = 0.54µH, R_H = 20Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* *(Note 1)*	*MAX*	*UNITS*
WUS Safe to Unsafe Delay	t_{D1}		0.6		3.6	µs
WUS Unsafe to Safe Delay	t_{D2}	I_W = 10mA			1.0	µs
Head Current Propagation	t_{D3}	L_H = 0, R_H = 0, from 50% points			30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0			0.5	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		1.5	4	ns
		10% to 90% points, L_H = 540nH, I_W = 10mA, R_H = 20Ω		3.5	7	

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

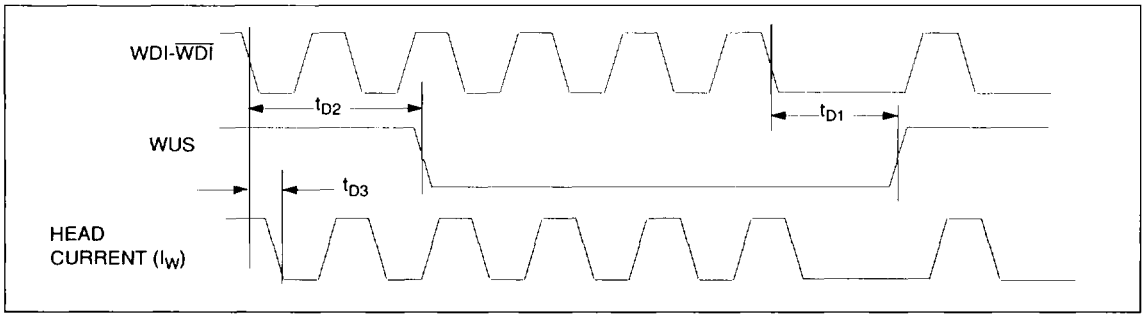

Figure 1: Write Mode Timing Diagram for VM7750F

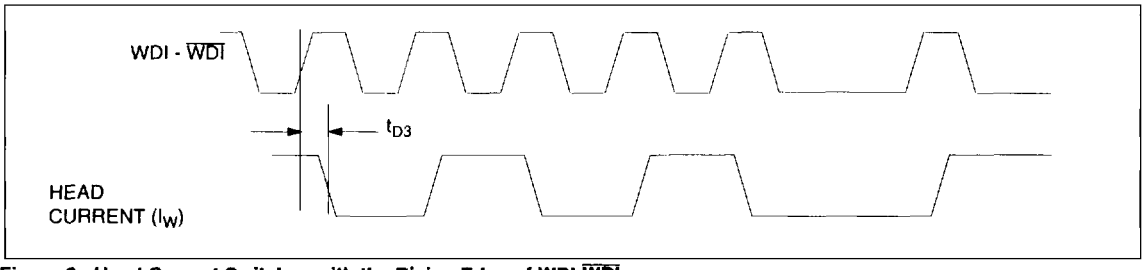

Figure 2: Head Current Switches with the Rising Edge of WDI-$\overline{WDI}$