# ALDC

## ALDC1-40S-M Data Sheet

Product Part Number: IBM22-ALDC1040S-00
Document Number: DCAL40DSU-02

November 2, 1994

**ALDC1-40S-M Design Notes**

1. Software Reset

   Software Reset (CMND equals X'A000') will not reset the ALDC Decoder Control Code Error (ERRS(1)) or the ALDC Decoder End Error (ERRS(0)).

   Recommendations:

   - A Start Decompression (CMND equals X'6800') or Start Decompression Output Disabled (CMND equals X'6C00') followed immediately by a Software Reset (CMND equals X'A000') will reset these errors.
   - Or, a Hardware Reset will reset these errors.

2. Peripheral Access Read When +M1BYTE is Tied High

   +MDATA(07:00) will equal X'00' for peripheral access reads on odd addresses (+ADDR(0) high) when +M1BYTE is tied high.

   Recommendation:

   - Force ALDC1-40S-M +ADDR(0) low using external logic if necessary to read a peripheral device under these conditions.

3. Recommended Use of the Busy Status Bit (STAT(7))

   The ALDC1-40S-M is in the Busy state whenever STAT(7)='1'B and both the Done and Any-Error status bits (STAT(0:1)) are equal to '0'B.

   Avoid writing opcodes other than Hold and Software Reset into the CMND register while the ALDC1-40S-M is in the Busy state.

# Contents

# Chapter 1. Product Overview

**ALDC** stands for **A**daptive, **L**ossless, **D**ata **C**ompression.

The ALDC1-40S-M is a low cost, high speed data compression product for use in data storage and data transmission applications. Using the ALDC compression algorithm, ALDC1-40S-M can achieve an average compression ratio of approximately 3:1. Many applications can use the flexible ALDC1-40S-M hardware interface. Also, ALDC1-40S-M's hardware interface allows growth capability for the future.

## 1.1 Distinctive Features

- ALDC1-40S-M has a single clock input.
- ALDC1-40S-M interfaces with common TTL and CMOS/TTL circuits.
- ALDC1-40S-M requires no additional external memory -- it is a single chip data compression solution.
- ALDC1-40S-M operates at sustained speeds up to 40 MB/s. Compression and decompression data rates are symmetrical.
- ALDC1-40S-M compresses and decompresses data blocks up to 4,294,967,295 bytes.
- ALDC1-40S-M provides a flexible microprocessor interface to the controlling microprocessor.
- The microprocessor interface supports both polling-driven and interrupt-driven applications.
- The original data interface and compressed data interface are independently configurable interfaces.
- The original data interface and compressed data interface contain independently configurable sixteen-byte FIFO buffers.
- The original data interface and compressed data interface both support configurable eight-bit peripheral access transfers to and from the microprocessor interface.

## 1.2 Package

ALDC1-40S-M is designed in IBM CMOS 0.8 micron triple-level metal gate array/standard cell technology.

- The ALDC1-40S-M has a 28 mm x 28 mm x 3.8 mm body size. It is a 144-lead plastic flat package with molded heat sink. It has 0.65 mm lead spacing.

Section Chapter 7 on page 7-1 gives the detailed physical dimension information. Other packaging options are available to suit application and system requirements.

## 1.3 Part Number

Your IBM Marketing Representative will help you obtain the ALDC1-40S-M. The IBM Original Equipment Manufacturer (OEM) catalog number for ALDC1-40S-M is **IBM22-ALDC1040S-00**.

The ALDC1-40S-M IBM part number is 63G9792.

## 1.4 Quality

The ALDC1-40S-M Acceptable Quality Level (AQL) is 50 PPM or less. Customers with different requirements should contact your IBM Marketing Representative.

Customers should return any module believed to be defective. IBM will replace any module confirmed defective by our manufacturing tests. We encourage you to return defective modules. The failure analysis results obtained from these modules help us to improve the quality of our products.

### 1.4.1 Reliability

The reliability objective is an end-of-life Average Failure Rate (AFR) equal to or less than 100 PPM/KPOH at nominal temperature and voltage conditions. This includes an Early Failure Rate (EFR) contribution equal to or less than 250 PPM/KPOH. Customers with different requirements should contact your IBM Marketing Representative.

# Chapter 2. Functional Description

ALDC1-40S-M provides a microprocessor interface, an original data interface, a compressed data interface, and a clock input.

Internal to ALDC1-40S-M are the ALDC encoder, ALDC decoder, and the ALDC1-40S-M registers.

Figure 2-1 illustrates these functional areas.

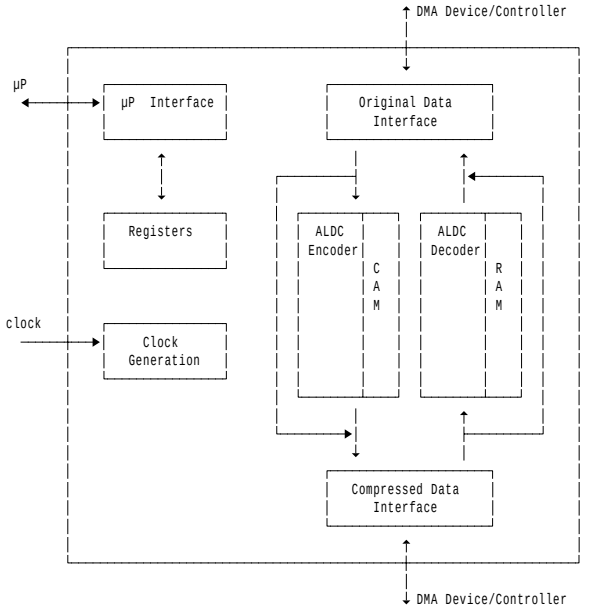



Figure 2-1. ALDC1-40S-M High-level Functional Units

## 2.1 Functional Areas

### 2.1.1 Microprocessor Interface

The microprocessor interface allows a microprocessor to query status and control ALDC1-40S-M. The ALDC1-40S-M registers are externally accessible through the microprocessor interface. These registers provide the primary means by which ALDC1-40S-M and the microprocessor communicate.

Section 4.2 on page 4-1 describes the microprocessor interface timing in detail. Section 3.1 on page 3-1 describes the ALDC1-40S-M registers in detail.

### 2.1.2 Original Data Interface and Compressed Data Interface

The original data interface and compressed data interface are identically designed. They are always discussed together in this document.

The original data interface accepts data for compression and provides decompressed data to the bus connected to it. The compressed data interface accepts compressed data for decompression from the bus connected to it. It provides compressed data to its bus.

The original data interface counts the bytes of original data received during compression operations and the bytes of decompressed data sent during decompression operations. This count is available in the Original Data Interface Transfer Count (TCO) register.

The compressed data interface counts the bytes of compressed data received during decompression operations and the bytes of compressed data sent during compression operations. This count is available in the Compressed Data Interface Transfer Count (TCC) register.

The original data interface and compressed data interface both buffer data during data transfer operations in sixteen-byte FIFO's.

Section 4.3 on page 4-8 describes the original data interface and compressed data interface in detail.

### 2.1.3 Clock Generation

The clock generation circuitry accepts a single clock input. It generates all internal clocks necessary for ALDC1-40S-M to function.

Section 4.4 on page 4-29 describes the clock timing in detail.

### 2.1.4 ALDC Encoder

The ALDC encoder accepts data bytes from the original data interface and provides compressed data bytes to the compressed data interface. The ALDC implementation of the adaptive Lempel-Ziv lossless compression algorithm accomplishes this function.

The ALDC encoder contains a 512-byte content addressable memory (CAM). The CAM is the history buffer during compression operations.

The ALDC encoder concatenates an end marker control code to the end of the compressed data. It also pads any remaining bits with zeros to align evenly on a byte boundary.

### 2.1.5 ALDC Decoder

The ALDC decoder accepts compressed data bytes from the compressed data interface and provides the reconstructed data bytes to the original data interface. The ALDC implementation of the adaptive Lempel-Ziv lossless compression algorithm accomplishes this function.

The ALDC decoder contains a 512-byte random access memory (RAM). The RAM is the history buffer during decompression operations.

The ALDC decoder expects to find an end marker control code in the final data received from the compressed data interface. If it does not detect the end marker control code, then it asserts an ALDC decoder end error. If it detects the end marker control code, then it strips the end marker control code from the decompressed data stream.

## 2.2 Data Transfer Operations

The data transfer operations describe how data may be transferred between the original data interface and the compressed data interface. The microprocessor interface controls the internal sequencing of ALDC1-40S-M to accomplish the data transfer operations. The data transfer operations are started when the appropriate data transfer command is decoded in the command register.

Data transfer operations typically involve blocks of data bytes. These blocks may either have fixed or variable length depending on the desired application. The transfer size in bytes is loaded into the appropriate microprocessor interface register. The transfer proceeds until the specified number of bytes are processed, a hardware or software reset occurs, an error occurs, or a hold opcode occurs.

After a data transfer operation has ended (either successfully or unsuccessfully), the microprocessor prepares ALDC1-40S-M for the next data transfer operation.

**Note:** Interrupts may be disabled by setting the ALDC1-40S-M Interrupt Mask register to X'FFFF'. If interrupts are disabled, then the microprocessor must poll the correct status bits to determine the progress and outcome of a data transfer operation.

### 2.2.1 General Data Transfer Sequencing

This is the general control sequence which occurs during data transfer operations:

1. The history buffer is cleared, the transfer count registers are reset to X'000000', the error status register is reset to X'0000', and the status register is set to X'0080' (ie. Busy).
2. The original data interface and compressed data interface are enabled to send and receive data as appropriate. Also, the encoder or decoder bypass paths are set up as appropriate.
3. Data is received and processed until the end of data is reached. During processing, the output data is sent as it becomes available.
4. When the end of data is reached at the sending interface, the interrupt outputs are asserted and the Done (STAT(0)) bit is set to B'1'.

**Exception Conditions:** The following exception conditions may prevent the general data transfer sequence from completing:

- If an error occurs during the data transfer operation, then the interrupt output is immediately asserted; the Any Error (STAT(1)) bit is set to B'1'; the proper bit in the error status (ERRS) register is also set to B'1'; and the transfer is ended. Depending on the type of error, the microprocessor may attempt to retry the current

transfer, reset ALDC1-40S-M (and retry the transfer), and/or report the failure.

- If a hold opcode occurs during a data transfer operation, then the interrupt output is asserted and Hold (STAT(6)) bit is set to B'1' after the current processing step. The microprocessor may at a later time issue a resume opcode to continue the data transfer operation.

  **Note:** A resume opcode must come directly after a hold opcode.

- If a hardware reset or a reset opcode occurs during a data transfer operation, then the history buffer is cleared, the microprocessor interface registers are reset to X'0000' as appropriate, and the transfer is ended.

### 2.2.2 Start Compression Bypass

The original data interface receives data from the external original data bus and sends it to the encoder bypass. The encoder bypass sends the data without modification to the compressed data interface. The compressed data interface sends the original data to the external compressed data bus.

### 2.2.3 Start Compression

The original data interface receives data from the external original data bus and sends it to the encoder bypass. The encoder bypass sends the data to the ALDC encoder. The ALDC encoder compresses the data and sends it to the encoder bypass (using a different port). The encoder bypass sends the compressed data to the compressed data interface. The compressed data interface sends the compressed data to the external compressed data bus.

### 2.2.4 Start Decompression Bypass

The compressed data interface receives data from the external compressed data bus and sends it to the decoder bypass. The decoder bypass sends the data without modification to the original data interface. The original data interface sends the unaltered data to the external original data bus.

### 2.2.5 Start Decompression

The compressed data interface receives compressed data from the external compressed data bus and sends it to the decoder bypass. The decoder bypass sends the data to the ALDC decoder. The ALDC decoder decompresses the data and sends it to the decoder bypass (using a different port). The decoder bypass sends the decompressed data to the original data interface. The original data interface sends the decompressed data to the external original data bus.

### 2.2.6 Start Decompression Output Disabled

The compressed data interface receives compressed data from the external compressed data bus and sends it to the decoder bypass. The decoder bypass sends the data to the ALDC decoder. The ALDC decoder decompresses the data and sends it to the decoder bypass (using a different port). The decoder bypass sends the decompressed data to the original data interface. The original data interface counts decompressed bytes but does not send the decompressed data to the external original data bus until the Original Data Interface Transfer Count (TCO) register is greater than the Data Disable Count (DDC) register. When TCO is greater than DDC, the original data interface sends the remaining decompressed data to the external original data bus.

**Note:** If OCNF(10) is set to B'1' and DDC is an odd number, then when TCO *equals* DDC the original data interface sends the remaining decompressed data to the external original data bus. This is done to maintain proper byte alignment.

# Chapter 3. Microprocessor Interface

## 3.1 Registers

Each register is two bytes wide.

When +M1BYTE is tied low, +ADDR(0) is not used. Data is read and written using +MDATA(15:00).

When +M1BYTE is tied high, +ADDR(0) is used to select the eight bits which will be read or written on +MDATA(07:00). In this case, when +ADDR(0) equals B'0' then the eight least significant register bits (7 through 0) are read or written. When +ADDR(0) equals B'1', then the eight most significant register bits (15 through 8) are read or written.

Figure 3-1 (Page 1 of 2). Register Summary

| +ADDR(4:1) | MNEMONIC | REGISTER NAME | PAGE | R/ W |
|---|---|---|---|---|
| X'0' | STAT | Status (See note 1.) | 3-2 | R |
| | OCNF | Original Data Interface Configuration (See note 2.) | 3-3 | R/ W |
| | CCNF | Compressed Data Interface Configuration (See note 3.) | 3-3 | R/ W |
| X'1' | ECL | EC Level (See note 1.) | 3-4 | R |
| | OPOL | Original Data Interface Polarity (See note 2.) | 3-5 | R/ W |
| | CPOL | Compressed Data Interface Polarity (See note 3.) | 3-5 | R/ W |
| X'2' | TCOH | Original Data Interface Transfer Count High (See note 1.) | 3-5 | R |
| X'3' | TCOL | Original Data Interface Transfer Count Low (See note 1.) | 3-5 | R |
| X'4' | TCCH | Compressed Data Interface Transfer Count High (See note 1.) | 3-6 | R |
| X'5' | TCCL | Compressed Data Interface Transfer Count Low (See note 1.) | 3-6 | R |
| X'6' | ERRS | Error Status (See note 1.) | 3-7 | R |
| X'7' | INTS | Interrupt Status (See note 1.) | 3-8 | R |
| X'8' | CMND | Command | 3-8 | R/ W |
| X'9' | | Reserved | | |
| X'A' | XFRH | Transfer Size High | 3-10 | R/ W |
| X'B' | XFRL | Transfer Size Low | 3-10 | R/ W |
| X'C' | DDCH | Data Disabled Count High | 3-10 | R/ W |
| X'D' | DDCL | Data Disabled Count Low | 3-10 | R/ W |
| X'E' | EMSK | Error Mask | 3-11 | R/ W |

Figure 3-1 (Page 2 of 2). Register Summary

| +ADDR(4:1) | MNEMONIC | REGISTER NAME | PAGE | R/ W |
|---|---|---|---|---|
| X'F' | IMSK | Interrupt Mask | 3-12 | R/ W |

**Notes:**

1. When CMND is not equal to X'C100', X'C200', X'C400', or X'C800'.
2. When CMND equals X'C100'.
3. When CMND equals X'C200'.

### 3.1.1 Status (STAT)

The Status register provides status bits to the microprocessor. STAT is reset to X'0000' by a hardware or software reset.

This register is only accessable when CMND is not equal to X'C100', X'C200', X'C400', or X'C800'.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'0' to read STAT.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'00' to read STAT(7:0); and +ADDR(4:0) equals X'01' to read STAT(15:8).

Figure 3-2 (Page 1 of 2). STAT

| BIT | NAME/NOTES |
|---|---|
| 15:8 | Reserved |
| 7 | Busy<br>This bit is set to B'1' when a data transfer operation is initiated by the microprocessor. It is reset to B'0' when the data transfer operation completes successfully, when an unmasked error occurs, when a reset occurs, or when a hold opcode is issued by the microprocessor.<br>**Important!**<br>See ALDC1-40S-M Design Note 3 on page ii. |
| 6 | Hold<br>This bit is set to B'1' when a data transfer operation is currently held. It is reset to B'0' when a held data transfer operation is resumed or when a reset occurs. |

Figure 3-2 (Page 1 of 2). STAT

| BIT | NAME/NOTES |
|---|---|
| 5 | Output Disabled<br>This bit is set to B'1' when original data interface output is disabled. It is reset to B'0' when original data interface output is re-enabled or when a reset occurs.<br>**Note:** The Start Decompression Output Disabled (CMND equals X'6C00') opcode and the Data Disabled Count (DDC) register are used to control original data interface output disabling. |
| 4 | Bypass<br>This bit is set to B'1' when compression and decompression are disabled. It is reset to B'0' when compression and decompression are re-enabled or when a reset occurs.<br>**Note:** The Start Compression Bypass (CMND equals X'5000') and Start Decompression Bypass (CMND equals X'6000') opcodes are used to control compression and decompression disabling. |
| 3 | Expansion<br>This bit is set to B'1' when the Compressed Data Interface Transfer Count (TCC) register is larger than the Transfer Size (XFR) register at the end of a compression operation. It is reset to B'0' when another data transfer operation begins or when a reset occurs.<br>See section 3.4 on page 3-13 for a discussion of data expansion. |

| Figure 3-2 (Page 2 of 2). STAT | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 2 | Any Interrupt<br>This bit is set to B'1' when an **unmasked** interrupt occurs. It is reset to B'0' when a data transfer operation begins or when a reset occurs.<br>**Notes:**<br>1. The Interrupt Status (INTS) register is used to determine the cause of the interrupt.<br>2. The Interrupt Mask (IMSK) register is used to control which interrupts are masked. |
| 1 | Any Error<br>This bit is set to B'1' when an **unmasked** error occurs. It is reset to B'0' when a data transfer operation begins or when a reset occurs.<br>**Notes:**<br>1. The Error Status (ERRS) register is used to determine the cause of the error.<br>2. The Error Mask (EMSK) register is used to control which errors are masked. |
| 0 | Done<br>This bit is set to B'1' when the current data transfer operation is complete. It is reset to B'0' when a new data transfer operation begins or when a reset occurs. |

## 3.1.2 Original Data Interface Configuration (OCNF) and Compressed Data Interface Configuration (CCNF)

The Original Data Interface Configuration register provides original data interface configuration capability to the microprocessor. The Compressed Data Interface Configuration register provides compressed data interface configuration capability to the microprocessor. OCNF and CCNF are reset to X'0000' by a hardware reset.

OCNF is only accessable when CMND is equal to X'C100'; CCNF when CMND is equal to X'C200'.

**Note:** The Original Data Interface Configuration (OCNF) and the Compressed Data Interface Configuration (CCNF) registers are independently configurable. In the discussion below, these registers are called the **xCNF** register, where the "x" is replaced by "O" only or "C" only, as appropriate.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'0' to read and write xCNF.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'00' to read and write xCNF(7:0); and +ADDR(4:0) equals X'01' to read and write xCNF(15:8).

| Figure 3-3 (Page 1 of 2). xCNF | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 15 | Parity<br>When set to a B'1', parity checking is enabled for the +xDATA(15:00) data bus. When reset to a B'0', parity checking is disabled for the +xDATA(15:00) data bus.<br>**Notes:**<br>1. The Odd (xCNF(14)) bit determines if odd or even parity is used.<br>2. The Two Byte (xCNF(10)) bit determines if parity is checked and generated only on +xPARITY(0) (for +xDATA(07:00)) or on both +xPARITY(1:0) (for +xDATA(15:00)). |
| 14 | Odd<br>When set to a B'1', odd parity checking and generation is used on the +xDATA(15:00) data bus. When reset to a B'0', even parity checking and generation is used on the +xDATA(15:00) data bus.<br>**Note:** This bit only has meaning if the Parity (xCNF(15)) bit is set to B'1'. |

| Figure 3-3 (Page 2 of 2). xCNF | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 13 | Controller<br>When set to a B'1', the original data interface (or compressed data interface) acts as a controller. When reset to a B'0', the original data interface (or compressed data interface) acts as a device.<br>**Note:** This bit only has meaning if xCNF(12) is a B'0'. |
| 12:11 | Mode<br>These bits configure the interface communication protocol of the original data interface. The values B'00' through B'11' are defined below:<br>**B'00'** Four-edge communication. This is the default value after reset.<br>**B'01'** Burst communication.<br>**B'10'** Synchronous communication.<br>**B'11'** Reserved. |
| 10 | Two Byte<br>When set to a B'1', +xDATA(15:00) (and +xPARITY(1:0) if original data interface (or compressed data interface) parity checking is enabled) are used. When reset to a B'0', +xDATA(07:00) (and +xPARITY(0) if original data interface (or compressed data interface) parity checking is enabled) are used. |
| 9:7 | Reserved |

| Figure 3-3 (Page 2 of 2). xCNF | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 6:4 | Wait States<br>These bits configure the number of wait states used during an original data interface (or compressed data interface) peripheral access. The values B'001' through B'111' are valid.<br>**Notes:**<br>1. The reset value (B'000') of the Wait States bits will cause improper operation of the original data interface (compressed data interface) during peripheral access. If peripheral access will be used on the original data interface (or compressed data interface), then these bits **must** be set to a valid value after every hardware reset.<br>2. These bits only have meaning during an original data interface (or compressed data interface) peripheral access. |
| 3:0 | FIFO Threshold<br>These bits configure the original data interface (or compressed data interface) FIFO threshold value. Values from B'0000' to B'1111' are valid.<br>**Note:** When these bits are reset to B'0000', the original data interface (or compressed data interface) FIFO operates as if its threshold is X'1'. |

### 3.1.3 EC Level (ECL)

The EC Level register provides engineering change information bits to the microprocessor. ECL is never reset.

This register is only accessable when CMND is not equal to X'C100', X'C200', X'C400', or X'C800'.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'1' to read ECL.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'02' to read ECL(7:0); and +ADDR(4:0) equals X'03' to read ECL(15:8).

| Figure 3-4. ECL | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 15:0 | EC Level<br>For ALDC1-40S-M, the value of these bits is B'00000000 11000001'. |

## 3.1.4 Original Data Interface Polarity (OPOL) and Compressed Data Interface Polarity (CPOL)

The Original Data Interface Polarity register provides original data interface polarity configuration capability to the microprocessor. The Compressed Data Interface Polarity register provides compressed data interface polarity configuration capability to the microprocessor. OPOL and CPOL are reset to X'00FF' by a hardware reset.

OPOL is only accessable when CMND is equal to X'C100'; CPOL when CMND is equal to X'C200'.

**Note:** The Original Data Interface Polarity (OPOL) and the Compressed Data Interface Polarity (CPOL) registers are independently configurable. In the discussion below, these registers are called the **xPOL** register, where the "x" is replaced by "O" only or "C" only, as appropriate.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'1' to read and write xPOL.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'02' to read and write xPOL(7:0); and +ADDR(4:0) equals X'03' to read and write xPOL(15:8).

A B'0' in an xPOL bit position will program the corresponding control pin polarity to be positive active. A B'1' will program the corresponding control pin polarity to be negative active.

| Figure 3-5. xPOL | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 15:8 | Reserved |
| 7 | xCIN(0) |
| 6 | xCIN(1) |
| 5 | xCOUT(0) |
| 4 | xCOUT(1) |
| 3 | xCOUT(2) |
| 2 | xCOUT(3) |
| 1 | xCOUT(4) |
| 0 | xCOUT(5) |

## 3.1.5 Original Data Interface Transfer Count (TCO)

The Original Data Interface Transfer Count register provides status information on the number of bytes transferred for a current data transfer operation. Original Data Interface Transfer Count (TCO) is a four byte register with the two most significant bytes contained in Original Data Interface Transfer Count High (TCOH) and the two least significant bytes contained in Original Data Interface Transfer Count Low (TCOL). TCOL and TCOH are reset to X'0000' by a hardware or software reset.

This register is only accessable when CMND is not equal to X'C100', X'C200', X'C400', or X'C800'.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'2' to read TCOH and use +ADDR(4:1) equals X'3' to read TCOL.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'04' to read TCOH(7:0); +ADDR(4:0) equals X'05' to read TCOH(15:8); +ADDR(4:0) equals X'06' to read TCOL(7:0); and +ADDR(4:0) equals X'07' to read TCOL(15:8).

During a compression operation, TCO is incremented as each original data byte is received by the original data interface. When TCO equals XFR during compression, all bytes in the compression operation have been received by ALDC1-40S-M.

During a decompression operation, TCO is incremented as each decompressed data byte is sent by the original data interface.

**Notes:**

1. If OCNF(10) is reset to B'0', then TCO will always increment by one as each byte is received. If OCNF(10) is set to B'1', then TCO will increment by two as each pair of bytes are received. At the end of a data transfer operation, when OCNF(10) is set to B'1', there is a possibility that only one byte will be required to complete the transfer (ie. when an odd number of bytes are transferred). In this case, the TCO will be incremented by one as the byte is received.
2. Because of the time needed to complete any outstanding compression operations on the final bytes received during compression, TCO cannot be used to determine when the compression operation is complete. The Done (STAT(0)) bit is used for this purpose.
3. TCO is a thirty-two bit register. Attempting to transfer 4 gigabytes or more data will result in a TCO register overflow. Therefore, the application or system designer must ensure that data is partitioned into data blocks smaller than 4 gigabytes, and that each data block is compressed and decompressed separately.

Figure 3-6. TCO

| BIT | NAME/NOTES |
|---|---|
| 31:16 | Original Data Interface Transfer Count High (TCOH) |
| 15:0 | Original Data Interface Transfer Count Low (TCOL) |

## 3.1.6 Compressed Data Interface Transfer Count (TCC)

The Compressed Data Interface Transfer Count register provides status information on the number of bytes transferred for a current data transfer operation. Compressed Data Interface Transfer Count (TCC) is a four byte register with the two most significant bytes contained in Compressed Data Interface Transfer Count High (TCCH) and the two least significant bytes contained in Compressed Data Interface Transfer Count Low (TCCL). TCCL and TCCH are reset to X'0000' by a hardware or software reset.

This register is only accessable when CMND is not equal to X'C100', X'C200', X'C400', or X'C800'.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'4' to read TCCH and use +ADDR(4:1) equals X'5' to read TCCL.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'08' to read TCCH(7:0); +ADDR(4:0) equals X'09' to read TCCH(15:8); +ADDR(4:0) equals X'0A' to read TCCL(7:0); and +ADDR(4:0) equals X'0B' to read TCCL(15:8).

During a decompression operation, TCC is incremented as each compressed data byte is received by the compressed data interface. When TCC equals XFR during decompression, all bytes in the decompression operation have been received by ALDC1-40S-M.

During a compression operation, TCC is incremented as each compressed data byte is sent by the compressed data interface.

**Notes:**

1. If CCNF(10) is reset to B'0', then TCC will always increment by one as each byte is received. If CCNF(10) is set to B'1', then TCC will increment by two as each pair of bytes are received. At the end of a data transfer operation, when CCNF(10) is set to B'1', there is a possibility that only one byte will be required to complete the transfer (ie. when an odd number of bytes are transferred). In this case, the TCC will be incremented by one as the byte is received.
2. Because of the time needed to complete any outstanding decompression operations on the final bytes received during decompression, TCC cannot be used to determine when the decompression operation is complete. The Done (STAT(0)) bit is used for this purpose.
3. TCC is a thirty-two bit register. Attempting to transfer 4 gigabytes or more data will result in a TCC register overflow. Therefore, the application or system designer must ensure that data is partitioned into data blocks smaller than 4 gigabytes, and that each data block is compressed and decompressed separately.

| Figure 3-7. TCC | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 31:16 | Compressed Data Interface Transfer Count High |
| 15:0 | Compressed Data Interface Transfer Count Low |

## 3.1.7 Error Status (ERRS)

The Error Status register provides error status bits to the microprocessor. ERRS is reset to X'0000' by a hardware or software reset.

This register is only accessable when CMND is not equal to X'C100', X'C200', X'C400', or X'C800'.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'6' to read ERRS.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'0C' to read ERRS(7:0); and +ADDR(4:0) equals X'0D' to read ERRS(15:8).

| Figure 3-8 (Page 1 of 2). ERRS | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 15:7 | Reserved |
| 6 | Original Data Interface Parity Error<br>This bit is set to B'1' when a parity error is detected during a transfer into +ODATA(15:00) and the original data interface Parity (OCNF(15)) bit is set to B'1'. It is reset to B'0' when a data transfer operation begins or when a reset occurs. |
| 5 | Compressed Data Interface Parity Error<br>This bit is set to B'1' when a parity error is detected during a transfer into +CDATA(15:00) and the compressed data interface Parity (CCNF(15)) bit is set to B'1'. It is reset to B'0' when a data transfer operation begins or when a reset occurs. |

| Figure 3-8 (Page 1 of 2). ERRS | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 4 | Microprocessor Interface Parity Error<br>This bit is set to B'1' when a parity error is detected during a microprocessor write to +MDATA(15:00) and +MENABLEP is tied high. It is reset to B'0' when a data transfer operation begins or when a reset occurs. |
| 3 | Compressed Data Interface Transfer Count (TCC) Overflow Error<br>This bit is set to B'1' when a carry out is detected on the Compressed Data Interface Transfer Count (TCC) register. It is reset to B'0' when a data transfer operation begins or when a reset occurs. |
| 2 | Original Data Interface Transfer Count (TCO) Overflow Error<br>This bit is set to B'1' when a carry out is detected on the Original Data Interface Transfer Count (TCO) register. It is reset to B'0' when a data transfer operation begins or when a reset occurs. |
| 1 | ALDC Decoder Control Code Error<br>This bit is set to B'1' during decompression when an invalid control code is detected in the compressed data stream. It is reset to B'0' when a data transfer operation begins or when a reset occurs.<br>**Important!**<br>See ALDC1-40S-M Design Note 1 on page ii. |

| Figure 3-8 (Page 2 of 2). ERRS | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 0 | ALDC Decoder End Error<br>This bit is set to B'1' during decompression when an End control code is detected while Compressed Data Interface Transfer Count (TCC) is less than Transfer Size (XFR) or when TCC equals XFR and no End control code is detected in the compressed data stream. It is reset to B'0' when a data transfer operation begins or when a reset occurs.<br>**Important!**<br>See ALDC1-40S-M Design Note 1 on page ii. |

## 3.1.8 Interrupt Status (INTS)

The Interrupt Status register provides interrupt status bits to the microprocessor. INTS is reset to X'0000' by a hardware or software reset.

This register is only accessable when CMND is not equal to X'C100', X'C200', X'C400', or X'C800'.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'7' to read INTS.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'0E' to read INTS(7:0); and +ADDR(4:0) equals X'0F' to read INTS(15:8).

See section 3.2 on page 3-12 for more information on interrupts.

| Figure 3-9. INTS | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 15:8 | Reserved |

| Figure 3-9. INTS | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 7 | Done Interrupt<br>This bit is set to B'1' when data transfer has completed on the compressed data interface during compression and when data transfer has completed on the original data interface during decompression. It is reset to B'0' when a data transfer operation begins or when a reset occurs. |
| 6 | Hold Interrupt<br>This bit is set to B'1' when the current transfer step after the microprocessor issues a Hold (CMND equals X'4200') opcode is completed. It is reset to B'0' when the microprocessor issues a Resume (CMND equals X'4400') opcode, when a data transfer operation begins, or when a reset occurs. |
| 5:1 | Reserved |
| 0 | Error Interrupt<br>This bit is set to B'1' when an error occurs. It is reset to B'0' when a data transfer operation begins or when a reset occurs.<br>**Note:** The Error Status (ERRS) register is used to determine the cause of the error. |

## 3.1.9 Command (CMND)

The Command register is used to program operation of ALDC1-40S-M. CMND is reset to X'0000' by a hardware reset. CMND is not changed by a software reset.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'8' to read and write CMND.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'10' to read and write CMND(7:0); and +ADDR(4:0) equals X'11' to read and write CMND(15:8).

| Figure 3-10. CMND | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 15:0 | Opcode<br>See Figure 3-11 on page 3-9 for proposed opcode descriptions. |

The CMND Register layout shown in Figure 3-10 on page 3-8 is defined in the opcode description given in Figure 3-11.

| Figure 3-11 (Page 1 of 2). Opcodes.<br>**Note:** Opcodes not explicitly named in this table are reserved for future use. They are invalid for ALDC1-40S-M and will produce no operation. | |
|---|---|
| **OPCODE** | **NAME/NOTES** |
| X'0000' | NOP<br>No operation is performed. |
| X'4200' | Hold<br>When a data transfer operation is in progress, any current operation steps are completed and the original data interface and compressed data interface data buses are placed into a high impedance state. The Hold Interrupt (INTS(6)) and Hold (STAT(6)) bits are then set to B'1'. All data currently being processed by the data transfer operation is preserved. |
| X'4400' | Resume<br>A previously held data transfer operation resumes processing. The Hold Interrupt (INTS(6)) and Hold (STAT(6)) bits are reset to B'0' and the Busy (STAT(7)) bit is set to B'1'. |
| X'5000' | Start Compression Bypass<br>See section 2.2.2 on page 2-3 for a detailed description of this data transfer operation. |
| X'5800' | Start Compression<br>See section 2.2.3 on page 2-3 for a detailed description of this data transfer operation. |

| Figure 3-11 (Page 1 of 2). Opcodes.<br>**Note:** Opcodes not explicitly named in this table are reserved for future use. They are invalid for ALDC1-40S-M and will produce no operation. | |
|---|---|
| **OPCODE** | **NAME/NOTES** |
| X'6000' | Start Decompression Bypass<br>See section 2.2.4 on page 2-3 for a detailed description of this data transfer operation. |
| X'6800' | Start Decompression<br>See section 2.2.5 on page 2-3 for a detailed description of this data transfer operation. |
| X'6C00' | Start Decompression Output Disabled<br>See section 2.2.6 on page 2-3 for a detailed description of this data transfer operation. |
| X'A000' | Software Reset<br>The Original Data Interface Configuration (OCNF), Compressed Data Interface Configuration (CCNF), EC Level (ECL), Original Data Interface Polarity (OPOL), Compressed Data Interface Polarity (CPOL), and Command (CMND) registers are not affected by this opcode. All other registers are reset, current operations are cancelled, and the history buffer is cleared.<br>**Important!**<br>See ALDC1-40S-M Design Note 1 on page ii. |
| X'C100' | Select Original Data Interface Configuration<br>The OCNF and OPOL registers are enabled for reads and writes. |
| X'C200' | Select Compressed Data Interface Configuration<br>The CCNF and CPOL registers are enabled for reads and writes. |

Figure 3-11 (Page 2 of 2). Opcodes.

**Note:** Opcodes not explicitly named in this table are reserved for future use. They are invalid for ALDC1-40S-M and will produce no operation.

| OPCODE | NAME/NOTES |
|---|---|
| X'C400' | Select Original Data Interface Peripheral Access<br><br>All peripheral access addresses (+ADDR(4) equals B'0') are enabled for reads and writes to an original data interface attached peripheral.<br><br>**Important!**<br>See ALDC1-40S-M Design Note 2 on page ii. |
| X'C800' | Select Compressed Data Interface Peripheral Access<br><br>All peripheral access addresses (+ADDR(4) equals B'0') are enabled for reads and writes to an compressed data interface attached peripheral.<br><br>**Important!**<br>See ALDC1-40S-M Design Note 2 on page ii. |

## 3.1.10 Transfer Size (XFR)

The Transfer Size register provides the microprocessor control of the number of bytes transferred during a data transfer operation. Transfer Size (XFR) is a four byte register with the two most significant bytes contained in Transfer Size High (XFRH) and the two least significant bytes contained in Transfer Size Low (XFRL). XFRL and XFRH are reset to X'0000' by a hardware or software reset.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'A' to read and write XFRH and use +ADDR(4:1) equals X'B' to read and write XFRL.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'14' to read and write XFRH(7:0); +ADDR(4:0) equals X'15' to read and write XFRH(15:8); +ADDR(4:0) equals X'16' to read and write XFRL(7:0); and +ADDR(4:0) equals X'17' to read and write XFRL(15:8).

The direction of the data transfer operation specifies whether the Original Data Interface Transfer Count (TCO) register or the Compressed Data Interface Transfer Count (TCC) register is used to determine when all data bytes have been received for the data transfer operation. During compression, TCO is used. During decompression, TCC is used. When the appropriate Transfer Count register (TCO or TCC) equals XFR, all bytes in the current data transfer operation have been received by ALDC1-40S-M.

**Note:** XFR is a thirty-two bit register. This means that the maximum data block size which can be specified is X'FFFF FFFF' (or 4,294,967,295) bytes. Therefore, the application or system designer must ensure that data is partitioned into data blocks smaller than 4 gigabytes, and that each data block is compressed and decompressed separately.

Figure 3-12. XFR

| BIT | NAME/NOTES |
|---|---|
| 31:16 | Transfer Size High (XFRH) |
| 15:0 | Transfer Size Low (XFRL) |

## 3.1.11 Data Disable Count (DDC)

The Data Disable Count register provides the microprocessor control of the number of bytes skipped during a Start Decompression Output Disabled (CMND equals X'6C00') operation. Data Disable Count (DDC) is a four byte register with the two most significant bytes contained in Data Disabled Count High (DDCH) and the two least significant bytes contained in Data Disabled Count Low (DDCL). DDCL and DDCH are reset to X'0000' by a hardware or software reset.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'C' to read and write DDCH and use +ADDR(4:1) equals X'D' to read and write DDCL.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'18' to read and write DDCH(7:0); +ADDR(4:0) equals X'19' to read and write DDCH(15:8); +ADDR(4:0) equals X'1A' to read and write DDCL(7:0); and +ADDR(4:0) equals X'1B' to read and write DDCL(15:8).

**Note:** If the Data Disable Count (DDC) is set to X'0000' during a Start Decompression Output Disabled (CMND equals X'6C00') operation or

the DDC is greater than the Transfer Size (XFR) during a Start Decompression Output Disabled (CMND equals X'6C00') operation, then the original data interface output will be disabled for the entire transfer.

| Figure 3-13. DDC | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 31:16 | Data Disabled Count High (DDCH) |
| 15:0 | Data Disabled Count Low (DDCL) |

## 3.1.12 Error Mask (EMSK)

The Error Mask register provides error reporting configuration capability to the microprocessor. EMSK is reset to X'0000' by a hardware or software reset.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'E' to read and write EMSK.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'1C' to read and write EMSK(7:0); and +ADDR(4:0) equals X'1D' to read and write EMSK(15:8).

**Note:** The Error Mask register is provided to allow *temporary* masking of error signals. This register should always be reset to X'0000' for field usage.

| Figure 3-14. EMSK | |
|---|---|
| **BIT** | **NAME/NOTES** |
| 15:7 | Reserved |
| 6 | Original Data Interface Parity Error Mask<br>When set to a B'1', the corresponding Original Data Interface Parity Error (ERRS(6)) bit is disabled. When reset to a B'0', the Original Data Interface Parity Error bit is re-enabled. |
| 5 | Compressed Data Interface Parity Error Mask<br>When set to a B'1', the corresponding Compressed Data Interface Parity Error (ERRS(5)) bit is disabled. When reset to a B'0', the Compressed Data Interface Parity Error bit is re-enabled. |
| 4 | Microprocessor Interface Parity Error Mask<br>When set to a B'1', the corresponding Microprocessor Interface Parity Error (ERRS(4)) bit is disabled. When reset to a B'0', the Microprocessor Interface Parity Error bit is re-enabled. |
| 3 | Compressed Data Interface Transfer Count (TCC) Overflow Error Mask<br>When set to a B'1', the corresponding Compressed Data Interface Transfer Count (TCC) Overflow Error (ERRS(3)) bit is disabled. When reset to a B'0', the Compressed Data Interface Transfer Count Overflow Error bit is re-enabled. |
| 2 | Original Data Interface Transfer Count (TCO) Overflow Error Mask<br>When set to a B'1', the corresponding Original Data Interface Transfer Count (TCO) Overflow Error (ERRS(2)) bit is disabled. When reset to a B'0', the Original Data Interface Transfer Count Overflow Error bit is re-enabled. |
| 1 | ALDC Decoder Control Code Error Mask<br>When set to a B'1', the corresponding ALDC Decoder Control Error (ERRS(1)) bit is disabled. When reset to a B'0', the ALDC Decoder Control Code Error bit is re-enabled. |
| 0 | ALDC Decoder End Error Mask<br>When set to a B'1', the corresponding ALDC Decoder End Error (ERRS(0)) bit is disabled. When reset to a B'0', the ALDC Decoder End Error bit is re-enabled. |

### 3.1.13 Interrupt Mask (IMSK)

The Interrupt Mask register provides interrupt reporting configuration capability to the microprocessor. IMSK is reset to X'0000' by a hardware or software reset.

When +M1BYTE is tied low, use +ADDR(4:1) equals X'F' to read and write IMSK.

When +M1BYTE is tied high, use +ADDR(4:0) equals X'1E' to read and write IMSK(7:0); and +ADDR(4:0) equals X'1F' to read and write IMSK(15:8).

**Note:** The microprocessor disables interrupts by setting bits in IMSK. When interrupts are disabled, it is the microprocessor responsibility to ensure that the correct STAT bits are polled.

Figure 3-15. IMSK

| BIT | NAME/NOTES |
|---|---|
| 15:8 | Reserved |
| 7 | Done Interrupt Mask<br>When set to a B'1', the corresponding Done Interrupt (INTS(7)) bit is disabled. When reset to a B'0', the Done Interrupt is re-enabled. |
| 6 | Hold Interrupt Mask<br>When set to a B'1', the corresponding Hold Interrupt (INTS(6)) bit is disabled. When reset to a B'0', the Hold Interrupt is re-enabled. |
| 5:1 | Reserved |
| 0 | Error Interrupt Mask<br>When set to a B'1', the corresponding Error Interrupt (INTS(0)) bit is disabled. When reset to a B'0', the Error Interrupt is re-enabled. |

## 3.2 Interrupts

There are two hardware interrupt signals for ALDC1-40S-M. One is -IREQOD, which is a negative active, open-drain output. The other is +IREQPP; a positive active, push-pull output.

When active, they indicate that a data transfer operation has completed successfully, has been held, or has failed.

The microprocessor can determine if the data transfer operation failed by reading and testing the Any Error (STAT(1)) bit. If the Any Error bit is set to a B'1', then an error occurred in the previously attempted data transfer operation. The cause of the error can be determined by reading the Error Status (ERRS) register. Error recovery procedures may then be invoked as appropriate.

If the Any Error bit is B'0', then no error occurred in the previous data transfer operation.

Likewise, the microprocessor can determine if the data transfer operation was held by reading and testing the Hold (STAT(6)) bit. If the Hold bit is set to a B'1', then the data transfer operation is held and waiting to be resumed.

If both the Any Error bit and the Hold bit are B'0' and the Done (STAT(0)) bit is a B'1', then the data transfer operation completed successfully.

The hardware interrupt signals automatically return to their inactive state when either a hardware reset or a software reset occurs, when a data transfer operation is resumed, or when a new data transfer operation begins.

**Note:** -IREQOD is an open-drain output and requires a pull-up resistor. See section Chapter 6 on page 6-1 for pull-up resistor selection considerations.

## 3.3 Resets

There is one hardware reset signal for ALDC1-40S-M (-RESET). When asserted, all registers (except the EC Level register) are reset, current operations are cancelled, and the history buffer is cleared.

There is also one software reset for ALDC1-40S-M (CMND equals X'A000'). The software reset does not affect the Original Data Interface Configuration (OCNF), Compressed Data Interface Configuration (CCNF), EC Level (ECL), Original Data Interface Polarity (OPOL), Compressed Data Interface Polarity (CPOL), or Command (CMND) registers. All other regis-

ters are reset, current operations are cancelled, and the history buffer is cleared.

**Important!**

See ALDC1-40S-M Design Note 1 on page ii.

Figure 3-16 summarizes the hardware and software resets for ALDC1-40S-M. Because some register's contents are modified during initialization for data transfer operations, this information is also included in the figure.

Figure 3-16. Reset Summary

| +ADDR(4:1) | MNEMONIC | HARDWARE RESET | OPCODE X'A000': SOFTWARE RESET | DATA TRANSFER INITIALIZATION |
|---|---|---|---|---|
| X'0' | STAT | X'0000' | X'0000' | X'0080' (Busy) |
| | OCNF | X'0000' | unchanged | unchanged |
| | CCNF | X'0000' | unchanged | unchanged |
| X'1' | ECL | unchanged | unchanged | unchanged |
| | OPOL | X'00FF' | unchanged | unchanged |
| | CPOL | X'00FF' | unchanged | unchanged |
| X'2' | TCOH | X'0000' | X'0000' | X'0000' |
| X'3' | TCOL | X'0000' | X'0000' | X'0000' |
| X'4' | TCCH | X'0000' | X'0000' | X'0000' |
| X'5' | TCCL | X'0000' | X'0000' | X'0000' |
| X'6' | ERRS | X'0000' | X'0000' | X'0000' |
| X'7' | INTS | X'0000' | X'0000' | X'0000' |
| X'8' | CMND | X'0000' | unchanged | unchanged |
| X'A' | XFRH | X'0000' | X'0000' | unchanged |
| X'B' | XFRL | X'0000' | X'0000' | unchanged |
| X'C' | DDCH | X'0000' | X'0000' | unchanged |
| X'D' | DDCL | X'0000' | X'0000' | unchanged |
| X'E' | EMSK | X'0000' | X'0000' | unchanged |
| X'F' | IMSK | X'0000' | X'0000' | unchanged |

## 3.4 Data Expansion

Data expansion occurs when the size of the data increases during a compression operation. This is a rare occurrence because the ALDC1-40S-M adapts to the data being compressed. However, the application or system designer must be aware of data expansion and consider its impact on system operation.

If data expansion causes the Compressed Data Interface Transfer Count (TCC) to exceed 4,294,967,295 bytes, then the ALDC1-40S-M would set the TCC Overflow Error (ERRS(12)) bit to B'1', set the Any Error (STAT(14)) bit to B'1', assert the -IREQOD and +IREQPP outputs, and cancel the transfer.

The ALDC1-40S-M also has an Expansion (STAT(12)) bit which may be used to detect data expansion when no errors occur.

### 3.4.1 Worst Case Expansion

The ALDC compression algorithm approaches a worst case of 12.5% data expansion. For example, if a given system always compresses 60,000 byte data blocks, then there is a small possibility that about 67,500 bytes may result from a worst case compression operation.

Continuing with the example, the microprocessor might detect that expansion occurred and initiate recovery by transferring the original 60,000 bytes instead.

The example demonstrates how data expansion might be handled at a system level. It is up to the application or system designer to determine the appropriate system response to data expansion.

Data modeling may indicate that the probability of data expansion is so small as to be nonexistent (for a specific application). In this case, the application or system designer need not be concerned about data expansion.

**Note:** If data expansion is a design concern, then the following formula may be used to calculate the maximum allowable transfer size for a given compressed data buffer size:

$$XFR_{max} = INT(\frac{8}{9}(CDB - 3))$$

where $XFR_{max}$ is the maximum allowable transfer size in bytes, CDB is the compressed data buffer size in bytes, and INT(x) is the integer function (sometimes called the floor function). CDB is under the control of the application or system designer. The compressed data buffer is *not* part of the ALDC1-40S-M. Rather, in this document, the compressed data buffer size describes the byte limit imposed on the number compressed bytes output during a compression operation. This limit might be imposed because of bus, memory, real-time, or other system constraints.

If no compressed data buffer size exists for the design, or if the compressed data buffer size is larger than 4,294,967,295 bytes, then $XFR_{max}$ should be set at 3,817,748,700,

# Chapter 4. Hardware Interface and Timing

## 4.1 Control Pins

The control pins are those pins which have more than one logical function depending upon the mode in which their respective interface is configured. They are summarized below.

The signal names are used to associate the pin names with their logical function.

Figure 4-1. Microprocessor Interface Control Pins

| Pin Name | Pin used as Signal When... MMODE is tied low. | Pin used as Signal When... MMODE is tied high. |
|---|---|---|
| MCIN(0) | -READ | -CS |
| MCIN(1) | -WRITE | +R/-W |
| MCOUT | -WAIT | -WAIT |

Figure 4-2. Original Data Interface and Compressed Data Interface Control Pins. When using this figure, replace "x" by "O" only or "C" only, as appropriate. The "O" is used to describe original data interface control pins and signals. The "C" is used to describe compressed data interface control pins and signals.

| Pin Name | Pin used as Signal When... xCNF(13:12) = B'10' (Controller) | xCNF(13:12) = B'00' (Device) | xCNF(12) = B'1' (Synchronous) | CMND = X'C400' (Peripheral Access) |
|---|---|---|---|---|
| xCIN(0) | xREQ | xACK | xCS | not used |
| xCIN(1) | not used | not used | xENABLE | not used |
| xCOUT(0) | xACK | xREQ | xREADY | not used |
| xCOUT(1) | xWR | not used | not used | xWR |
| xCOUT(2) | xRD | not used | not used | xRD |
| xCOUT(3) | not used | not used | not used | xPCS |
| xCOUT(4) | xAF | xAF | xAF | xAF |
| xCOUT(5) | xAE | xAE | xAE | xAE |

**Note:** The xPOL register controls the polarity of the control pins.

## 4.2 Microprocessor Interface

ALDC1-40S-M provides an asynchronous interface to the controlling microprocessor.

The microprocessor interface is shown in Figure 4-3 on page 4-2.

The microprocessor interface can be run in either one of two modes which are selected using the MMODE pin. When MMODE is tied high, the microprocessor interface is controlled using a chip select and a read/write signal. When MMODE is tied low, the microprocessor interface is controlled using a read and a write signal. Read timing using -CS and +R/-W on the microprocessor interface is shown in Figure 4-4 on page 4-2. Write timing using -CS and +R/-W on the microprocessor interface is shown in Figure 4-5 on page 4-4. Read timing using -READ and -WRITE on the microprocessor interface is shown in Figure 4-6 on page 4-5. Write timing using -READ and -WRITE on the microprocessor interface is shown in Figure 4-7 on page 4-7.

Hardware reset timing on the microprocessor interface is shown in Figure 4-8 on page 4-8.

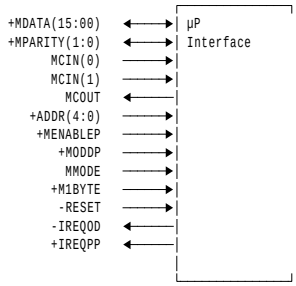



Figure 4-3. Microprocessor Interface

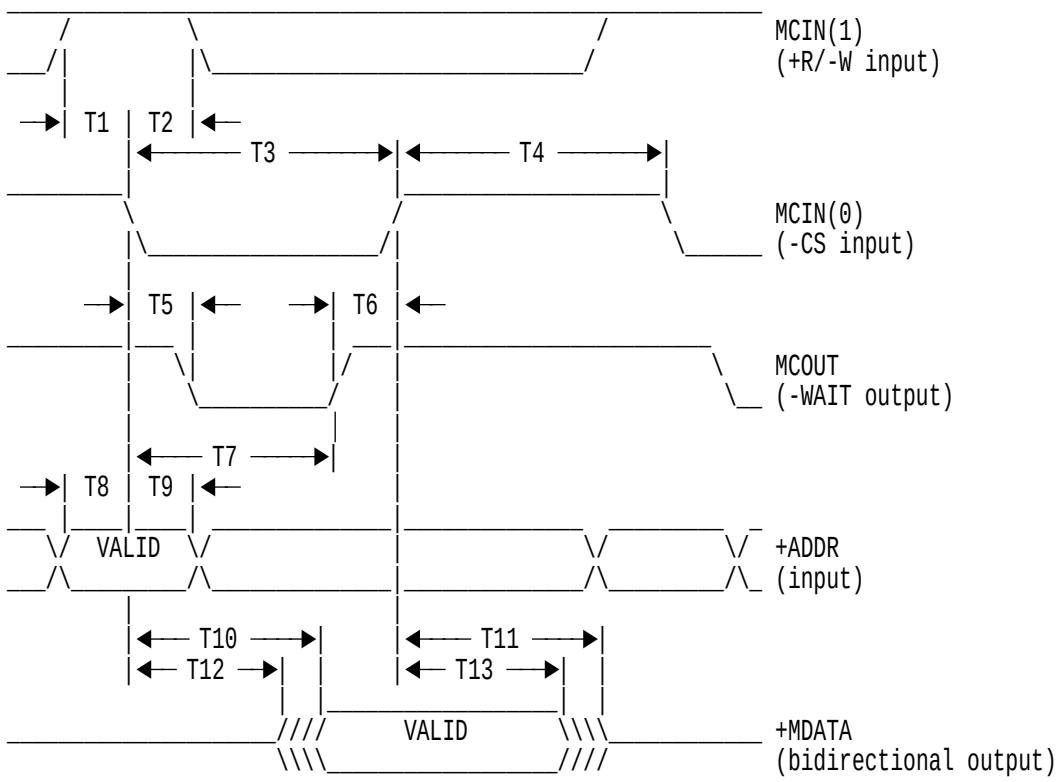



Figure 4-4 (Part 1 of 2). Microprocessor Interface Read Timing with MMODE Tied High

| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | +R/-W high before -CS active | 0.5 ns | |
| T2 | +R/-W high after -CS active | 3.5 ns | |
| T3 | -CS active to -CS inactive (See note 1.) | 3 clock cycles | |
| T4 | -CS inactive to -CS active | 2 clock cycles | |
| T5 | -WAIT active after -CS active | 5 ns | 17.5 ns |
| T6 | -CS inactive after -WAIT inactive (See note 1.) | 0 ns | |
| T7 | -WAIT inactive after -CS active | 2 clock cycles | 3 clock cycles + 18 ns |
| T8 | +ADDR valid before -CS active | 0 ns | |
| T9 | +ADDR hold time after -CS active | 5 ns | |
| T10 | +MDATA valid after -CS active | 1 clock cycle + 4 ns | 2 clock cycles + 24 ns |
| T11 | +MDATA disable time after -CS inactive | 1 clock cycle + 5.5 ns | 2 clock cycle + 20 ns |
| T12 | +MDATA enable time after -CS active | 1 clock cycle + 6 ns | 2 clock cycles + 21.5 ns |
| T13 | +MDATA valid after -CS inactive | 1 clock cycle + 4 ns | 2 clock cycle + 20 ns |

**Note:**

1. When using -WAIT to control -CS inactive, ignore T3. Otherwise, ignore T6.

**Usage note:** The microprocessor interface latches the address on the falling edge of -CS. The user should latch output data on the rising edge of -CS.

Figure 4-4 (Part 2 of 2). Microprocessor Interface Read Timing with MMODE Tied High

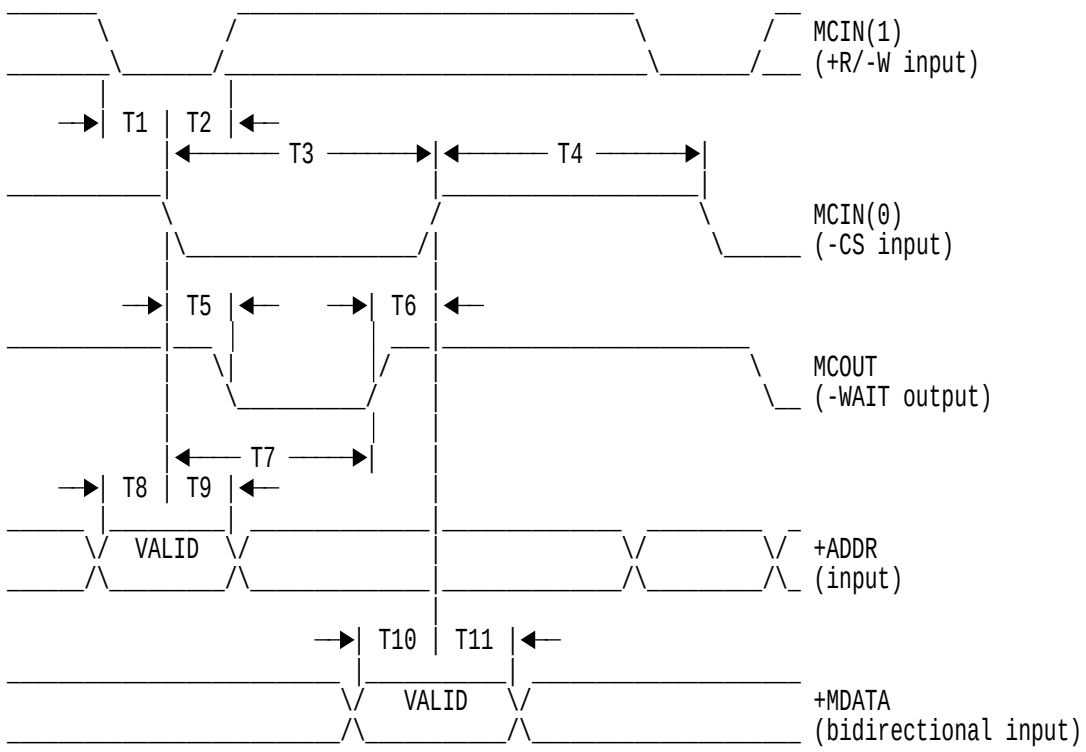



Figure 4-5 (Part 1 of 2). Microprocessor Interface Write Timing with MMODE Tied High

| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | +R/-W low before -CS active | 0.5 ns | |
| T2 | +R/-W low after -CS active | 3.5 ns | |
| T3 | -CS active to -CS inactive (See note 1.) | 2 clock cycles | |
| T4 | -CS inactive to -CS active | 3 clock cycles | |
| T5 | -WAIT active after -CS active | 5 ns | 17.5 ns |
| T6 | -CS inactive after -WAIT inactive (See note 1.) | 0 ns | |
| T7 | -WAIT inactive after -CS active | 1 clock cycle | 2 clock cycles + 18 ns |
| T8 | +ADDR valid before -CS active | 0 ns | |
| T9 | +ADDR hold time after -CS active | 5 ns | |
| T10 | +MDATA valid before -CS inactive | 2.5 ns | |
| T11 | +MDATA hold time after -CS inactive | 3.5 ns | |

**Note:**

1. When using -WAIT to control -CS inactive, ignore T3. Otherwise, ignore T6.

**Usage note:** The microprocessor interface latches the address on the falling edge of -CS. The microprocessor interface latches input data on the rising edge of -CS.

Figure 4-5 (Part 2 of 2). Microprocessor Interface Write Timing with MMODE Tied High

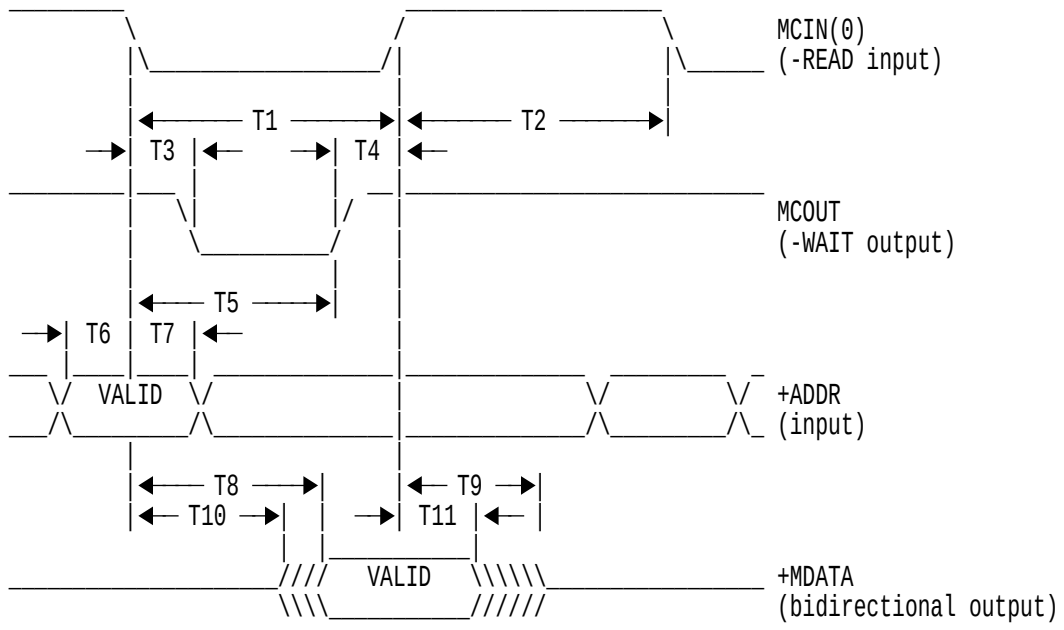



Figure 4-6 (Part 1 of 2). Microprocessor Interface Read Timing with MMODE Tied Low

| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | -READ active to -READ inactive (See note 1.) | 3 clock cycles | |
| T2 | -READ inactive to -READ active | 2 clock cycles | |
| T3 | -WAIT active after -READ active | 7.5 ns | 17 ns |
| T4 | -WAIT inactive before -READ inactive (See note 1.) | 0 ns | |
| T5 | -WAIT inactive after -READ active | 2 clock cycles | 3 clock cycles + 18 ns |
| T6 | +ADDR valid before -READ active | 0 ns | |
| T7 | +ADDR hold time after -READ active | 5.5 ns | |
| T8 | +MDATA valid after -READ active | 1 clock cycle + 4 ns | 2 clock cycles + 24 ns |
| T9 | +MDATA disable time after -READ inactive | 1 clock cycle + 5.5 ns | 2 clock cycles + 20 ns |
| T10 | +MDATA enable time after -READ active | 1 clock cycle + 6 ns | 2 clock cycles + 21.5 ns |
| T11 | +MDATA valid after -READ inactive | 1 clock cycle + 4 ns | 2 clock cycles + 20 ns |

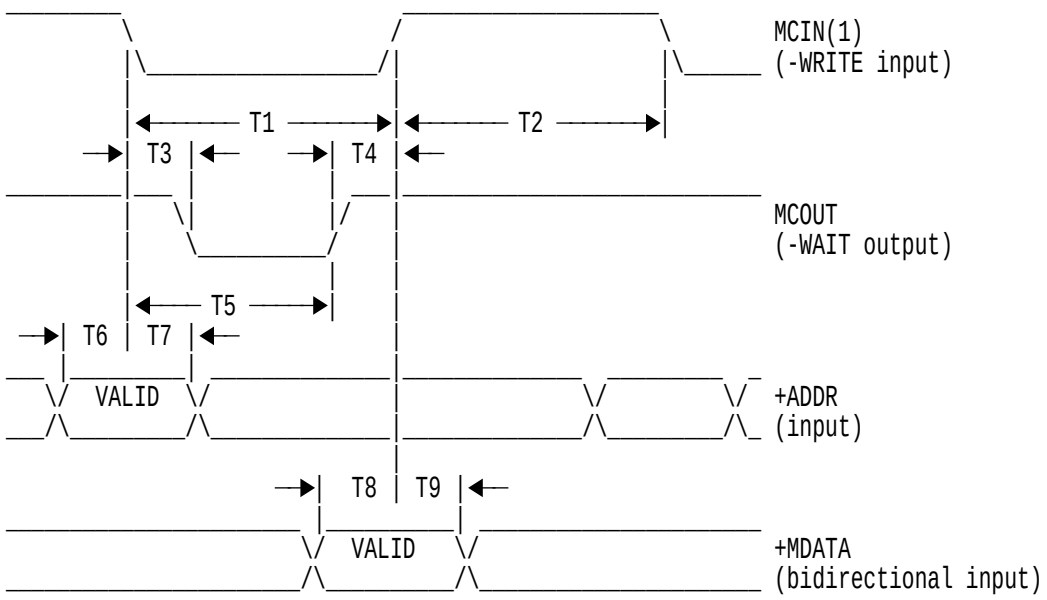
**Note:**

1. When using -WAIT to control -READ inactive, ignore T1. Otherwise ignore T4.

**Usage note:** The microprocessor interface latches the address on the falling edge of -READ. The user should latch output data on the rising edge of -READ.

**Note:** -WRITE must be inactive during all transfers out of the microprocessor interface.

Figure 4-6 (Part 2 of 2). Microprocessor Interface Read Timing with MMODE Tied Low




| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | -WRITE active to -WRITE inactive (See note 1.) | 2 clock cycles | |
| T2 | -WRITE inactive to -WRITE active | 3 clock cycles | |
| T3 | -WAIT active after -WRITE active | 7.5 ns | 17 ns |
| T4 | -WAIT inactive before -WRITE inactive (See note 1.) | 0 ns | |
| T5 | -WAIT inactive after -WRITE active | 1 clock cycle | 2 clock cycles + 18 ns |
| T6 | +ADDR valid before -WRITE active | 0 ns | |
| T7 | +ADDR hold time after -WRITE active | 5.5 ns | |
| T8 | +MDATA valid before -WRITE inactive | 2.5 ns | |
| T9 | +MDATA hold time after -WRITE inactive | 4.5 ns | |

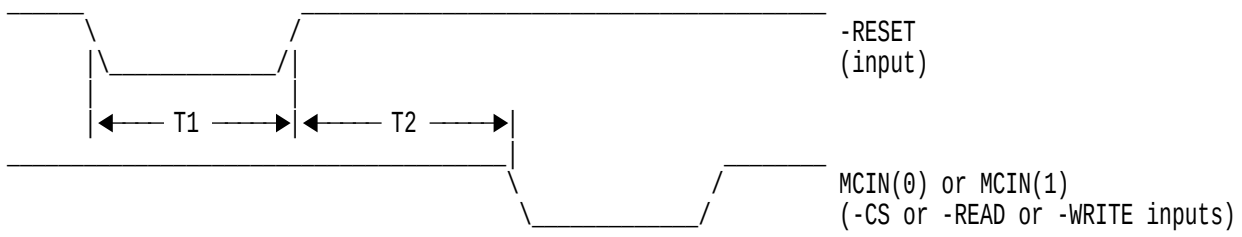
**Note:**

1. When using -WAIT to control -WRITE inactive, ignore T1. Otherwise, ignore T4.

**Usage note:** The microprocessor interface latches the address on the falling edge of -WRITE. The microprocessor interface latches input data on the rising edge of -WRITE.

**Note:** -READ must be inactive during all transfers into the microprocessor interface.

Figure 4-7. Microprocessor Interface Write Timing with MMODE Tied Low




| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | -RESET active to -RESET inactive | 4 clock cycles | |
| T2 | -RESET inactive to -CS or -READ or -WRITE active | 2 clock cycles | |

Figure 4-8. Microprocessor Interface Hardware Reset

## 4.3 Original Data Interface and Compressed Data Interface

Both the original data interface and the compressed data interface operate in four modes. These modes are described below.

**Note:** The original data interface and compressed data interface are idependently configured using the OCNF, OPOL, CCNF, and CPOL registers. See pages 3-3 to 3-5 for more detail on these registers.

**Note:** The following timing diagrams describe the communication between the original data interface or compressed data interface and the external module connected to it. In all of these timing diagrams, the Original Data Interface Polarity (OPOL) and Compressed Data Interface Polarity (CPOL) registers are assumed to be reset to X'00FF'. This is their default state (ie. negative active polarity). If any OPOL or CPOL bits are changed, then the corresponding control pin will be inverted from what is shown in these timing diagrams (ie. positive active polarity).

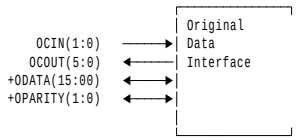



Figure 4-9. Original Data Interface

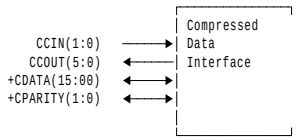
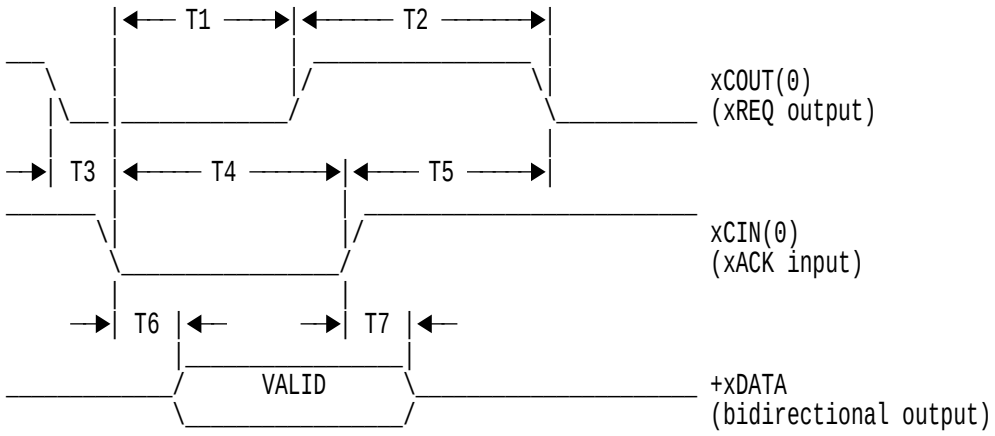


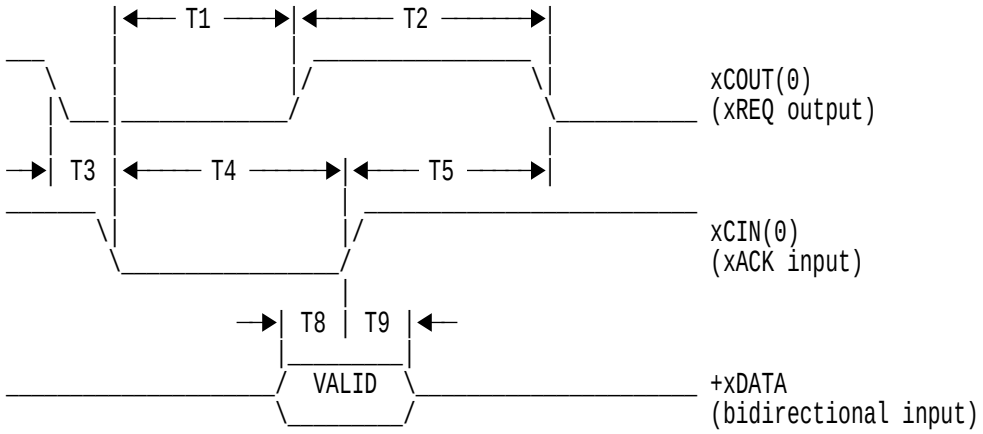

Figure 4-10. Compressed Data Interface

### 4.3.1 Four-edge Mode

This mode is an asynchronous data transfer in which one or two bytes is transferred for every request/acknowledge pair. As shown in Figure 4-11 on page 4-9 and Figure 4-12 on page 4-10, a typical four-edge transfer assumes a request goes active to initiate the transfer, the acknowledge then goes active in response to the request, which leads to a withdrawal of the request and finally the acknowledge is withdrawn and data is transferred on the inactivating edge of the acknowledge.




Out of ALDC1-40S-M

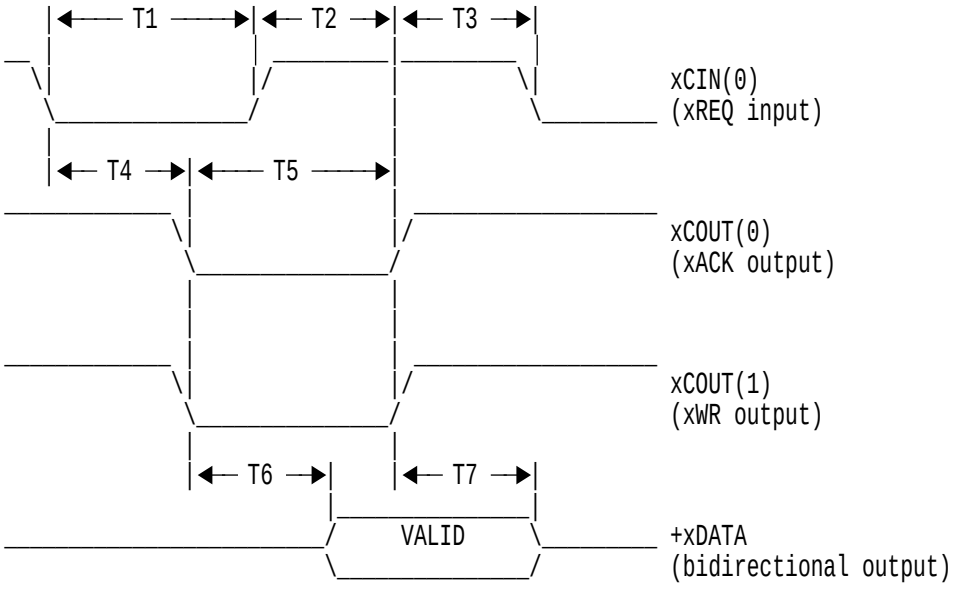



Into ALDC1-40S-M

Figure 4-11 (Part 1 of 2). Four-edge Device Timing

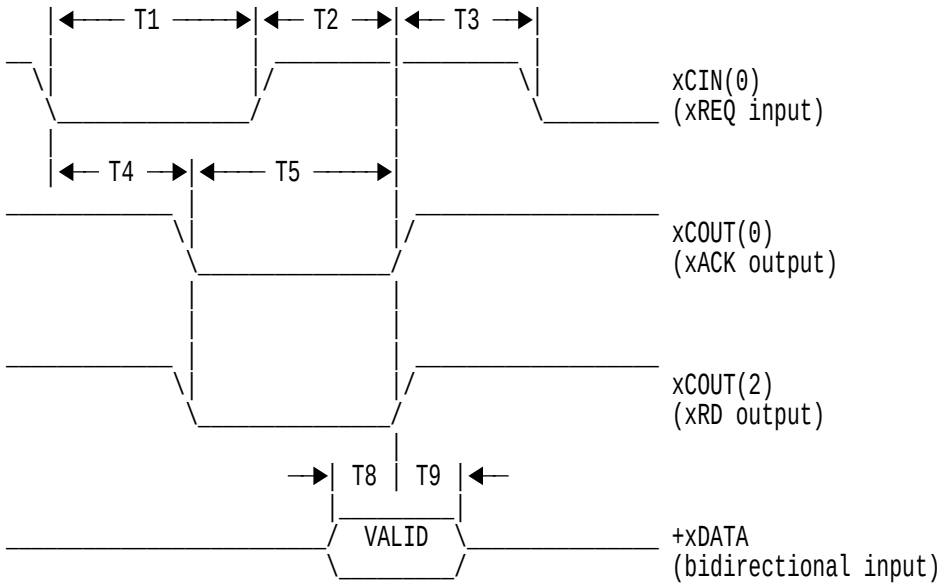
| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | xACK active to xREQ inactive | 5 ns<br>{7 ns} | 20 ns<br>{24 ns} |
| T2 | xREQ inactive to next xREQ active | 2 clock cycles – 5 ns | |
| T3 | xREQ active to xACK active | 1 clock cycle | |
| T4 | xACK active to xACK inactive | 2 clock cycles | |
| T5 | xACK inactive to next xREQ active | 1 clock cycle | |
| T6 | +xDATA valid after xACK active | 5 ns | 22 ns |
| T7 | +xDATA valid after xACK inactive | 5 ns | 22 ns |
| T8 | +xDATA valid before xACK inactive | 2 ns | |
| T9 | +xDATA hold time after xACK inactive | 8 ns | |

Figure 4-11 (Part 2 of 2). Four-edge Device Timing. When using this figure, replace "x" by "O" only or "C" only, as appropriate. Negative active timings are shown. Positive active timing values are given in brackets { } when different from the negative active timing values.




Out of ALDC1-40S-M

Figure 4-12 (Part 1 of 3). Four-edge Controller Timing




Into ALDC1-40S-M

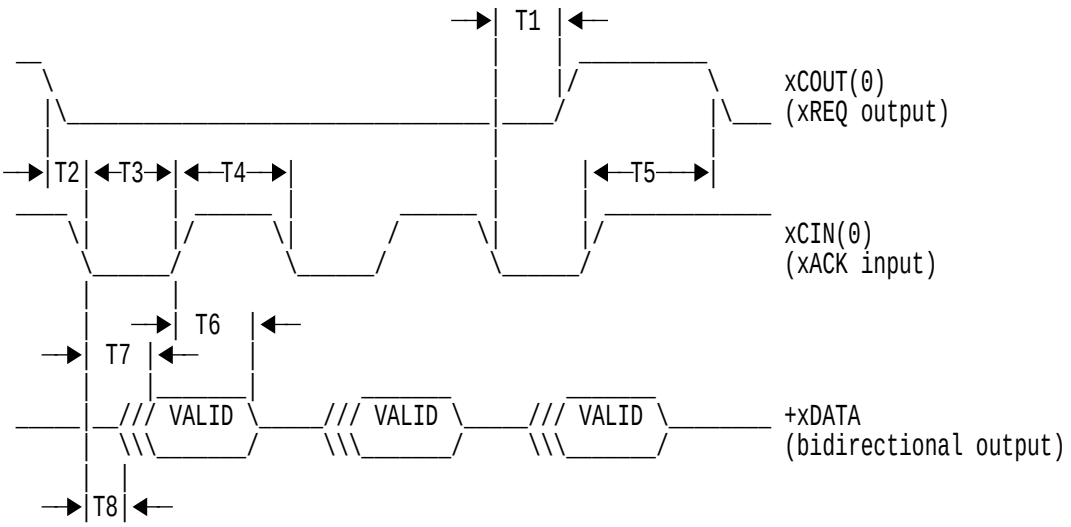
Figure 4-12 (Part 2 of 3). Four-edge Controller Timing

| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | xREQ active to xREQ inactive | 2 clock cycles | |
| T2 | xREQ inactive to xACK inactive | 1 clock cycle | 2 clock cycles + 22 ns<br>{2 clock cycles + 26 ns} |
| T3 | xACK inactive to next xREQ active | 0 ns | |
| T4 | xREQ active to xACK active | 1 clock cycle | |
| T5 | xACK active to xACK inactive | 2 clock cycles – 5 ns | |
| T6 | +xDATA valid after xACK active | 1 clock cycle – 5 ns | 1 clock cycle + 5 ns<br>{1 clock cycle + 9 ns} |
| T7 | +xDATA valid after xACK inactive | 1 clock cycle – 5 ns<br>{1 clock cycle – 7 ns} | 1 clock cycle + 8 ns<br>{1 clock cycle + 4 ns} |
| T8 | +xDATA valid before xACK inactive | 12 ns<br>{16 ns} | |
| T9 | +xDATA hold time after xACK inactive | 0 ns | |

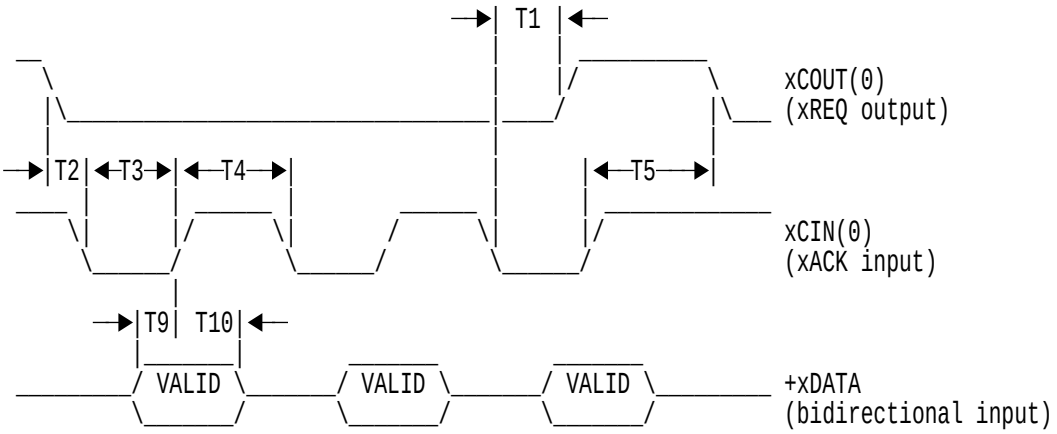
Figure 4-12 (Part 3 of 3). Four-edge Controller Timing. When using this figure, replace "x" by "O" only or "C" only, as appropriate. Negative active timings are shown. Positive active timing values are given in brackets { } when different from the negative active timing values.

## 4.3.2 Burst Mode

This mode is like the four-edge mode. It is asynchronous and requires both a request and acknowledge signal. The key difference is that there may be multiple acknowledges and therefore multiple data transfers during a single extended request, thereby reducing the number of cycles required per transfer.




Out of ALDC1-40S-M




Into ALDC1-40S-M

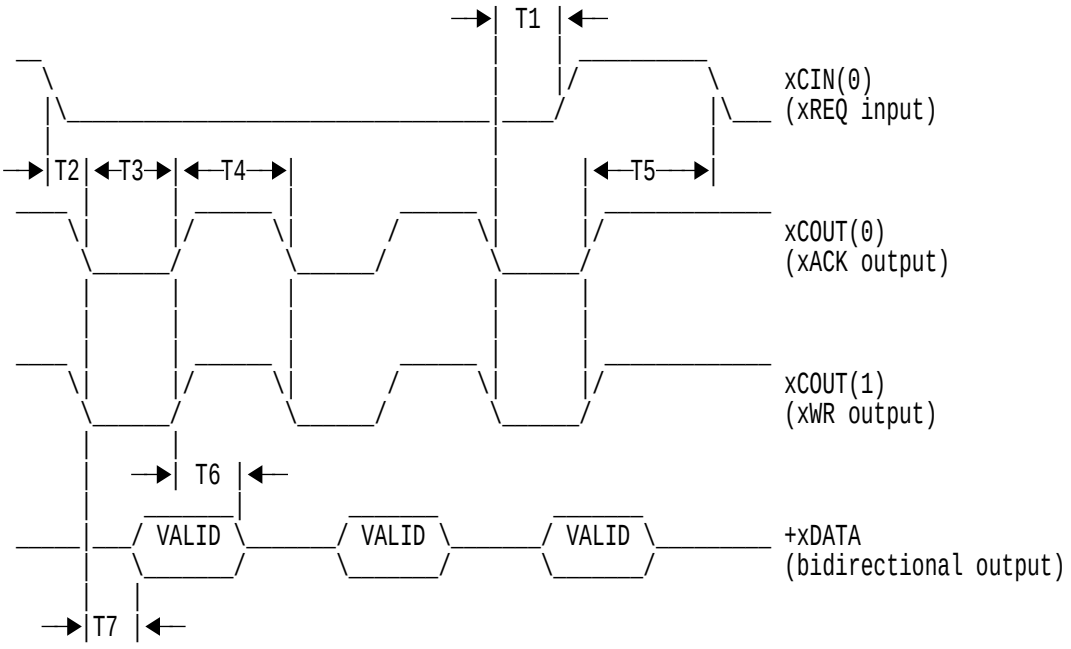
Figure 4-13 (Part 1 of 2). Burst Device Timing

| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | Last xACK active to xREQ inactive - Ending Burst (See note 1) | 5 ns<br>{7 ns} | 1 clock cycle + 29 ns<br>{1 clock cycle + 33 ns} |
| T2 | xREQ active to xACK active - Starting Burst | 1 clock cycle | |
| T3 | xACK active to xACK inactive | 2 clock cycles | |
| T4 | xACK inactive to xACK active (See notes 1, 2 and 3) | 2 clock cycles | |
| T5 | Last xACK inactive to next xREQ active - Start new burst | 2 clock cycles | |
| T6 | +xDATA valid after xACK inactive | 5 ns | 22 ns |
| T7 | +xDATA valid after xACK active. (See note 2) | 5 ns | 1 clock cycle + 25 ns |
| T8 | +xDATA enable time after xACK active | 5 ns | 22 ns |
| T9 | +xDATA valid before xACK inactive | 2 ns | |
| T10 | +xDATA hold time after xACK inactive | 7 ns | |

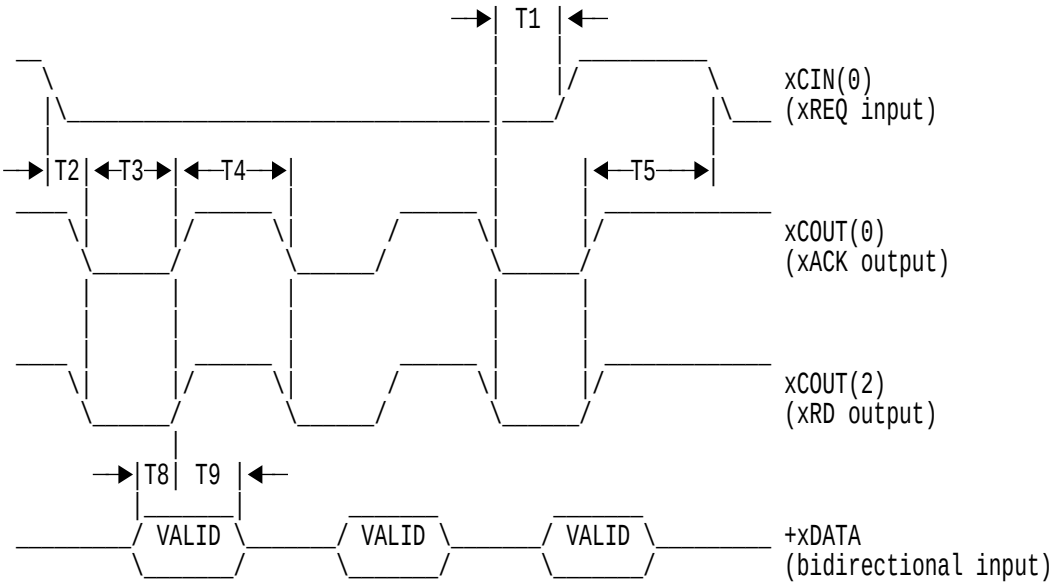
**Notes:**

1. If T4 is 3 clock cycles or greater, then the maximum T1 is 29 ns {33 ns}.
2. If T4 is 3 clock cycles or greater, then the maximum T6 is 25 ns.
3. If only one xACK active interval occurs during one xREQ cycle, then T4 does not exist.

Figure 4-13 (Part 2 of 2). Burst Device Timing. When using this figure, replace "x" by "O" only or "C" only, as appropriate. Negative active timings are shown. Positive active timing values are given in brackets { } when different from the negative active timing values.




Out of ALDC1-40S-M




Into ALDC1-40S-M

Figure 4-14 (Part 1 of 2). Burst Controller Timing

| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | Last xACK active to xREQ inactive - Ending Burst | 0 ns | 2 clock cycles |
| T2 | xREQ active to xACK active - Starting Burst | 1 clock cycle | |
| T3 | xACK active to xACK inactive | 2 clock cycles – 5 ns | 2 clock cycles<br>{2 clock cycles + 5 ns} |
| T4 | xACK inactive to xACK active | 2 clock cycles<br>{2 clock cyccles – 5 ns} | |
| T5 | Last xACK inactive to next xREQ active - Start new burst | 2 clock cycles | |
| T6 | +xDATA valid after xACK inactive | 1 clock cycle – 5 ns<br>{1 clock cycle – 9 ns} | 1 clock cycle + 8 ns |
| T7 | +xDATA valid after xACK active | 1 clock cycle – 5 ns | 1 clock cycle + 5 ns<br>{1 clock cycle + 9 ns} |
| T8 | +xDATA valid before xACK inactive | 12 ns<br>{16 ns} | |
| T9 | +xDATA hold time after xACK inactive | 0 ns | |

Figure 4-14 (Part 2 of 2). Burst Controller Timing. When using this figure, replace "x" by "O" only or "C" only, as appropriate. Negative active timings are shown. Positive active timing values are given in brackets { } when different from the negative active timing values.

### 4.3.3 Synchronous Mode

This mode allows fast data transfers up to 40 MB/s in which a one or two bytes of data are transferred every cycle at the activating edge of an externally supplied clock.

To transmit, the ALDC1-40S-M activates xREADY indicating +xDATA is valid. The receiver activates both xCS and xENABLE to accept +xDATA. The ALDC1-40S-M may generate new +xDATA on the next rising edge of +OSC.

In receiving mode, the ALDC1-40S-M activates xREADY indicating it is waiting for valid +xDATA. The transmitter activates both xCS and xENABLE to validate +xDATA. The ALDC1-40S-M accepts +xDATA on the next rising edge of +OSC.

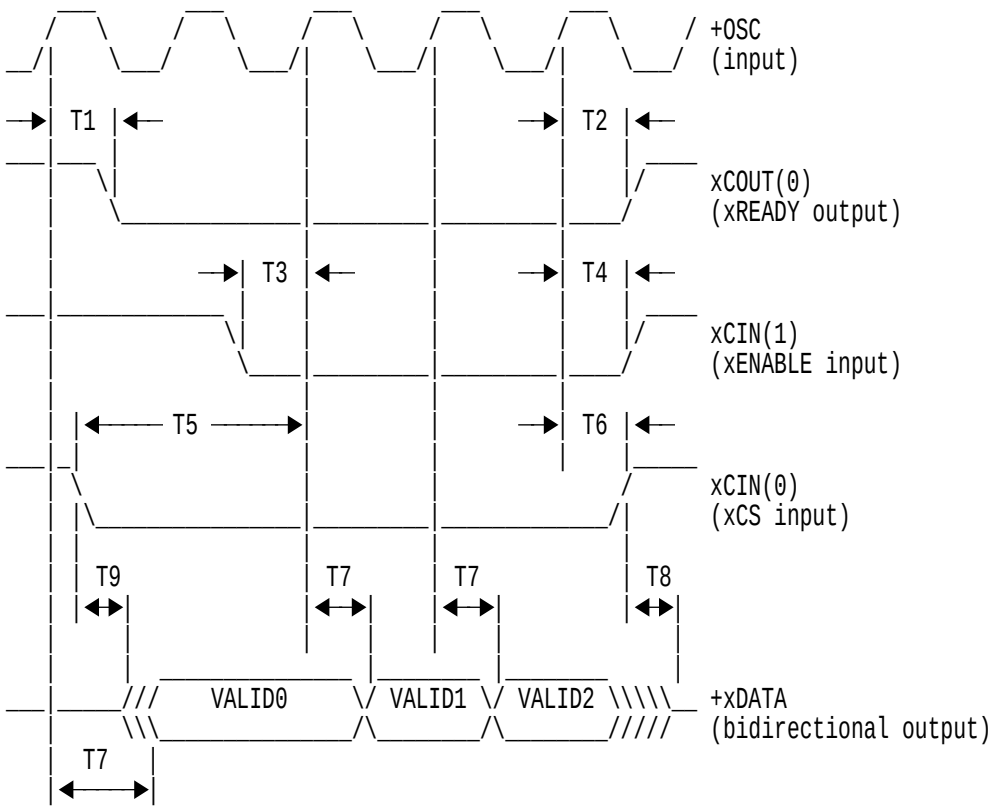
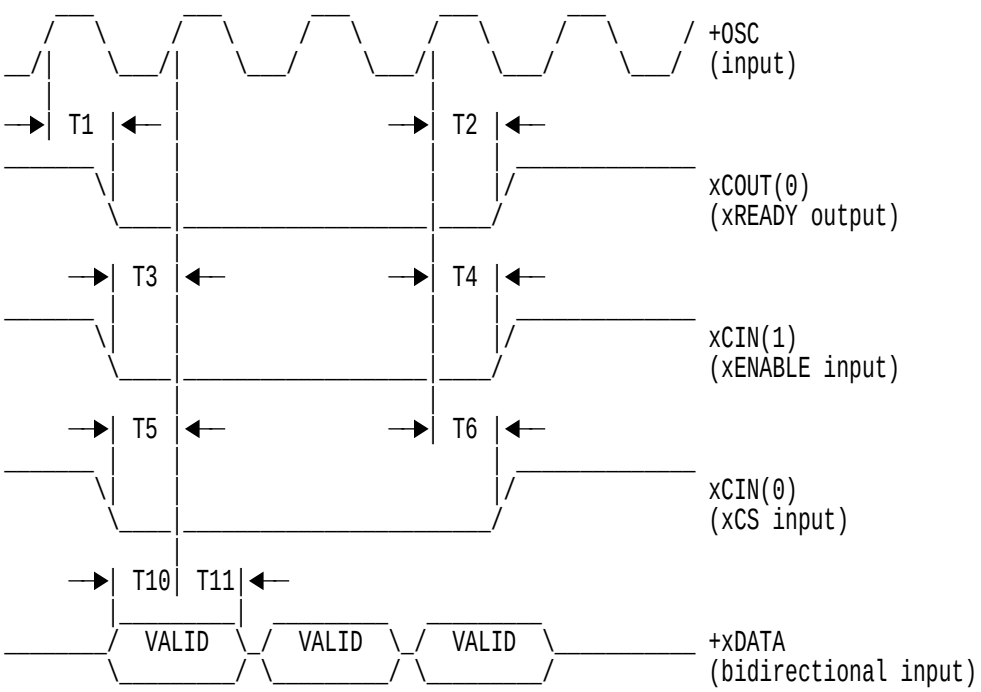



Figure 4-15 (Part 1 of 3). Synchronous Timing




Into ALDC1-40S-M

Figure 4-15 (Part 2 of 3). Synchronous Timing

| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | Low to high transition of +OSC to xREADY active | 8 ns | 31 ns |
| T2 | Low to high transition of +OSC to xREADY inactive | 8 ns | 31 ns |
| T3 | xENABLE active to low to high transition of +OSC | 13 ns | |
| T4 | Low to high transition of +OSC to xENABLE inactive | 5 ns | |
| T5 | xCS active to low to high transition of +OSC | 13 ns | |
| T6 | Low to high transition of +OSC to xCS inactive | 5 ns | |
| T7 | Low to high transition of +OSC to +xDATA valid | 9 ns | 35 ns |
| T8 | +xDATA disable time after xCS inactive | 4 ns | 20 ns |
| T9 | +xDATA enable time after xCS active | 4 ns | 20 ns |
| T10 | +xDATA valid before low to high transition of +OSC | 6 ns | |
| T11 | +xDATA hold time after low to high transition of +OSC | 5 ns | |

Figure 4-15 (Part 3 of 3). Synchronous Timing. When using this figure, replace "x" by "O" only or "C" only, as appropriate. Negative active timings are shown. Positive active timing values and negative active timing values are identical.

### 4.3.4 Peripheral Access Mode

Peripheral access allows the microprocessor to write to and read from a peripheral connected to the original data interface or compressed data interface. This mode is a relatively slow, asynchronous transfer.

**Note:** Peripheral access mode is used by the microprocessor to program the peripheral and is not allowed during a data transfer operation.

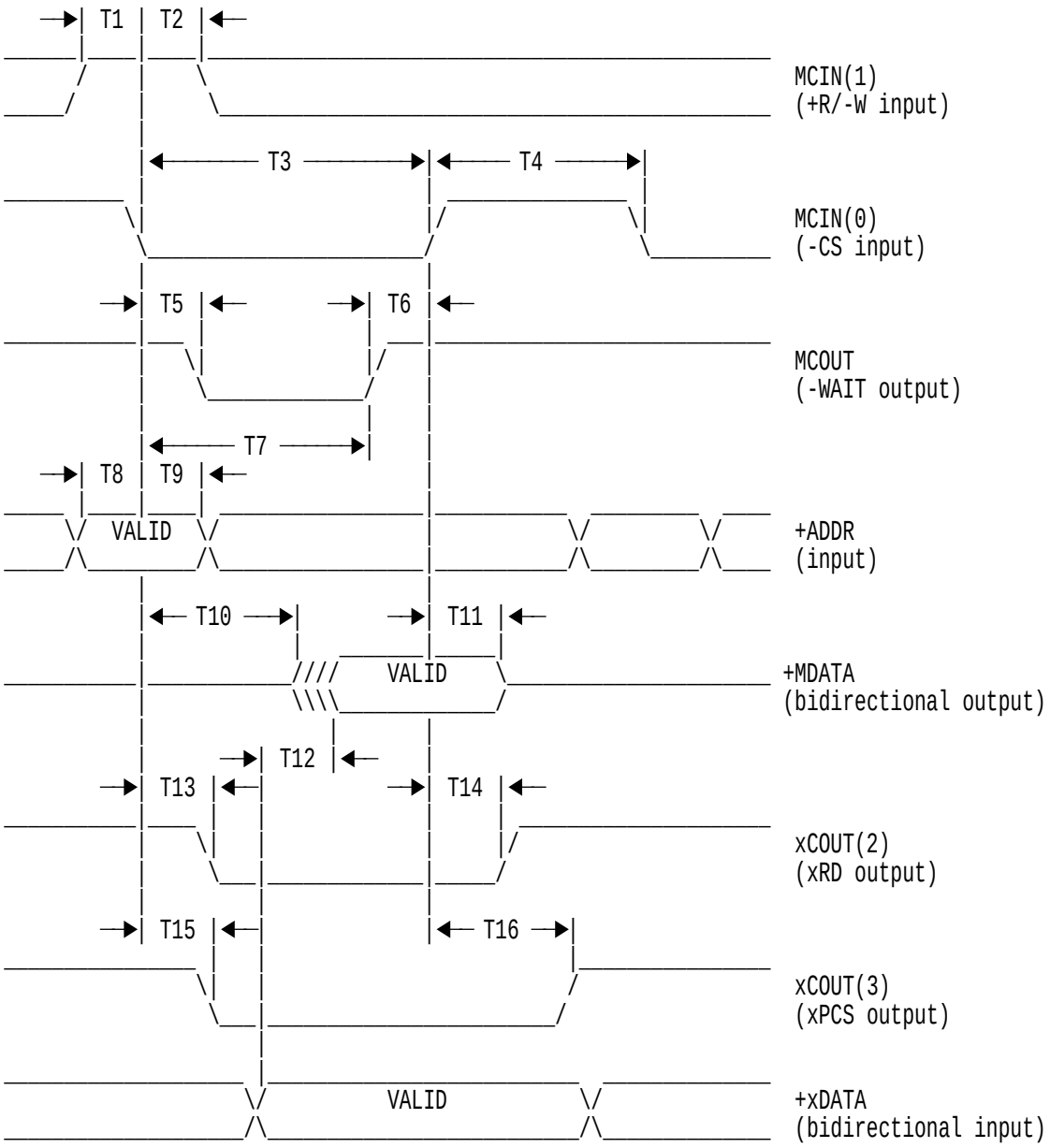



Figure 4-16 (Part 1 of 2). Peripheral Access Read Timing with MMODE Tied High

| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | +R/-W high before -CS active | 0.5 ns | |
| T2 | +R/-W high after -CS active | 3.5 ns | |
| T3 | -CS active to -CS inactive (See notes 1 and 2.) | (n+ 1) clock cycles | |
| T4 | -CS inactive to -CS active | 2 clock cycles | |
| T5 | -WAIT active after -CS active | 5 ns | 17.5 ns |
| T6 | -CS inactive after -WAIT inactive (See note 1.) | 0 ns | |
| T7 | -WAIT inactive after -CS active (See note 2.) | n clock cycles | (n+ 1) clock cycles + 18 ns |
| T8 | +ADDR valid before -CS active | 0 ns | |
| T9 | +ADDR hold time after -CS active | 5 ns | |
| T10 | +MDATA enable time after -CS active | 1 clock cycle + 6 ns | 2 clock cycles + 21.5 ns |
| T11 | +MDATA disable time after -CS inactive | 1 clock cycle + 5.5 ns | 2 clock cycle + 20 ns |
| T12 | Delay from +xDATA valid to +MDATA valid (See note 3.) | 0 ns | 24.5 ns |
| T13 | xRD active after -CS active | 1 clock cycle | 2 clock cycles + 17 ns |
| T14 | xRD inactive after -CS inactive | 1 clock cycle | 2 clock cycles + 12.5 ns<br>{2 clock cycles + 16.5 ns} |
| T15 | xPCS active after -CS active | 1 clock cycle | 2 clock cycles + 16 ns |
| T16 | xPCS inactive after -CS inactive | 1 clock cycle | 2 clock cycles + 12 ns<br>{2 clock cycles + 16 ns} |

**Notes:**

1. When using -WAIT to control -CS inactive, ignore T3. Otherwise, ignore T6.
2. n is the value stored in register xCNF(6:4). ($1 \leq n \leq 7$)
3. If +MENABLEP is tied low, maximum T12 is 19.5 ns.

**Usage note:** The microprocessor interface latches the address on the falling edge of -CS. The user should latch output data on the rising edge of -CS.

**Important!**

See ALDC1-40S-M Design Note 2 on page ii.

Figure 4-16 (Part 2 of 2). Peripheral Access Read Timing with MMODE Tied High. When using this figure, replace "x" by "O" only or "C" only, as appropriate. Negative active timings are shown. Positive active timing values are given in brackets { } when different from the negative active timing values.

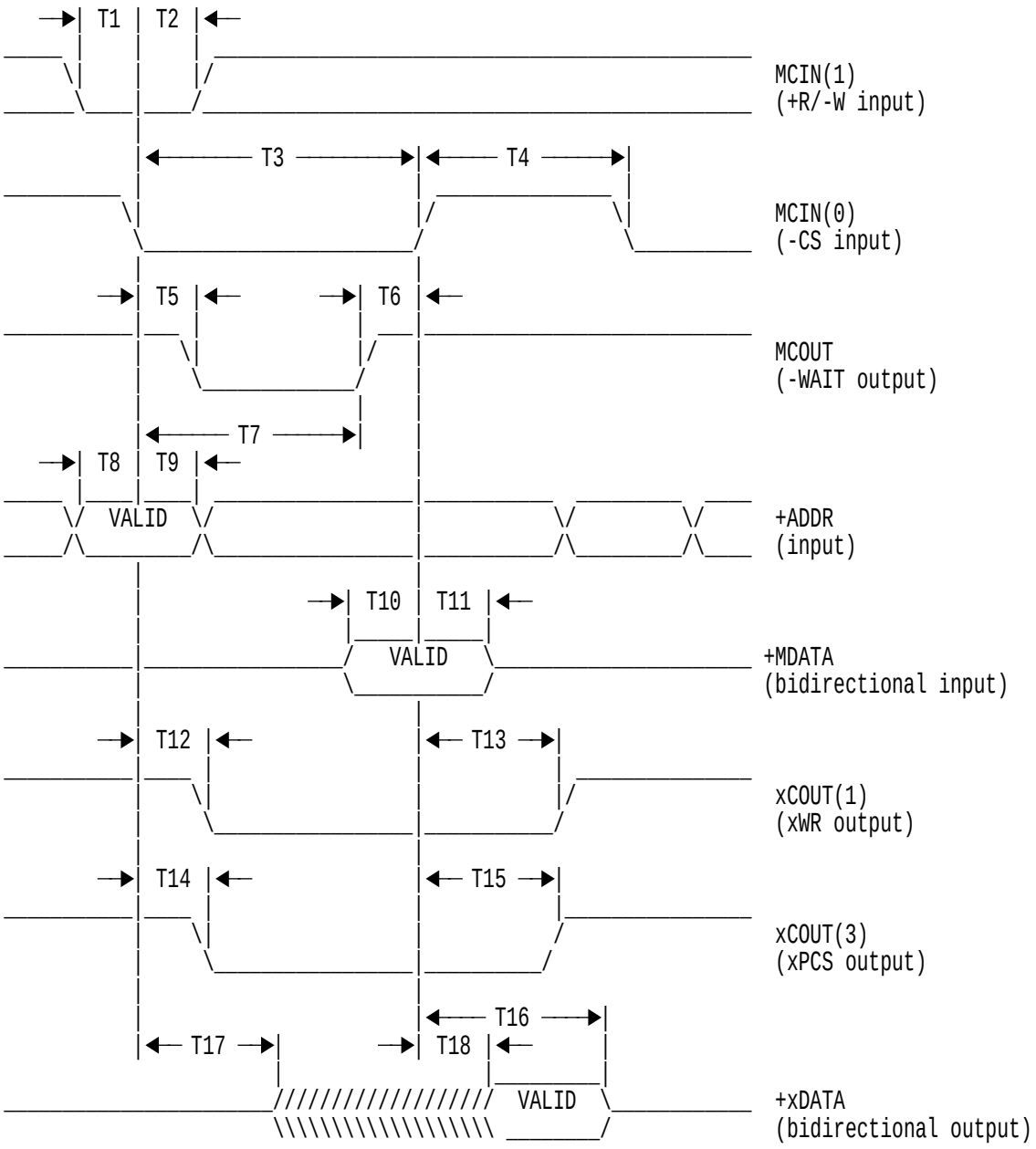



Figure 4-17 (Part 1 of 2). Peripheral Access Write Timing with MMODE Tied High

| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | +R/-W low before -CS active | 0.5 ns | |
| T2 | +R/-W low after -CS active | 3.5 ns | |
| T3 | -CS active to -CS inactive (See notes 1 and 2.) | (n+1) clock cycles | |
| T4 | -CS inactive to -CS active | 3 clock cycles | |
| T5 | -WAIT active after -CS active | 5 ns | 17.5 ns |
| T6 | -CS inactive after -WAIT inactive (See note 1.) | 0 ns | |
| T7 | -WAIT inactive after -CS active (See note 2.) | n clock cycles | (n+ 1) clock cycles + 18 ns |
| T8 | +ADDR valid before -CS active | 0 ns | |
| T9 | +ADDR hold time after -CS active | 5 ns | |
| T10 | +MDATA valid before -CS inactive | 2.5 ns | |
| T11 | +MDATA hold time after -CS inactive | 3.5 ns | |
| T12 | xWR active after -CS active | 1 clock cycle | 2 clock cycles + 17 ns |
| T13 | xWR inactive after -CS inactive | 1 clock cycle | 2 clock cycles + 12.5 ns<br>{2 clock cycles + 16.5 ns} |
| T14 | xPCS active after -CS active | 1 clock cycle | 2 clock cycles + 16 ns |
| T15 | xPCS inactive after -CS inactive | 1 clock cycle | 2 clock cycles + 12 ns<br>{2 clock cycles + 16 ns} |
| T16 | +xDATA disable time after -CS inactive | 2 clock cycles | 3 clock cycles + 17.5 ns |
| T17 | +xDATA enable time after -CS active | 1 clock cycle | 2 clock cycles + 13.5 ns |
| T18 | +xDATA valid after -CS inactive | 3.5 ns | 18.5 ns |

**Notes:**

1. When using -WAIT to control -CS inactive, ignore T3. Otherwise, ignore T6.
2. n is the value stored in register xCNF(6:4). ($1 \leq n \leq 7$)

**Usage note:** The microprocessor interface latches the address on the falling edge of -CS. The Microprocessor Interface latches input data on the rising edge of -CS.

Figure 4-17 (Part 2 of 2). Peripheral Access Write Timing with MMODE Tied High. When using this figure, replace "x" by "O" only or "C" only, as appropriate. Negative active timings are shown. Positive active timing values are given in brackets { } when different from the negative active timing values.

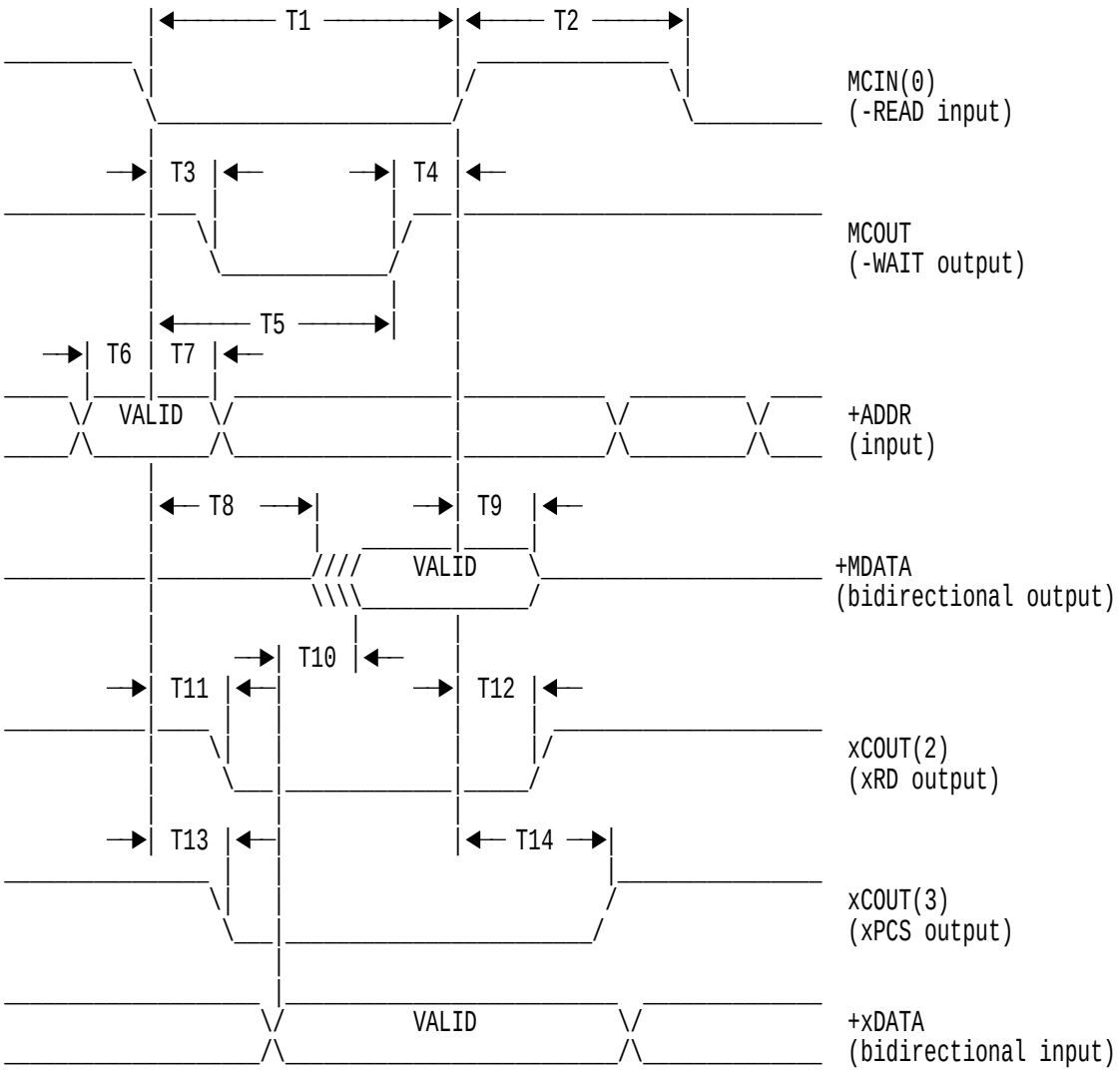



Figure 4-18 (Part 1 of 2). Peripheral Access Read Timing with MMODE Tied Low

| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | -READ active to -READ inactive (See notes 1 and 2.) | (n+ 1) clock cycles | |
| T2 | -READ inactive to -READ active | 2 clock cycles | |
| T3 | -WAIT active after -READ active | 7.5 ns | 17 ns |
| T4 | -READ inactive after -WAIT inactive (See note 1.) | 0 ns | |
| T5 | -WAIT inactive after -READ active (See note 2.) | n clock cycles | (n+ 1) clock cycles + 18 ns |
| T6 | +ADDR valid before -READ active | 0 ns | |
| T7 | +ADDR hold time after -READ active | 5.5 ns | |
| T8 | +MDATA enable time after -READ active | 1 clock cycle | 2 clock cycles + 21.5 ns |
| T9 | +MDATA disable time after -READ inactive | 1 clock cycle | 2 clock cycles + 20 ns |
| T10 | Delay from +xDATA valid to +MDATA valid (See note 3.) | 0 ns | 24.5 ns |
| T11 | xRD active after -READ active | 1 clock cycle | 2 clock cycles + 17 ns |
| T12 | xRD inactive after -READ inactive | 1 clock cycle | 2 clock cycles + 12.5 ns<br>{2 clock cycles + 16.5 ns} |
| T13 | xPCS active after -READ active | 1 clock cycle | 2 clock cycles + 16 ns |
| T14 | xPCS inactive after -READ inactive | 1 clock cycle | 2 clock cycles + 12 ns<br>{2 clock cycles + 16 ns} |

**Notes:**

1. When using -WAIT to control -READ inactive, ignore T1. Otherwise, ignore T4.
2. n is the value stored in register xCNF(6:4). ($1 \leq n \leq 7$)
3. If +MENABLEP is tied low, maximum T10 is 19.5 ns.

**Usage note:** The microprocessor interface latches the address on the falling edge of -READ. The user should latch output data on the rising edge of -READ.

**Note:** -WRITE must be inactive during all transfers out of the Microprocessor Interface.

**Important!**

See ALDC1-40S-M Design Note 2 on page ii.

Figure 4-18 (Part 2 of 2). Peripheral Access Read Timing with MMODE Tied Low. When using this figure, replace "x" by "O" only or "C" only, as appropriate. Negative active timings are shown. Positive active timing values are given in brackets { } when different from the negative active timing values.

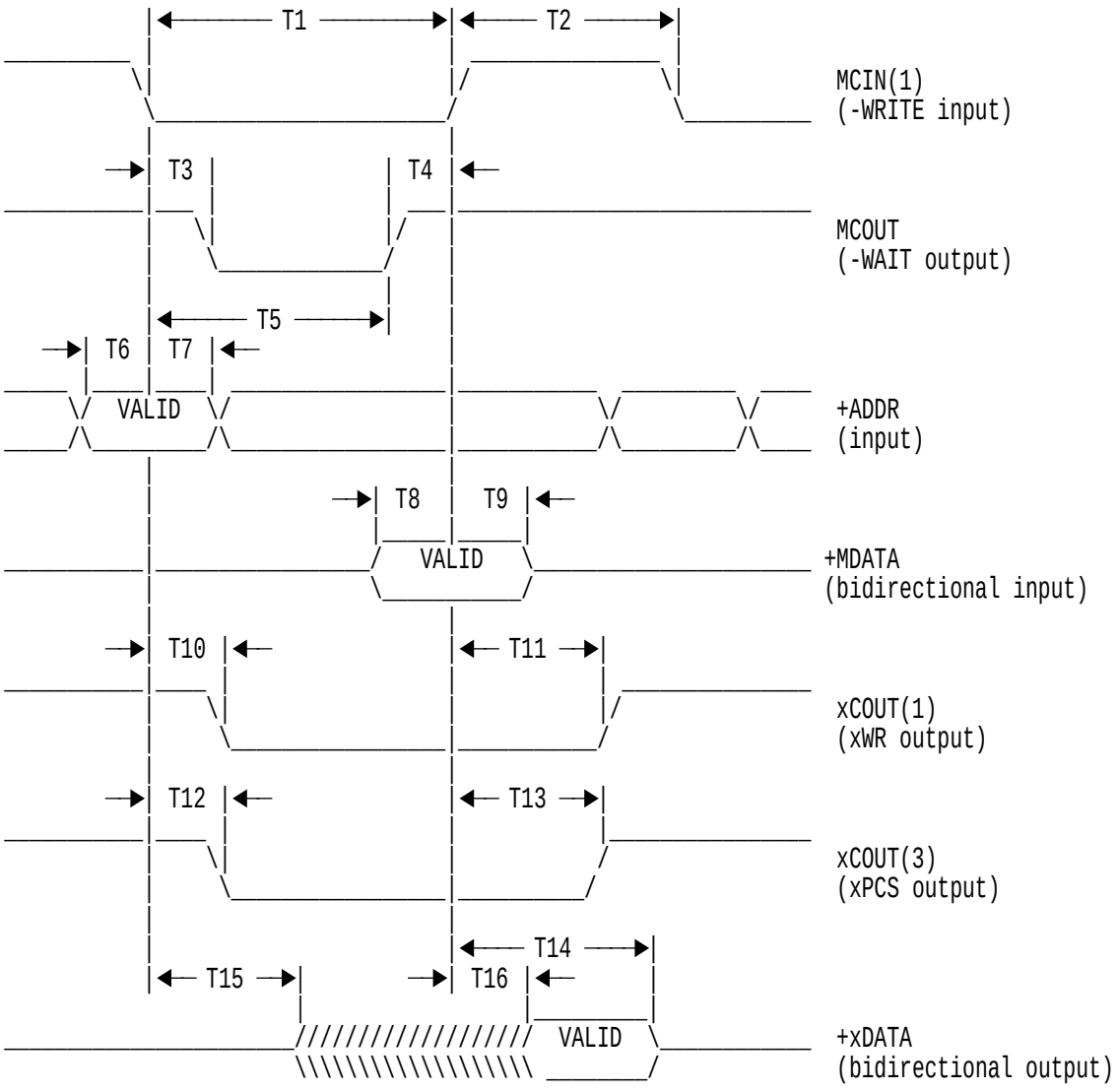



Figure 4-19 (Part 1 of 2). Peripheral Access Write Timing with MMODE Tied Low

| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | -WRITE active to -WRITE inactive (See notes 1 and 2.) | (n+ 1) clock cycles | |
| T2 | -WRITE inactive to -WRITE active | 3 clock cycles | |
| T3 | -WAIT active after -WRITE active | 7.5 ns | 17 ns |
| T4 | -WAIT inactive before -WRITE inactive (See note 1.) | 0 ns | |
| T5 | -WAIT inactive after -WRITE active (See note 2.) | n clock cycles | (n+ 1) clock cycles + 18 ns |
| T6 | +ADDR valid before -WRITE active | 0 ns | |
| T7 | +ADDR hold time after -WRITE active | 5.5 ns | |
| T8 | +MDATA valid before -WRITE inactive | 2.5 ns | |
| T9 | +MDATA hold time after -WRITE inactive | 4.5 ns | |
| T10 | xWR active after -WRITE active | 1 clock cycle | 2 clock cycles + 17 ns |
| T11 | xWR inactive after -WRITE inactive | 1 clock cycle | 2 clock cycles + 12.5 ns<br>{2 clock cycles + 16.5 ns} |
| T12 | xPCS active after -WRITE active | 1 clock cycle | 2 clock cycles + 16 ns |
| T13 | xPCS inactive after -WRITE inactive | 1 clock cycle | 2 clock cycles + 12 ns<br>{2 clock cycles + 16 ns} |
| T14 | +xDATA disable time after -WRITE inactive | 2 clock cycle | 3 clock cycles + 17.5 ns |
| T15 | +xDATA enable time after -WRITE active | 1 clock cycle | 2 clock cycles + 13.5 ns |
| T16 | +xDATA valid after -WRITE inactive | 3.5 ns | 18.5 ns |

**Notes:**

1. When using -WAIT to control -WRITE inactive, ignore T1. Otherwise, ignore T4.
2. n is the value stored in register xCNF(6:4). ($1 \leq n \leq 7$)

**Usage note:** The microprocessor interface latches the address on the falling edge of -WRITE. The Microprocessor Interface latches input data on the rising edge of -WRITE.

**Note:** -READ must be inactive during all transfers into the Microprocessor Interface.

Figure 4-19 (Part 2 of 2). Peripheral Access Write Timing with MMODE Tied Low. When using this figure, replace "x" by "O" only or "C" only, as appropriate. Negative active timings are shown. Positive active timing values are given in brackets { } when different from the negative active timing values.

## 4.3.5 FIFO Operation

The original data interface and compressed data interface both contain sixteen-byte FIFO's that allow the user to optimize bus performance by providing configurable FIFO thresholds.

These FIFO's are reset to empty by a hardware reset, a software reset, or a data transfer operation.

**Note:** The Original Data Interface FIFO Threshold (OCNF(3:0)) bits and the Compressed Data Interface FIFO Threshold (CCNF(3:0)) bits are independently configurable. In the discussion below, these threshold bits are called the **xFIFO threshold**, where the "x" is replaced by "O" only or "C" only, as appropriate.

The xFIFO threshold is written into the respective xCNF register through the microprocessor interface. The xFIFO threshold may take on any value from B'0000' to B'1111'.

### 4.3.5.1 Four-edge and Burst Devices

When the original data interface or compressed data interface is configured as a four-edge or burst device, then the xFIFO threshold is used to trigger when xREQ activates and deactivates.

When transferring data out of the original data interface or compressed data interface, xREQ activates when the number of available bytes in the xFIFO is greater than or equal to the xFIFO threshold. The xREQ signal remains active until the xFIFO is empty. When the xFIFO is empty, xREQ deactivates.

**Note:** The xREQ signal also activates when, during compression, the Original Data Interface Transfer Count (TCO) register (or, during decompression, the Compressed Data Interface Transfer Count (TCC) register) equals the Transfer Size (XFR) register. This condition indicates that all bytes in the current data operation have been received and that only transfers out of the compressed data interface (or original data interface, respectively) remain.

When transferring data into the original data interface or compressed data interface, xREQ activates at the beginning of the transfer. When the xFIFO is full, xREQ deactivates. The xREQ signal activates each time the number of empty byte locations in the xFIFO is greater than or equal to the xFIFO threshold. The xREQ signal remains active until the xFIFO is full.

### 4.3.5.2 Four-edge and Burst Controllers

When the original data interface or compressed data interface is configured as a four-edge or burst controller, then the xFIFO threshold is used to trigger when xACK activates and deactivates. The xFIFO conditions which cause xACK to activate and deactivate are identical to those which cause xREQ to activate and deactivate when configured as a four-edge or burst device. See section 4.3.5.1 above.

**Note:** The xACK signal can only be active after the original data interface or compressed data interface receives an active xREQ regardless of the xFIFO threshold.

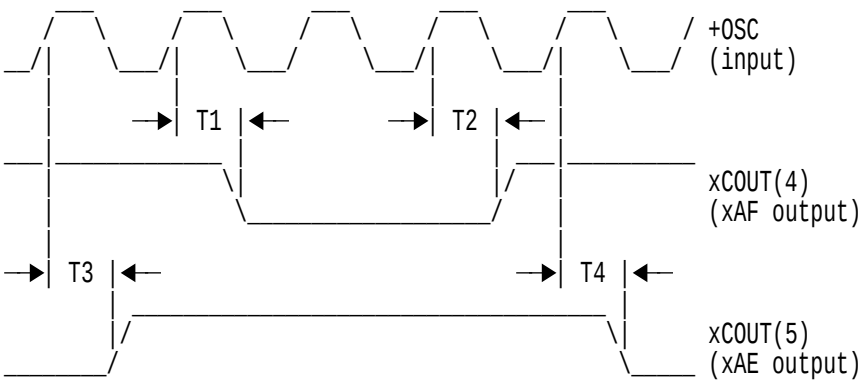
## 4.3.6 Almost Full and Almost Empty

The AImost Full (xAF) and AImost Empty (xAE) signals are always available to the user. The xAF signal can be used to perform a look-ahead stop when transferring data into the original data interface or compressed data interface. The xAE signal can be used to perform a look-ahead stop when transferring data out of the original data interface or compressed data interface.

The xAF signal deactivates when a transfer operation begins. The xAF signal activates the clock cycle after the number of empty byte locations in the xFIFO is less than or equal to the xFIFO threshold. The xAF signal deactivates the clock cycle after the number of empty byte locations in the xFIFO is greater than the xFIFO threshold.

The xAE signal activates when a transfer operation begins. The xAE signal deactivates the clock cycle after the number of available bytes in the xFIFO is greater than the xFIFO threshold. The xAE signal activates the clock cycle after the number of available bytes in the xFIFO is less than or equal to the xFIFO threshold.

See Figure 4-20 on page 4-29 for details.




| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | Low to high transition of +OSC to xAF active | 7 ns | 26 ns |
| T2 | Low to high transition of +OSC to xAF inactive | 7 ns | 26 ns |
| T3 | Low to high transition of +OSC to xAE inactive | 7 ns | 26 ns |
| T4 | Low to high transition of +OSC to xAE active | 7 ns | 26 ns |

Figure 4-20. Almost Full and Almost Empty Timing. When using this figure, replace "x" by "O" only or "C" only, as appropriate. Negative active timings are shown. Positive active timing values and negative active timing values are identical.

## 4.4 Clock Interface

The +OSC signal is the clock input for ALDC1-40S-M. The timings for the microprocessor interface, original data interface, and compressed data interface are specified relative to the clock timing.

The clock interface is shown in Figure 4-21. Detailed clock timing information is given in Figure 4-22 on page 4-30.

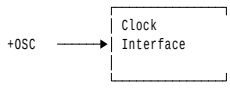
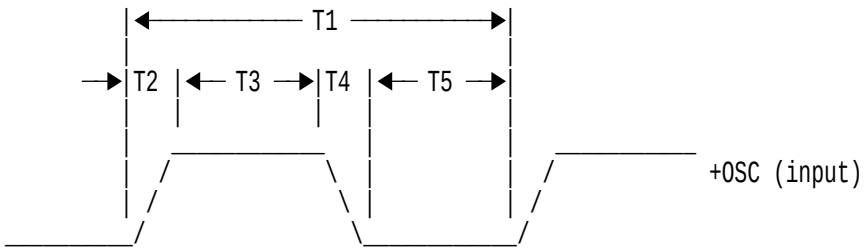



Figure 4-21. Clock Interface




| REF | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| T1 | +OSC period | 25 ns | |
| T2 | +OSC rise time | | 4 ns |
| T3 | +OSC width high | 8.5 ns | |
| T4 | +OSC fall time | | 4 ns |
| T5 | +OSC width low | 8.5 ns | |

Figure 4-22. Clock Timing

# Chapter 5. Pin Description

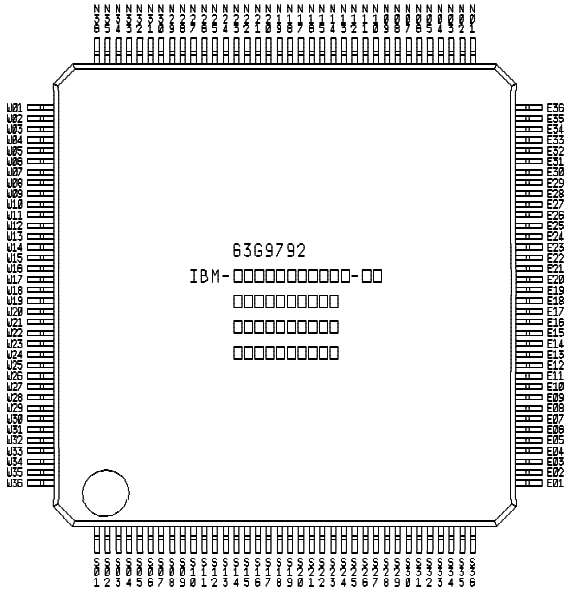



Figure 5-1. ALDC1-40S-M Pin Numbering Diagram. Module is viewed from top. See Figure 5-2 for the corresponding pin names, signal directions, and descriptions.

Figure 5-2 (Page 1 of 9). ALDC1-40S-M Pin Description. See Figure 5-1 to identify pin locations.

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| N01 | GND | | A ground pin. |
| N02 | +ODATA(15) | bid | The original data interface data bit 15 pin. May be tied high, tied low, or not connected when not enabled.<br>+ODATA(15) is enabled by setting OCNF(10) to B'1'. |
| N03 | +ODATA(14) | bid | The original data interface data bit 14 pin. May be tied high, tied low, or not connected when not enabled.<br>+ODATA(14) is enabled by setting OCNF(10) to B'1'. |
| N04 | -TEST | in | A manufacturing test input. Must be tied high. |
| N05 | OCIN(0) | in | The original data interface control input bit 0 pin. When OCNF(13:12) is set to B'10', this pin is used as the OREQ signal. When OCNF(13:12) is set to B'00', this pin is used as the OACK signal. When OCNF(12) is set to B'1', this pin is used as the OCS signal. See Figure 4-2 on page 4-1.<br>The polarity of OCIN(0) is controlled by OPOL(7). |
| N06 | GND | | A ground pin. |

Figure 5-2 (Page 2 of 9). ALDC1-40S-M Pin Description. See Figure 5-1 on page 5-1 to identify pin locations.

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| N07 | OCIN(1) | in | The original data interface control input bit 1 pin. When OCNF(12) is set to B'1', this pin is used as the OENABLE signal. See Figure 4-2 on page 4-1.<br>The polarity of OCIN(1) is controlled by OPOL(6). |
| N08 | Vdd | | A +5 Volt power supply pin. |
| N09 | +ODATA(13) | bid | The original data interface data bit 13 pin. May be tied high, tied low, or not connected when not enabled.<br>+ODATA(13) is enabled by setting OCNF(10) to B'1'. |
| N10 | +ODATA(12) | bid | The original data interface data bit 12 pin. May be tied high, tied low, or not connected when not enabled.<br>+ODATA(12) is enabled by setting OCNF(10) to B'1'. |
| N11 | +ODATA(11) | bid | The original data interface data bit 11 pin. May be tied high, tied low, or not connected when not enabled.<br>+ODATA(11) is enabled by setting OCNF(10) to B'1'. |
| N12 | GND | | A ground pin. |
| N13 | +ODATA(10) | bid | The original data interface data bit 10 pin. May be tied high, tied low, or not connected when not enabled.<br>+ODATA(10) is enabled by setting OCNF(10) to B'1'. |
| N14 | +ODATA(09) | bid | The original data interface data bit 9 pin. May be tied high, tied low, or not connected when not enabled.<br>+ODATA(09) is enabled by setting OCNF(10) to B'1'. |
| N15 | Vdd | | A +5 Volt power supply pin. |
| N16 | +ODATA(08) | bid | The original data interface data bit 8 pin. May be tied high, tied low, or not connected when not enabled.<br>+ODATA(08) is enabled by setting OCNF(10) to B'1'. |
| N17 | +OPARITY(1) | bid | The original data interface parity bit 1 pin. When enabled, this pin checks parity on input and generates parity on output for the associated +ODATA(08) through +ODATA(15) pins. May be tied high, tied low, or not connected when not enabled.<br>+OPARITY(1) is enabled by setting OCNF(15) and OCNF(10) to B'1'. |
| N18 | GND | | A ground pin. |
| N19 | Vdd | | A +5 Volt power supply pin. |
| N20 | MCIN(0) | in | The microprocessor interface control input bit 0 pin. When MMODE is high, this pin is used as the -CS signal. When MMODE is low, this pin is used as the -READ signal. |
| N21 | MCIN(1) | in | The microprocessor interface control input bit 1 pin. When MMODE is high, this pin is used as the +R/-W signal. When MMODE is low, this pin is used as the -WRITE signal. |

Figure 5-2 (Page 3 of 9). ALDC1-40S-M Pin Description. See Figure 5-1 on page 5-1 to identify pin locations.

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| N22 | +MDATA(15) | bid | The microprocessor interface data bit 15 pin. May be tied high, tied low, or not connected when not enabled.<br>+MDATA(15) is enabled by tieing +M1BYTE low. |
| N23 | +MDATA(14) | bid | The microprocessor interface data bit 14 pin. May be tied high, tied low, or not connected when not enabled.<br>+MDATA(14) is enabled by tieing +M1BYTE low. |
| N24 | GND | | A ground pin. |
| N25 | +MDATA(13) | bid | The microprocessor interface data bit 13 pin. May be tied high, tied low, or not connected when not enabled.<br>+MDATA(13) is enabled by tieing +M1BYTE low. |
| N26 | +MDATA(12) | bid | The microprocessor interface data bit 12 pin. May be tied high, tied low, or not connected when not enabled.<br>+MDATA(12) is enabled by tieing +M1BYTE low. |
| N27 | +MDATA(11) | bid | The microprocessor interface data bit 11 pin. May be tied high, tied low, or not connected when not enabled.<br>+MDATA(11) is enabled by tieing +M1BYTE low. |
| N28 | +MDATA(10) | bid | The microprocessor interface data bit 10 pin. May be tied high, tied low, or not connected when not enabled.<br>+MDATA(10) is enabled by tieing +M1BYTE low. |
| N29 | Vdd | | A +5 Volt power supply pin. |
| N30 | +MDATA(09) | bid | The microprocessor interface data bit 9 pin. May be tied high, tied low, or not connected when not enabled.<br>+MDATA(09) is enabled by tieing +M1BYTE low. |
| N31 | +MDATA(08) | bid | The microprocessor interface data bit 8 pin. May be tied high, tied low, or not connected when not enabled.<br>+MDATA(08) is enabled by tieing +M1BYTE low. |
| N32 | MCOUT | out | The microprocessor interface control output pin. This pin is used as the -WAIT signal. |
| N33 | -TEST | in | A manufacturing test input. Must be tied high. |
| N34 | GND | | A ground pin. |
| N35 | +MPARITY(1) | bid | The microprocessor interface parity bit 1 pin. When enabled, this pin checks parity on input and generates parity on output for the associated +MDATA(08) through +MDATA(15) pins. May be tied high, tied low, or not connected when not enabled.<br>+MPARITY(1) is enabled by tieing +MENABLEP high and tieing +M1BYTE low. |
| N36 | Vdd | | A +5 Volt power supply pin. |
| W01 | GND | | A ground pin. |
| W02 | +MDATA(07) | bid | The microprocessor interface data bit 7 pin. |
| W03 | +MDATA(06) | bid | The microprocessor interface data bit 6 pin. |

Figure 5-2 (Page 4 of 9). ALDC1-40S-M Pin Description. See Figure 5-1 on page 5-1 to identify pin locations.

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| W04 | +MDATA(05) | bid | The microprocessor interface data bit 5 pin. |
| W05 | Vdd | | A +5 Volt power supply pin. |
| W06 | -TEST | in | A manufacturing test input. Must be tied high. |
| W07 | -TEST | in | A manufacturing test input. Must be tied high. |
| W08 | +M1BYTE | in | The microprocessor interface data bus width selector pin. |
| W09 | +MDATA(04) | bid | The microprocessor interface data bit 4 pin. |
| W10 | GND | | A ground pin. |
| W11 | +MDATA(03) | bid | The microprocessor interface data bit 3 pin. |
| W12 | +MDATA(02) | bid | The microprocessor interface data bit 2 pin. |
| W13 | +MDATA(01) | bid | The microprocessor interface data bit 1 pin. |
| W14 | Vdd | | A +5 Volt power supply pin. |
| W15 | +MDATA(00) | bid | The microprocessor interface data bit 0 pin. |
| W16 | +MPARITY(0) | bid | The microprocessor interface parity bit 0 pin. When enabled, this pin checks parity on input and generates parity on output for the associated +MDATA(00) through +MDATA(07) pins. May be tied high, tied low, or not connected when not enabled.<br>+MPARITY(0) is enabled by tieing +MENABLEP high. |
| W17 | -TEST | in | A manufacturing test input. Must be tied high. |
| W18 | GND | | A ground pin. |
| W19 | Vdd | | A +5 Volt power supply pin. |
| W20 | +CDATA(07) | bid | The compressed data interface data bit 7 pin. |
| W21 | +CDATA(06) | bid | The compressed data interface data bit 6 pin. |
| W22 | GND | | A ground pin. |
| W23 | +CDATA(05) | bid | The compressed data interface data bit 5 pin. |
| W24 | +CDATA(04) | bid | The compressed data interface data bit 4 pin. |
| W25 | Vdd | | A +5 Volt power supply pin. |
| W26 | +CDATA(03) | bid | The compressed data interface data bit 3 pin. |
| W27 | +CDATA(02) | bid | The compressed data interface data bit 2 pin. |
| W28 | GND | | A ground pin. |
| W29 | +CDATA(01) | bid | The compressed data interface data bit 1 pin. |
| W30 | +CDATA(00) | bid | The compressed data interface data bit 0 pin. |
| W31 | Vdd | | A +5 Volt power supply pin. |
| W32 | +CPARITY(0) | bid | The compressed data interface parity bit 0 pin. When enabled, this pin checks parity on input and generates parity on output for the associated +CDATA(00) through +CDATA(07) pins. May be tied high, tied low, or not connected when not enabled.<br>+CPARITY(0) is enabled by setting CCNF(15) to B'1'. |

Figure 5-2 (Page 5 of 9). ALDC1-40S-M Pin Description. See Figure 5-1 on page 5-1 to identify pin locations.

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| W33 | -TIE | in | Must be tied low. |
| W34 | GND | | A ground pin. |
| W35 | | | Unused. May be tied high, tied low, or not connected. |
| W36 | Vdd | | A +5 Volt power supply pin. |
| S01 | GND | | A ground pin. |
| S02 | +CDATA(15) | bid | The compressed data interface data bit 15 pin. May be tied high, tied low, or not connected when not enabled. +CDATA(15) is enabled by setting CCNF(10) to B'1'. |
| S03 | Vdd | | A +5 Volt power supply pin. |
| S04 | | | A test output. Must not be connected. |
| S05 | +MENABLEP | in | The microprocessor interface parity enable pin. |
| S06 | GND | | A ground pin. |
| S07 | +CDATA(14) | bid | The compressed data interface data bit 14 pin. May be tied high, tied low, or not connected when not enabled. +CDATA(14) is enabled by setting CCNF(10) to B'1'. |
| S08 | +CDATA(13) | bid | The compressed data interface data bit 13 pin. May be tied high, tied low, or not connected when not enabled. +CDATA(13) is enabled by setting CCNF(10) to B'1'. |
| S09 | Vdd | | A +5 Volt power supply pin. |
| S10 | +CDATA(12) | bid | The compressed data interface data bit 12 pin. May be tied high, tied low, or not connected when not enabled. +CDATA(12) is enabled by setting CCNF(10) to B'1'. |
| S11 | +CDATA(11) | bid | The compressed data interface data bit 11 pin. May be tied high, tied low, or not connected when not enabled. +CDATA(11) is enabled by setting CCNF(10) to B'1'. |
| S12 | GND | | A ground pin. |
| S13 | +CDATA(10) | bid | The compressed data interface data bit 10 pin. May be tied high, tied low, or not connected when not enabled. +CDATA(10) is enabled by setting CCNF(10) to B'1'. |
| S14 | +CDATA(09) | bid | The compressed data interface data bit 9 pin. May be tied high, tied low, or not connected when not enabled. +CDATA(09) is enabled by setting CCNF(10) to B'1'. |
| S15 | Vdd | | A +5 Volt power supply pin. |
| S16 | +CDATA(08) | bid | The compressed data interface data bit 8 pin. May be tied high, tied low, or not connected when not enabled. +CDATA(08) is enabled by setting CCNF(10) to B'1'. |

Figure 5-2 (Page 6 of 9). ALDC1-40S-M Pin Description. See Figure 5-1 on page 5-1 to identify pin locations.

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| S17 | +CPARITY(1) | bid | The compressed data interface parity bit 1 pin. When enabled, this pin checks parity on input and generates parity on output for the associated +CDATA(08) through +CDATA(15) pins. May be tied high, tied low, or not connected when not enabled.<br>+CPARITY(1) is enabled by setting CCNF(15) and CCNF(10) to B'1'. |
| S18 | GND | | A ground pin. |
| S19 | Vdd | | A +5 Volt power supply pin. |
| S20 | CCIN(0) | in | The compressed data interface control input bit 0 pin. When CCNF(13:12) is set to B'10', this pin is used as the CREQ signal. When CCNF(13:12) is set to B'00', this pin is used as the CACK signal. When CCNF(12) is set to B'1', this pin is used as the CCS signal. See Figure 4-2 on page 4-1.<br>The polarity of CCIN(0) is controlled by CPOL(7). |
| S21 | CCIN(1) | in | The compressed data interface control input bit 1 pin. When CCNF(12) is set to B'1', this pin is used as the CENABLE signal. See Figure 4-2 on page 4-1.<br>The polarity of CCIN(1) is controlled by CPOL(6). |
| S22 | +ADDR(4) | in | The microprocessor interface address bit 4 pin. |
| S23 | GND | | A ground pin. |
| S24 | CCOUT(0) | out | The compressed data interface control output bit 0 pin. When CCNF(13:12) is set to B'10', this pin is used as the CACK signal. When CCNF(13:12) is set to B'00', this pin is used as the CREQ signal. When CCNF(12) is set to B'1', this pin is used as the CREADY signal. See Figure 4-2 on page 4-1.<br>The polarity of CCOUT(0) is controlled by CPOL(5). |
| S25 | CCOUT(1) | out | The compressed data interface control output bit 1 pin. When CCNF(13:12) is set to B'10' or when the CMND register is set to X'C800', this pin is used as the CWR signal. See Figure 4-2 on page 4-1.<br>The polarity of CCOUT(1) is controlled by CPOL(4). |
| S26 | CCOUT(2) | out | The compressed data interface control output bit 2 pin. When CCNF(13:12) is set to B'10' or when the CMND register is set to X'C800', this pin is used as the CRD signal. See Figure 4-2 on page 4-1.<br>The polarity of CCOUT(2) is controlled by CPOL(3). |
| S27 | CCOUT(3) | out | The compressed data interface control output bit 3 pin. When the CMND register is set to X'C800', this pin is used as the CPCS signal. See Figure 4-2 on page 4-1.<br>The polarity of CCOUT(3) is controlled by CPOL(2). |
| S28 | Vdd | | A +5 Volt power supply pin. |

Figure 5-2 (Page 7 of 9). ALDC1-40S-M Pin Description. See Figure 5-1 on page 5-1 to identify pin locations.

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| S29 | CCOUT(4) | out | The compressed data interface control output bit 4 pin. This pin is used as the CAF signal. See Figure 4-2 on page 4-1.<br>The polarity of CCOUT(4) is controlled by CPOL(1). |
| S30 | +ADDR(3) | in | The microprocessor interface address bit 3 pin. |
| S31 | +ADDR(2) | in | The microprocessor interface address bit 2 pin. |
| S32 | +ADDR(1) | in | The microprocessor interface address bit 1 pin. |
| S33 | +ADDR(0) | in | The microprocessor interface address bit 0 pin. May be tied high, tied low, or not connected when not enabled. +ADDR(0) is enabled by tieing +M1BYTE high. |
| S34 | GND | | A ground pin. |
| S35 | CCOUT(5) | out | The compressed data interface control output bit 5 pin. This pin is used as the CAE signal. See Figure 4-2 on page 4-1.<br>The polarity of CCOUT(5) is controlled by CPOL(0). |
| S36 | Vdd | | A +5 Volt power supply pin. |
| E01 | GND | | A ground pin. |
| E02 | -IREQOD | out | The microprocessor interface open-drain interrupt request pin.<br>**Note:** -IREQOD is an open-drain output and requires a pull-up resistor if used. See Chapter 6 on page 6-1 for pull-up resistor selection considerations. |
| E03 | +IREQPP | out | The microprocessor interface push-pull interrupt request pin. |
| E04 | Vdd | | A +5 Volt power supply pin. |
| E05 | OCOUT(5) | out | The original data interface control output bit 5 pin. This pin is used as the OAE signal. See Figure 4-2 on page 4-1.<br>The polarity of OCOUT(5) is controlled by OPOL(0). |
| E06 | OCOUT(0) | out | The original data interface control output bit 0 pin. When OCNF(13:12) is set to B'10', this pin is used as the OACK signal. When OCNF(13:12) is set to B'00', this pin is used as the OREQ signal. When OCNF(12) is set to B'1', this pin is used as the OREADY signal. See Figure 4-2 on page 4-1.<br>The polarity of OCOUT(0) is controlled by OPOL(5). |
| E07 | OCOUT(1) | out | The original data interface control output bit 1 pin. When OCNF(13:12) is set to B'10' or when the CMND register is set to X'C400', this pin is used as the OWR signal. See Figure 4-2 on page 4-1.<br>The polarity of OCOUT(1) is controlled by OPOL(4). |

Figure 5-2 (Page 8 of 9). ALDC1-40S-M Pin Description. See Figure 5-1 on page 5-1 to identify pin locations.

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| E08 | OCOUT(2) | out | The original data interface control output bit 2 pin. When OCNF(13:12) is set to B'10' or when the CMND register is set to X'C400', this pin is used as the ORD signal. See Figure 4-2 on page 4-1.<br>The polarity of OCOUT(2) is controlled by OPOL(3). |
| E09 | OCOUT(4) | out | The original data interface control output bit 4 pin. This pin is used as the OAF signal. See Figure 4-2 on page 4-1.<br>The polarity of OCOUT(4) is controlled by OPOL(1). |
| E10 | -RESET | in | The ALDC1-40S-M hardware reset pin. |
| E11 | GND | | A ground pin. |
| E12 | | | Unused. May be tied high, tied low, or not connected. |
| E13 | -TIE | in | Must be tied low. |
| E14 | Vdd | | A +5 Volt power supply pin. |
| E15 | OCOUT(3) | out | The original data interface control output bit 3 pin. When the CMND register is set to X'C400', this pin is used as the OPCS signal. See Figure 4-2 on page 4-1.<br>The polarity of OCOUT(3) is controlled by OPOL(2). |
| E16 | +MODDP | in | The microprocessor interface parity mode selector pin. When high (and +MENABLEP high), the microprocessor interface generates and checks for odd parity. When low (and +MENABLEP high), the microprocessor interface generates and checks for even parity. |
| E17 | MMODE | in | The microprocessor interface mode selector pin. |
| E18 | GND | | A ground pin. |
| E19 | Vdd | | A +5 Volt power supply pin. |
| E20 | +OSC | in | The system clock pin. Low to high +OSC transitions are used to clock the ALDC1-40S-M. |
| E21 | GND | | A ground pin. |
| E22 | +ODATA(07) | bid | The original data interface data bit 7 pin. |
| E23 | +ODATA(06) | bid | The original data interface data bit 6 pin. |
| E24 | +ODATA(05) | bid | The original data interface data bit 5 pin. |
| E25 | Vdd | | A +5 Volt power supply pin. |
| E26 | +ODATA(04) | bid | The original data interface data bit 4 pin. |
| E27 | +ODATA(03) | bid | The original data interface data bit 3 pin. |
| E28 | GND | | A ground pin. |
| E29 | +ODATA(02) | bid | The original data interface data bit 2 pin. |
| E30 | +ODATA(01) | bid | The original data interface data bit 1 pin. |
| E31 | -TEST | in | A manufacturing test input. Must be tied high. |
| E32 | Vdd | | A +5 Volt power supply pin. |

Figure 5-2 (Page 9 of 9). ALDC1-40S-M Pin Description. See Figure 5-1 on page 5-1 to identify pin locations.

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| E33 | +ODATA(00) | bid | The original data interface data bit 0 pin. |
| E34 | GND | | A ground pin. |
| E35 | +OPARITY(0) | bid | The original data interface parity bit 0 pin. When enabled, this pin checks parity on input and generates parity on output for the associated +ODATA(00) through +ODATA(07) pins. May be tied high, tied low, or not connected when not enabled.<br>+OPARITY(0) is enabled by setting OCNF(15) to B'1'. |
| E36 | Vdd | | A +5 Volt power supply pin. |

# Chapter 6. Electrical Characteristics

## 6.1 Recommended Operating Conditions

Figure 6-1. Recommended Operating Conditions

| SYM | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{dd}$ | DC Supply Voltage | 4.75 | 5.00 | 5.25 | V |
| $V_i$ | DC Input Voltage | 0 | | $V_{dd}$ | V |
| $V_o$ | DC Output Voltage | 0 | | $V_{dd}$ | V |
| $T_a$ | Ambient Operating Temperature | 0 | | + 70 | ˚C |
| $T_c$ | Case Temperature | | | + 85 | ˚C |
| $t_r$ | Input Rise Time (See note 1.) | | | 4 | ns |
| $t_f$ | Input Fall Time (See note 1.) | | | 4 | ns |

**Note:**

1. Measured from 10% to 90% of $V_{dd}$.

## 6.2 Absolute Maximum and Minimum Ratings

Figure 6-2. Absolute Maximum and Minimum Ratings. These are the absolute maximum and minimum values that may be be applied for extended periods of time without damaging ALDC1-40S-M. Circuit functionality is *not* implied.

| SYM | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{dd}$ | DC Supply Voltage | – 0.5 | + 6.0 | V |
| $T_{st}$ | Storage Temperature | – 40 | + 125 | ˚C |
| P | Power Dissipation (See note 1.) | | 1.7 | W |

**Note:**

1. Worst case power dissipation at maximum data transfer rate (40 MB/s) and $V_{dd}$ = 5.25 V.

## 6.3 DC Characteristics

Figure 6-3 (Page 1 of 2). DC Characteristics

| SYM | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{ih}$ | Positive Logic Level Input Voltage | 2.00 | 5.00 | 5.25 | V |
| $V_{il}$ | Negative Logic Level Input Voltage | – 0.30 | 0.00 | 0.80 | V |
| $I_{ih}$ | Positive Logic Level Input Current | | | 20 | µa |

Figure 6-3 (Page 2 of 2). DC Characteristics

| SYM | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{il}$ | Negative Logic Level Input Current<br>For all inputs without internal pull-up resistors. | | | – 20 | µa |
| $I_{il}$ | Negative Logic Level Input Current<br>For all inputs with internal pull-up resistors. | | | – 355 | µa |
| $V_{oh}$ | Positive Logic Level Output Voltage<br>For all outputs except -IREQOD. | 2.40 | 5.00 | 5.25 | V |
| $V_{ol}$ | Negative Logic Level Output Voltage<br>For all outputs except -IREQOD. | 0.00 | 0.00 | 0.50 | V |
| $V_{ol}$ | Negative Logic Level Output Voltage<br>For the -IREQOD (open-drain) output. | 0.00 | 0.00 | 0.40 | V |
| $I_{oh}$ | Positive Logic Level Output Current<br>For all outputs except -IREQOD. | | | – 4 | ma |
| $I_{ol}$ | Negative Logic Level Output Current<br>For all outputs except -IREQOD. | | | 4 | ma |
| $I_{ol}$ | Negative Logic Level Output Current<br>For the -IREQOD (open-drain) output. (See note 1.) | | | 24 | ma |
| $I_Z$ | High Impedance Leakage Current | – 20 | | + 20 | µa |
| $I_{dd}$ | DC Supply Current<br>Leakage current at 0 Hz clock frequency. | | | 8 | ma |
| $C_i$ | Input Capacitance | 2.8 | | 4.0 | pf |
| $C_o$ | Output Capacitance | 2.8 | | 4.0 | pf |

**Note:**

1. The negative logic level output current for the -IREQOD output sets the lower bound on choice of pull-up resistor used. Pull-up resistor on -IREQOD output should not be less than 5.25 ÷ 0.02 . 270 Ω.

## 6.4 AC Characteristics

Figure 6-4. AC Characteristics. The differences observed in the output transition times for the -IREQOD output are due to an open-drain driver on this output.

| SYM | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{lh}$ | Negative Logic Level to Positive Logic Level Output Transition Time<br>For all outputs except -IREQOD. (See note 1.) | | | 4.7 | ns |
| $t_{hl}$ | Positive Logic Level to Negative Logic Level Output Transition Time<br>For all outputs except -IREQOD. (See note 1.) | | | 5.8 | ns |
| $t_{lh}$ | Negative Logic Level to Positive Logic Level Output Transition Time<br>For the -IREQOD (open-drain) output. (See notes 1 and 2.) | | | 38.6 | ns/kΩ |
| $t_{hl}$ | Positive Logic Level to Negative Logic Level Output Transition Time<br>For the -IREQOD (open-drain) output. (See note 1.) | | | 6.3 | ns |

**Notes:**

1. Worst case at $T_a$ = 70°C, $V_{dd}$ = 4.75 V, and load capacitance ($C_L$) = 50pf.
2. Transition time is dependent on value of pull-up resistor used. For example, using a 2000 Ω resistor as pull-up on the -IREQOD output gives maximum $t_{lh}$ = 2 × 38.6 = 77.2 ns.

## 6.5 Idd vs. Clock Frequency

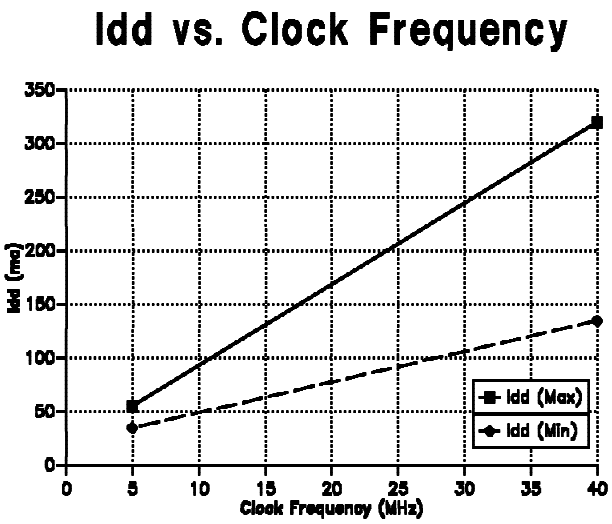



Figure 6-5. Idd vs. Clock Frequency. Maximum $I_{dd}$ measured at maximum input and output data rates and $V_{dd}$ = 5.25 V at given clock frequency. Minimum $I_{dd}$ measured at standby state (no data input or output) and $V_{dd}$ = 4.75 V at given clock frequency. The clock frequency is measured at the +OSC input.

**Note:** This graph contains preliminary power measurements.

# Chapter 7. Physical Dimensions

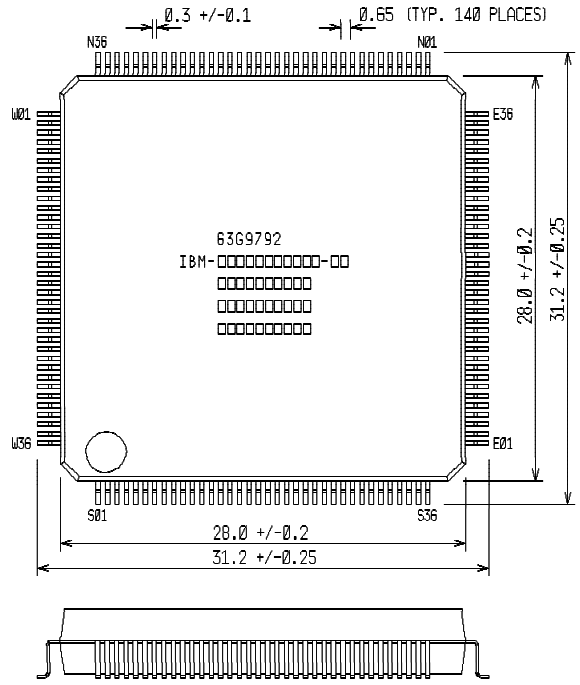



Figure 7-1. ALDC1-40S-M Top and Side Views. All length and tolerance dimensions in millimeters. The orientation mark is shown in the lower left-hand corner of the top view.

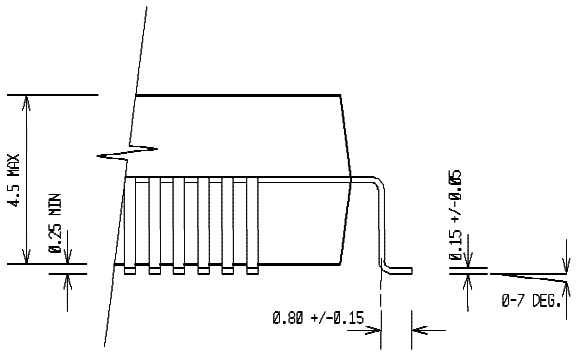



Figure 7-2. ALDC1-40S-M Pin Close-up View. All length and tolerance dimensions in millimeters.

# Appendix A. Notation

## A.1 Bit Significance

Bit numbering and bit significance notation follow the industry standard usage convention. That is, lower bit numbers have lower bit significance and higher bit numbers have higher bit significance.

A range of bits is noted by writing the most significant bit and the least significant bit of the range separated by a colon (:). For example, bits seven through zero on a bus are written 7:0. Or, bits five through two of a register named SAMP are written SAMP(5:2).

## A.2 Binary Numbers

Binary numbers are denoted by B'##' in this document, where ## is the binary number being represented. For example, B'1010' is the binary representation for decimal ten. B'11000101' is equivalent to 197.

## A.3 Hexadecimal Numbers

Hexadecimal numbers are denoted by X'##' in this document, where ## is the hexadecimal number to be represented. For example, X'A' is the hexadecimal representation for decimal ten. X'2CBE' is equivalent to 11454.

## A.4 Pin and Signal Names

Pin and signal names are written in this document using a special font. The pin name -RESET (the ALDC1-40S-M hardware reset pin) demonstrates this font. In addition, if a pin or signal name begins with a + then it is always positive active (as in +ODATA(04)). If a pin or signal name begins with a - then it is always negative active (as in -RESET). If a pin or signal name does not begin with a + or -, then its active state is undefined or configurable.

## A.5 Byte Order

In this document, lower order bytes are stored at lower addresses in memory. When writing to or reading from one of the ALDC1-40S-M interfaces (configured to be two bytes wide), the second (higher order) byte is at a consecutively higher address than the first byte. For example, if X'1234' was to be written into the CMND register, then +MDATA(15) through +MDATA(08) would be set to X'12' and +MDATA(07) through +MDATA(00) would be set to X'34'. In memory, the X'12' is one address above the X'34'.

The same holds true for the original data interface and compressed data interface. Suppose a long string of bytes was to be transferred into the original data interface during a compression operation. For this example, let the first byte be X'01', the second byte be X'02', the third byte be X'03', etc. Each higher order byte is stored at a consecutively higher address. Then on the first transfer into the original data interface, +ODATA(15) through +ODATA(08) would be set to X'02' and +ODATA(07) through +ODATA(00) would be set to X'01'.

If an interface is configured to be one byte wide, then the order of a byte is completely determined by the order in which it is sent to or received from the interface.

## A.6 Device and Controller

Asynchronous handshaking protocols distinguish between devices (sometimes called *slaves*) and controllers (sometimes called *masters*). Within this document, references made to devices and controllers use the following convention:

**Device** A device is any circuitry which generates a request signal and receives an acknowledge signal.

**Controller** A controller is any circuitry which receives a request signal and generates an acknowledge signal.

**Note:** The concept of device and controller are **not** used when discussing synchronous communication.

# Appendix B. IBM ALDC Compression Products

Figure B-1 (Page 1 of 2). IBM ALDC Compression Products

| PRODUCT NAME (OEM CATALOG NUMBER) | PACKAGE | DESCRIPTION | AVAIL-ABILITY |
|---|---|---|---|
| ALDC1-5S-L (IBM22-ALDC1005S-00) | 100 lead low quad flat package. 14 mm x 14 mm x 1.4 mm body size with 0.5 mm lead spacing. | Maximum 5 MB/s data rate for compression and decompression. The microprocessor interface, original data interface, and compressed data interface all use one-byte wide data buses. | Now |
| ALDC1-5S-P (IBM22-ALDC1005S-01) | 100 lead plastic flat package. 14 mm x 20 mm x 2.7 mm body size with 0.65 mm lead spacing. | Maximum 5 MB/s data rate for compression and decompression. The microprocessor interface, original data interface, and compressed data interface all use one-byte wide data buses. | Now |
| ALDC1-20S-H (IBM22-ALDC1020S-00) | 144 lead plastic flat package with heat spreader. 28 mm x 28 mm x 3.8 mm body size with 0.65 mm lead spacing. | Maximum 20 MB/s data rate for compression and decompression. The microprocessor interface uses a one- or two-byte wide data bus which operates in two handshaking modes. The original data interface and compressed data interface use one- or two-byte wide data buses which operate in four handshaking modes. | Now |
| ALDC1-40S-M (IBM22-ALDC1040S-00) | 144 lead plastic flat package with molded heat sink. 28 mm x 28 mm x 3.8 mm body size with 0.65 mm lead spacing. | Maximum 40 MB/s data rate for compression and decompression. The microprocessor interface uses a one- or two-byte wide data bus which operates in two handshaking modes. The original data interface and compressed data interface use one- or two-byte wide data buses which operate in four asynchronous and one synchronous handshaking modes. | Now |

Figure B-1 (Page 2 of 2). IBM ALDC Compression Products

| PRODUCT NAME (OEM CATALOG NUMBER) | PACKAGE | DESCRIPTION | AVAIL-ABILITY |
|---|---|---|---|
| ALDC1-20S-HA (IBM22-ALDC1020S-01) | 100 lead plastic flat package with heat spreader. 14 mm x 20 mm x 2.7 mm body size with 0.65 mm lead spacing. | Maximum 20 MB/s data rate for compression and decompression. The microprocessor interface uses a one-byte wide data bus which operates in two handshaking modes. The original data interface and compressed data interface use one- or two-byte wide data buses which operate in four handshaking modes. | Now |

# How to Contact IBM Microelectronics Division

| REGION | ADDRESS | TELEPHONE NUMBER |
|---|---|---|
| United States and Canada: | IBM Microelectronics Division<br>1580 Route 52, Building 504<br>Hopewell Junction, NY 12533-6531 | (800) IBM-0181<br>ext: 742 |
| Europe: | IBM<br>La Pompignane BP 1021<br>34006 Montpellier<br>France | (33) 6713-5757 (Francais)<br>(33) 6713-5756 (Italiano)<br>(33) 6713-5750 (FAX)*<br>*From Paris add 16 |
| | IBM Informations Systeme GmbH<br>Laatzener Strasse 1<br>30539 Hannover<br>Germany | (49) 511-516-3444 (English)<br>(49) 511-516-3555 (Deutsch)<br>(49) 511-516-3888 (FAX) |
| Japan: | IBM<br>800 Ichimiyake<br>Yasu-cho, Yasu-gun<br>Shiga-ken, Japan 520-23 | (81) 775-87-4745<br>(81) 775-87-4735 (FAX) |

Printed in U.S.A.