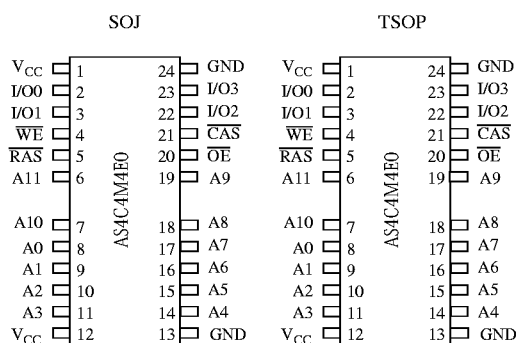


5V/3V 4M×4 CMOS DRAM (EDO)

Features

- Organization: 4,194,304 words × 4 bits
- High speed
 - 45/50/60 ns $\overline{\text{RAS}}$ access time
 - 23/25/30 ns column address access time
 - 10/12/15 ns $\overline{\text{CAS}}$ access time
- Low power consumption
 - Active: 908 mW max
 - Standby: 5.5 mW max, CMOS I/O
- Extended data out
- 4096 refresh cycles, 64 ms refresh interval
- $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
- TTL-compatible, three-state I/O
- JEDEC standard package
 - 300 mil, 24/26-pin SOJ
 - 300 mil, 24/26-pin TSOP
- 5V power supply (AS4C4M4E0)
- 3V power supply (AS4LC4M4E0)
- Latch-up current ≥ 200 mA
- ESD protection ≥ 2000 mV
- For 2048 refresh device, contact Alliance.

Pin arrangement



Pin designation

Pin(s)	Description
A0 to A11	Address inputs
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable
I/O0 to I/O3	Input/output
$\overline{\text{OE}}$	Output enable
V_{CC}	Power
GND	Ground



Selection guide

	Symbol	AS4C4M4E0-45 AS4LC4M4E0-45	AS4C4M4E0-50 AS4LC4M4E0-50	AS4C4M4E0-60 AS4LC4M4E0-60	Unit
Maximum $\overline{\text{RAS}}$ access time	t_{RAC}	45	50	60	ns
Maximum column address access time	t_{CAA}	23	25	30	ns
Maximum $\overline{\text{CAS}}$ access time	t_{CAC}	10	12	15	ns
Maximum output enable ($\overline{\text{OE}}$) access time	t_{OEA}	10	13	15	ns
Minimum read or write cycle time	t_{RC}	75	85	100	ns
Minimum fast page mode cycle time	t_{PC}	20	25	30	ns
Maximum operating current	I_{CC1}	145	135	120	mA
Maximum CMOS standby current	I_{CC5}	1.0	1.0	1.0	mA



Functional description

The AS4C4M4E0 and AS4LC4M4E0 are high performance 16-megabit CMOS Dynamic Random Access Memories (DRAM) organized as 4,194,304 words \times 4 bits. The devices are fabricated using advanced CMOS technology and innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels. The Alliance 16Mb DRAM family is optimized for use as main memory in PC, workstation, router and switch applications.

These products feature a high speed page mode operation where read and write operations within a single row (or page) can be executed at very high speed by toggling column addresses within that row. Row and column addresses are alternately latched into input buffers using the falling edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ inputs respectively. Also, $\overline{\text{RAS}}$ is used to make the column address latch transparent, enabling application of column addresses prior to $\overline{\text{CAS}}$ assertion.

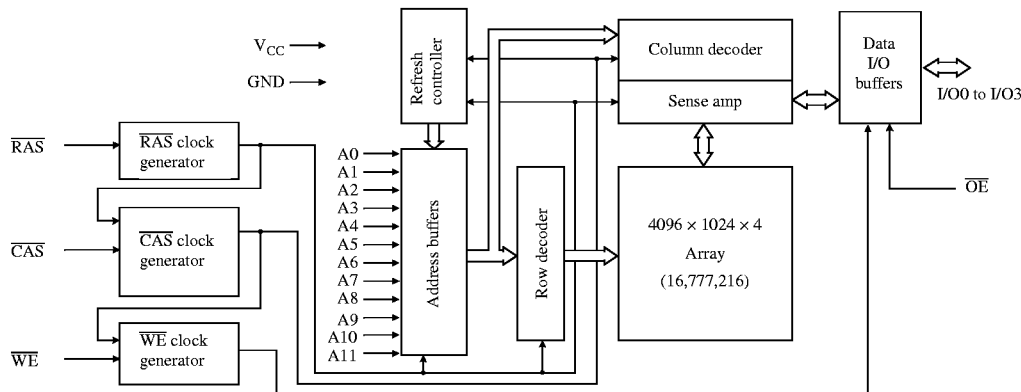
Extended data out (EDO) read mode enables 60MHz operation using 60ns devices. In contrast to 'fast page mode' devices, data remains active on outputs after $\overline{\text{CAS}}$ is de-asserted high, giving system logic more time to latch the data. Use $\overline{\text{OE}}$ and $\overline{\text{WE}}$ to control output impedance and prevent bus contention during read-modify-write and shared bus applications. Outputs also go to high impedance at the last occurrence of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ going high.

Refresh on the 4096 address combinations of A0 to A11 must be performed every 64 ms using:

- $\overline{\text{RAS}}$ -only refresh: $\overline{\text{RAS}}$ is asserted while $\overline{\text{CAS}}$ is held high. Each of the 4096 rows must be strobed. Outputs remain high impedance.
- Hidden refresh: $\overline{\text{CAS}}$ is held low while $\overline{\text{RAS}}$ is toggled. Refresh address is generated internally. Outputs remain low impedance with previous valid data.
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh (CBR): At least one $\overline{\text{CAS}}$ is asserted prior to $\overline{\text{RAS}}$. Refresh address is generated internally. Outputs are high-impedance ($\overline{\text{OE}}$ and $\overline{\text{WE}}$ are don't care).
- Normal read or write cycles refresh the row being accessed.

The AS4C4M4E0 and AS4LC4M4E0 are available in the standard 24/26-pin plastic SOJ and 24/26-pin plastic TSOP packages. The AS4C4M4E0 operates with a single power supply of $5\text{V} \pm 0.5\text{V}$ and the AS4LC4M4E0 operates at $3.3\text{V} \pm 0.3\text{V}$. Both provide TTL compatible inputs and outputs.

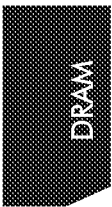
Logic block diagram



Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage	AS4C4M4E0	V_{CC}	4.5	5.0	5.5	V
	AS4LC4M4E0	V_{CC}	3.0	3.3	3.6	V
		GND	0.0	0.0	0.0	V
Input voltage	AS4C4M4E0	V_{IH}	2.4	-	V_{CC}	V
	AS4LC4M4E0	V_{IH}	2.0	-	V_{CC}	V
		V_{IL}	-0.5^{\dagger}	-	0.8	V
Ambient operating temperature		T_A	0		70	$^{\circ}\text{C}$

$^{\dagger}V_{IL}$ min -3.0V for pulse widths less than 5 ns. Recommended operating conditions apply throughout this document unless otherwise specified.





Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage	V_{in}	-1.0	+7.0	V
Input voltage (DQs)	V_{DQ}	-1.0	$V_{CC} + 0.5$	V
Power supply voltage	V_{CC}	-1.0	+7.0	V
Storage temperature (plastic)	T_{STG}	-55	+150	°C
Soldering temperature × time	T_{SOLDER}	-	260×10	°C × sec
Power dissipation	P_D	-	1	W
Short circuit output current	I_{out}	-	50	mA

DC electrical characteristics

Parameter	Symbol	Test conditions	-45		-50		-60		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Input leakage current	I_{IL}	$0V \leq V_{in} \leq +5.5V$, Pins not under test = 0V	-5	+5	-5	+5	-5	+5	µA	
Output leakage current	I_{OL}	D_{OUT} disabled, $0V \leq V_{out} \leq +5.5V$	-5	+5	-5	+5	-5	+5	µA	
Operating power supply current	I_{CC1}	\overline{RAS} , UCAS, LCAS, Address cycling; $t_{RC} = \text{min}$	-	145	-	135	-	120	mA	1,2
TTL standby power supply current	I_{CC2}	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} \geq V_{IH}$	-	2.0	-	2.0	-	2.0	mA	
Average power supply current, \overline{RAS} refresh mode or CBR	I_{CC3}	\overline{RAS} cycling, $\overline{UCAS} = \overline{LCAS} \geq V_{IH}$, $t_{RC} = \text{min}$ of \overline{RAS} low after \overline{XCAS} low.	-	130	-	120	-	110	mA	1
EDO page mode average power supply current	I_{CC4}	$\overline{RAS} = V_{IL}$, UCAS or LCAS, address cycling: $t_{HPC} = \text{min}$	-	140	-	130	-	120	mA	1, 2
CMOS standby power supply current	I_{CC5}	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{CC} - 0.2V$	-	1.0	-	1.0	-	1.0	mA	
Output voltage	V_{OH}	$I_{OUT} = -5.0 \text{ mA}$	2.4	-	2.4	-	2.4	-	V	
	V_{OL}	$I_{OUT} = 4.2 \text{ mA}$	-	0.4	-	0.4	-	0.4	V	
CAS before \overline{RAS} refresh current	I_{CC6}	\overline{RAS} , UCAS or LCAS cycling, $t_{RC} = \text{min}$	-	130	-	120	-	110	mA	

DPAK



AC parameters common to all waveforms

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t _{RC}	Random read or write cycle time	75	–	80	–	100	–	ns	
t _{RP}	$\overline{\text{RAS}}$ precharge time	30	–	30	–	40	–	ns	
t _{RAS}	$\overline{\text{RAS}}$ pulse width	45	10K	50	10K	60	10K	ns	
t _{CAS}	$\overline{\text{CAS}}$ pulse width	8	10K	8	10K	10	10K	ns	
t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	15	35	15	35	15	43	ns	6
t _{RAD}	$\overline{\text{RAS}}$ to column address delay time	12	25	12	25	12	30	ns	7
t _{RSH}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ hold time	10	–	10	–	10	–	ns	
t _{CSH}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ hold time	40	–	40	–	50	–	ns	
t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	5	–	5	–	5	–	ns	
t _{ASR}	Row address setup time	0	–	0	–	0	–	ns	
t _{RAH}	Row address hold time	8	–	8	–	10	–	ns	
t _T	Transition time (rise and fall)	1	50	1	50	1	50	ns	4,5
t _{REF}	Refresh period	–	64	–	64	–	64	ms	3
t _{CP}	$\overline{\text{CAS}}$ precharge time	8	–	8	–	10	–	ns	
t _{RAL}	Column address to $\overline{\text{RAS}}$ lead time	25	–	25	–	30	–	ns	
t _{ASC}	Column address setup time	0	–	0	–	0	–	ns	
t _{CAH}	Column address hold time	8	–	8	–	10	–	ns	

Read cycle

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t _{RAC}	Access time from $\overline{\text{RAS}}$	–	45	–	50	–	60	ns	6
t _{CAC}	Access time from $\overline{\text{CAS}}$	–	10	–	12	–	15	ns	6,13
t _{AA}	Access time from address	–	23	–	25	–	30	ns	7,13
t _{RCS}	Read command setup time	0	–	0	–	0	–	ns	
t _{RCH}	Read command hold time to $\overline{\text{CAS}}$	0	–	0	–	0	–	ns	9
t _{RRH}	Read command hold time to $\overline{\text{RAS}}$	0	–	0	–	0	–	ns	9



Write cycle

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t _{WCS}	Write command setup time	0	–	0	–	0	–	ns	11
t _{WCH}	Write command hold time	10	–	10	–	10	–	ns	11
t _{WP}	Write command pulse width	10	–	10	–	10	–	ns	
t _{RWL}	Write command to $\overline{\text{RAS}}$ lead time	10	–	10	–	10	–	ns	
t _{CWL}	Write command to $\overline{\text{CAS}}$ lead time	8	–	8	–	10	–	ns	
t _{DS}	Data-in setup time	0	–	0	–	0	–	ns	12
t _{DH}	Data-in hold time	8	–	8	–	10	–	ns	12

Read-modify-write cycle

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t _{RWC}	Read-write cycle time	105	–	113	–	135	–	ns	
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	65	–	67	–	77	–	ns	11
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	30	–	32	–	35	–	ns	11
t _{AWD}	Column address to $\overline{\text{WE}}$ delay time	40	–	42	–	47	–	ns	11

Refresh cycle

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t _{CSR}	$\overline{\text{CAS}}$ setup time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$)	5	–	5	–	5	–	ns	3
t _{CHR}	$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$)	8	–	8	–	10	–	ns	3
t _{RPC}	$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	0	–	0	–	0	–	ns	
t _{CPT}	$\overline{\text{CAS}}$ precharge time (CBR counter test)	10	–	10		10	–	ns	

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Hyper page mode cycle

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t _{CPWD}	CAS precharge to WE delay time	45	–	45	–	52	–	ns	
t _{CPA}	Access time from CAS precharge	–	28	–	28	–	35	ns	13
t _{RASP}	RAS pulse width	45	100K	50	100K	60	100K	ns	
t _{DOH}	Previous data hold time from CAS	5	–	5	–	5	–	ns	
t _{REZ}	Output buffer turn off delay from RAS	0	13	0	13	0	15	ns	
t _{WEZ}	Output buffer turn off delay from WE	0	13	0	13	0	15	ns	
t _{OEZ}	Output buffer turn off delay from OE	0	13	0	13	0	15	ns	
t _{HPC}	Hyper page mode cycle time	20	–	20	–	25	–	ns	
t _{HPRWC}	Hyper page mode RMW cycle	47	–	47	–	56	–	ns	
t _{RHCP}	RAS hold time from CAS	30	–	30	–	35	–	ns	

Output enable

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t _{CLZ}	CAS to output in Low Z	0	–	0	–	0	–	ns	8
t _{ROH}	RAS hold time referenced to OE	8	–	8	–	10	–	ns	
t _{OEA}	OE access time	–	10	–	13	–	15	ns	
t _{OED}	OE to data delay	13	–	13	–	15	–	ns	
t _{OEZ}	Output buffer turnoff delay from OE	0	13	0	13	0	15	ns	8
t _{OEH}	OE command hold time	10	–	10	–	10	–	ns	
t _{OLZ}	OE to output in Low Z	0	–	0	–	0	–	ns	
t _{OFF}	Output buffer turn-off time	0	13	0	13	0	15	ns	8,10

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Notes

- 1 I_{CC1} , I_{CC3} , I_{CC4} , and I_{CC6} are dependent on frequency.
- 2 I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
- 3 An initial pause of 200 μ s is required after power-up followed by any 8 \overline{RAS} cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 \overline{CAS} -before- \overline{RAS} initialization cycles instead of 8 \overline{RAS} cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8 ms).
- 4 AC Characteristics assume $t_f = 2$ ns. All AC parameters are measured with a load equivalent to two TTL loads and 100 pF, $V_{IL}(\text{min}) \geq \text{GND}$ and $V_{IH}(\text{max}) \leq V_{CC}$.
- 5 $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
- 6 Operation within the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
- 7 Operation within the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
- 8 Assumes three state test load (5 pF and a 380 Ω Thevenin equivalent).
- 9 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 10 $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels. t_{OFF} is referenced from rising edge of \overline{RAS} or \overline{CAS} , whichever occurs last.
- 11 t_{WCS} , t_{WCH} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If $t_{WS} \geq t_{WS}(\text{min})$ and $t_{WH} \geq t_{WH}(\text{min})$, the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
- 12 These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WE} leading edge in read-write cycles.
- 13 Access time is determined by the longest of t_{CAA} or t_{CAC} or t_{CPA}
- 14 $t_{ASC} \geq t_{CP}$ to achieve $t_{PC}(\text{min})$ and $t_{CPA}(\text{max})$ values.
- 15 These parameters are sampled and not 100% tested.
- 16 These characteristics apply to AS4C4M4E0 5V devices.

AC test conditions

- Access times are measured with output reference levels of $V_{OH} = 2.4\text{V}$ and $V_{OL} = 0.4\text{V}$, $V_{IH} = 2.4\text{V}$ and $V_{IL} = 0.8\text{V}$
- Input rise and fall times: 2 ns

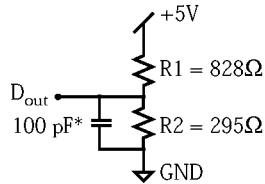


Figure A: Equivalent output load (AS4C4M4E0)

*including scope and jig capacitance

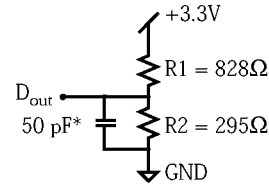


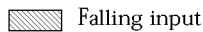
Figure B: Equivalent output load (AS4LC4M4E0)

*including scope and jig capacitance

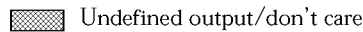
Key to switching waveforms



Rising input



Falling input

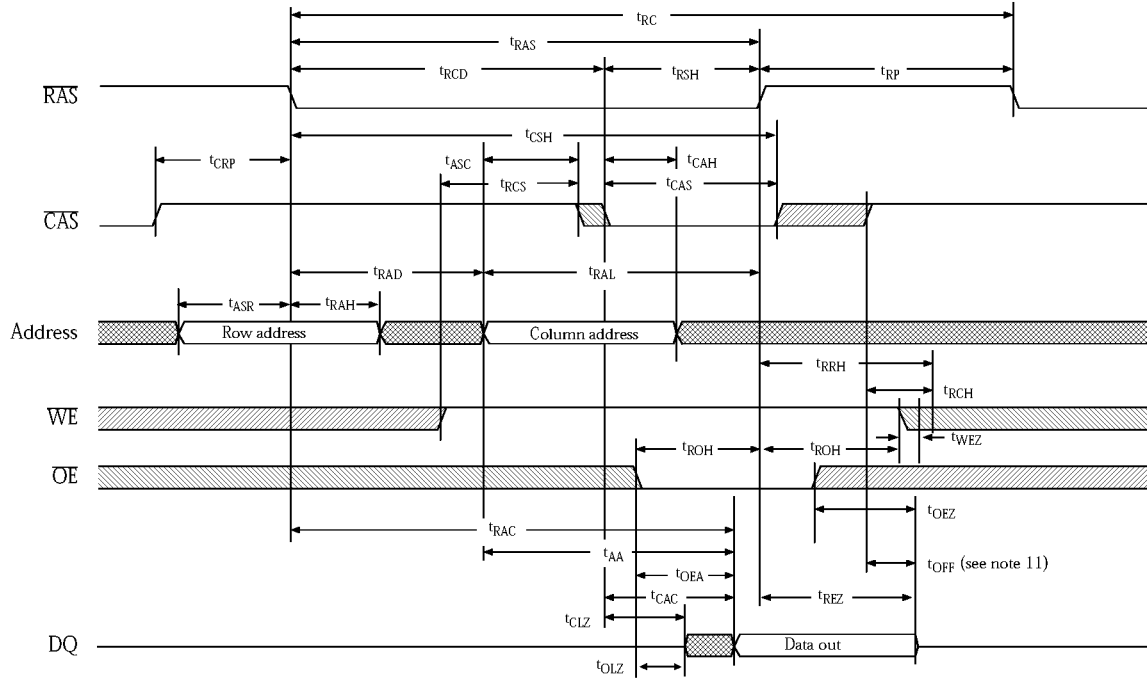


Undefined output/don't care

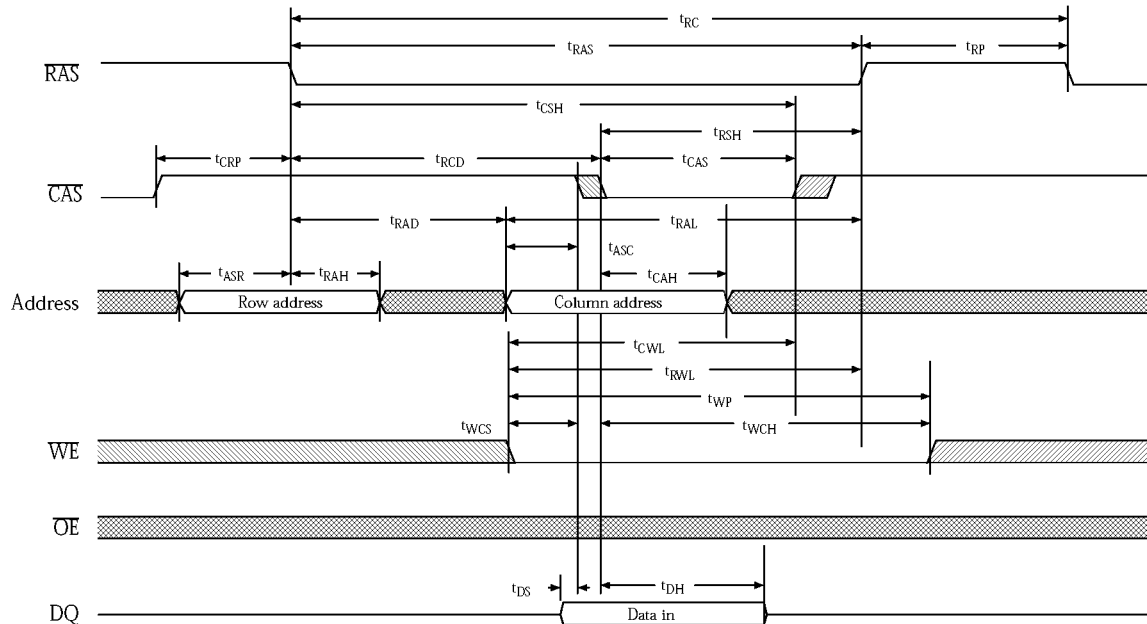




Read waveform



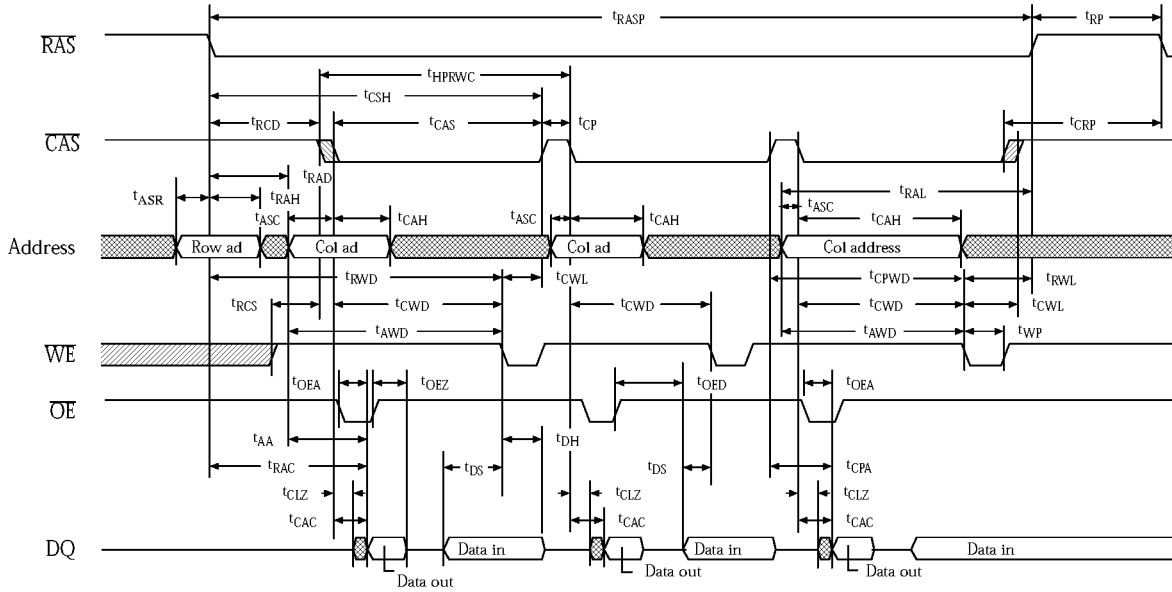
Early write waveform



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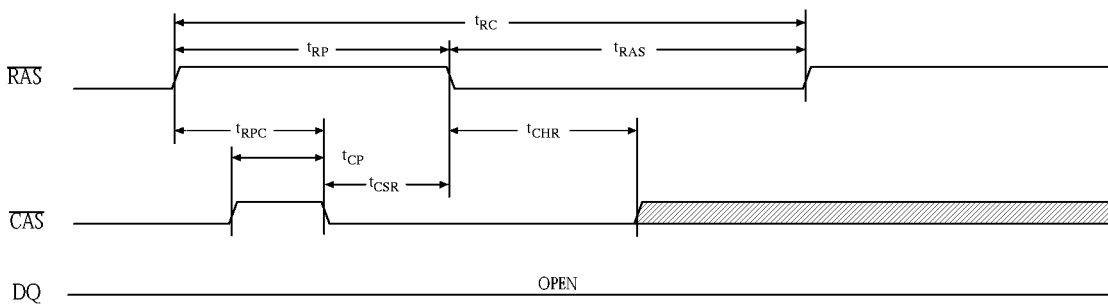


EDO page mode read-modify-write waveform



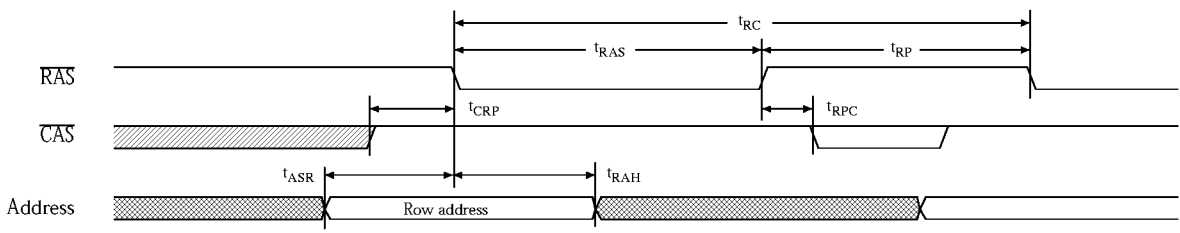
CAS before RAS refresh waveform

$\overline{WE} = A = V_{IH}$ or V_{IL}



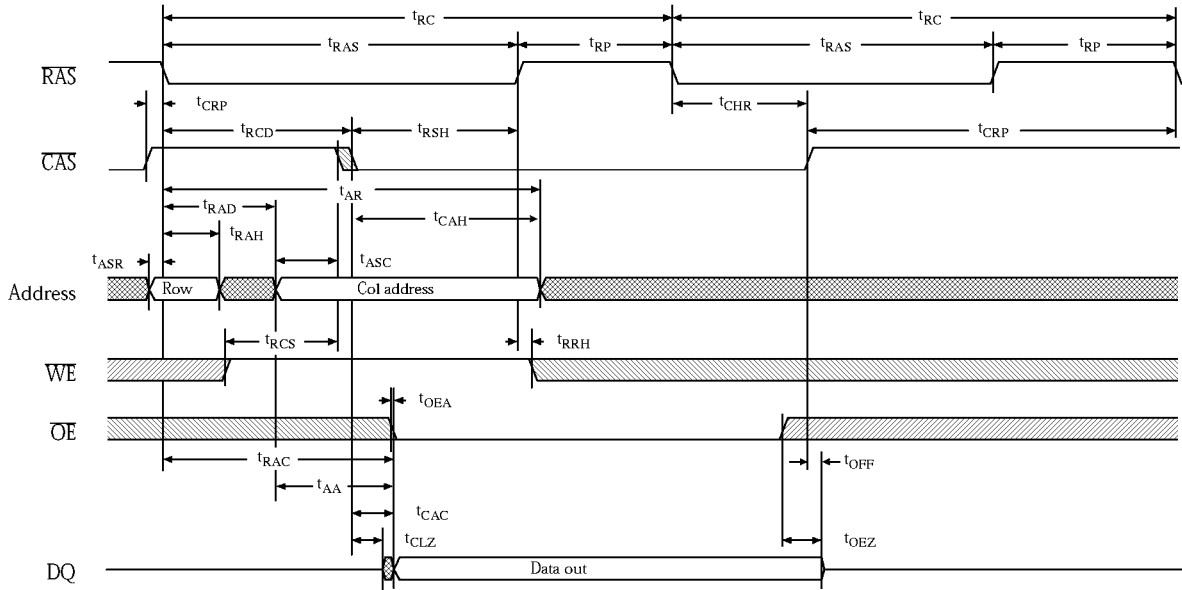
RAS only refresh waveform

$\overline{WE} = \overline{OE} = V_{IH}$ or V_{IL}

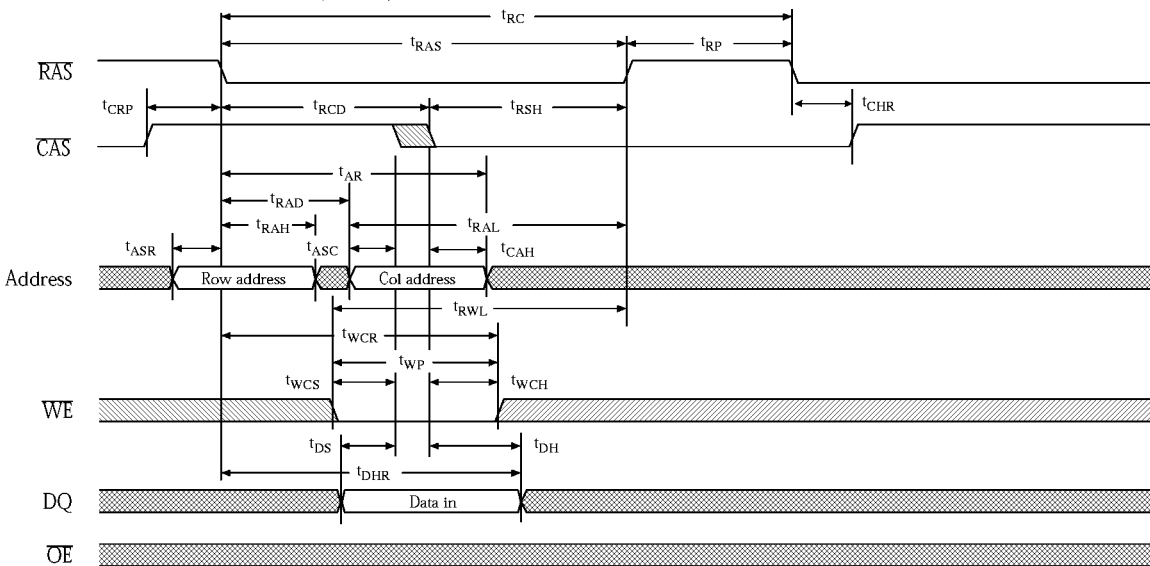




Hidden refresh waveform (read)



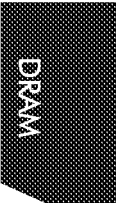
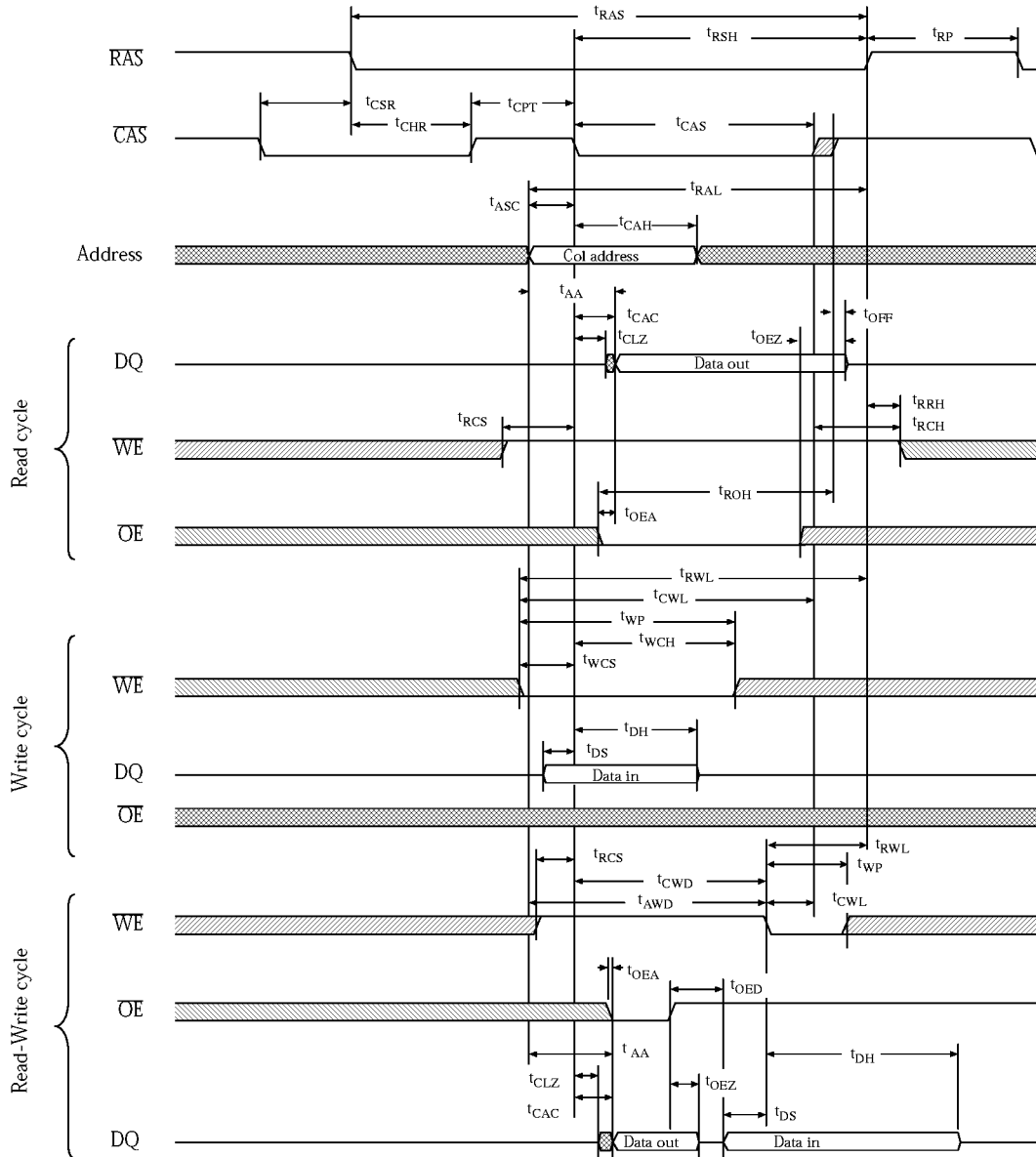
Hidden refresh waveform (write)



DRAM

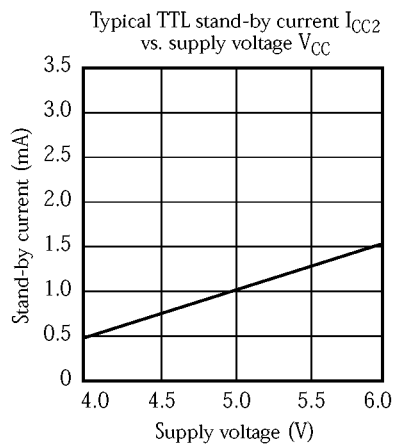
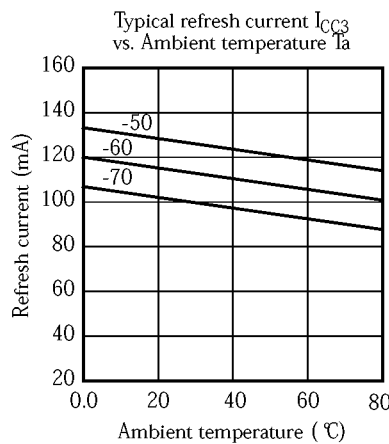
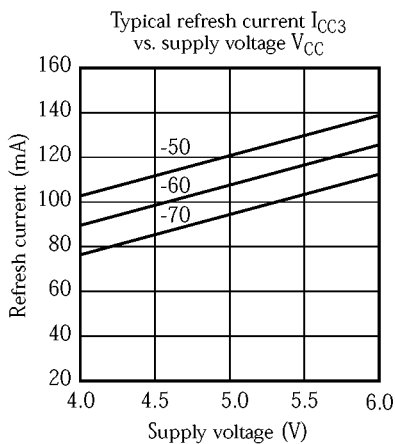
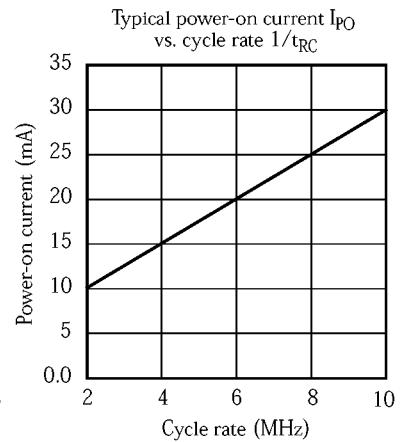
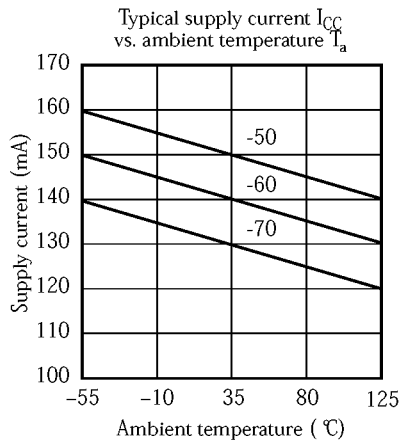
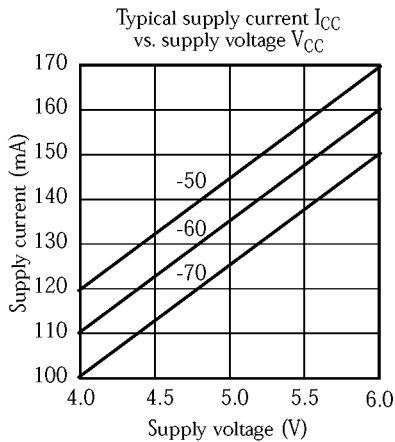
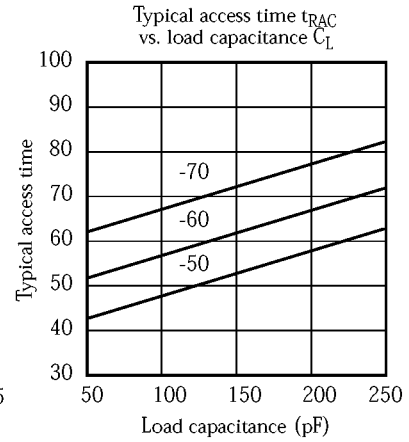
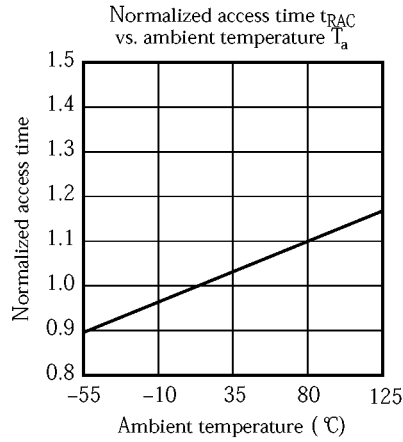
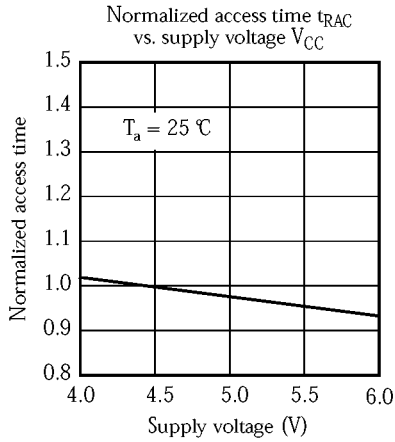


CAS before RAS refresh counter test waveform

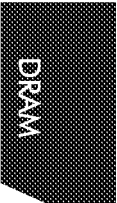
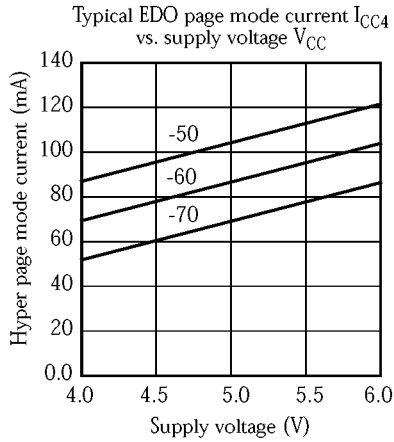
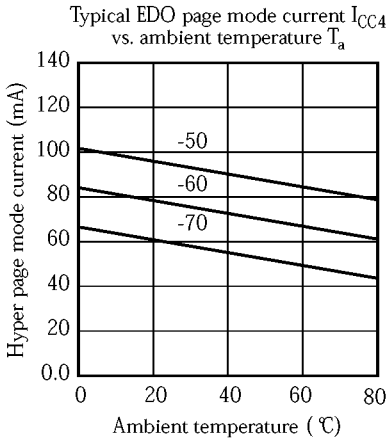
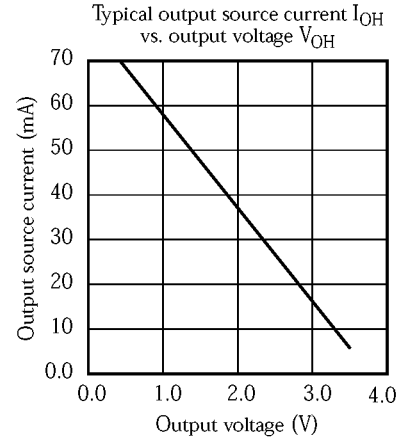
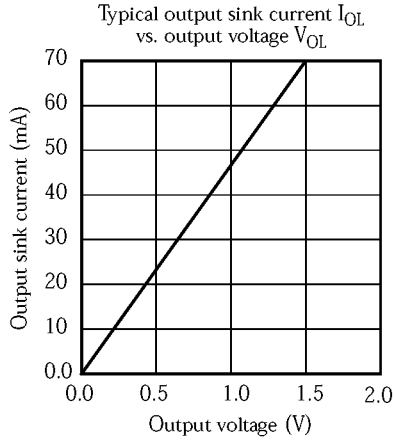
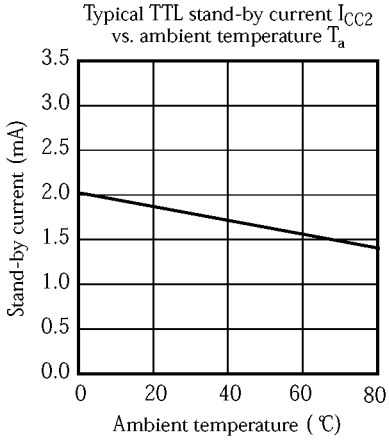




Typical DC and AC characteristics



DRAM





Capacitance ¹⁵

$f = 1 \text{ MHz}, T_o = \text{Room temperature}$

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN1}	A0 to A9	$V_{in} = 0V$	5	pF
	C_{IN2}	RAS, UCAS, LCAS, WE, OE	$V_{in} = 0V$	7	pF
DQ capacitance	C_{DQ}	DQ0 to DQ15	$V_{in} = V_{out} = 0V$	7	pF

AS4C4M4E0 ordering information

Package \ RAS access time		45 ns	50 ns	60 ns
Plastic SOJ, 300 mil, 24/26-pin	5V	AS4C4M4E0-45JC	AS4C4M4E0-50JC	AS4C4M4E0-60JC
Plastic TSOP, 300 mil, 24/26-pin	3.3V	AS4C4M4E0-45TC	AS4C4M4E0-50TC	AS4LC4M4E0-60TC

AS4LC4M4E0 ordering information

Package \ RAS access time		45 ns	50 ns	60 ns
Plastic SOJ, 300 mil, 24/26-pin	5V	AS4LC4M4E0-45JC	AS4LC4M4E0-50JC	AS4LC4M4E0-60JC
Plastic TSOP, 300 mil, 24/26-pin	3.3V	AS4LC4M4E0-45TC	AS4LC4M4E0-50TC	AS4LC4M4E0-60TC

AS4C4M4E0 part numbering system

AS4	C	1M16E0	-XX	X	C
DRAM prefix	C = 5V CMOS LC = 3.3V CMOS	Device number	RAS access time	Package: J = SOJ 300 mil, 24/26 T = TSOP 300 mil, 24/26	Commercial temperature range, 0 °C to 70 °C

