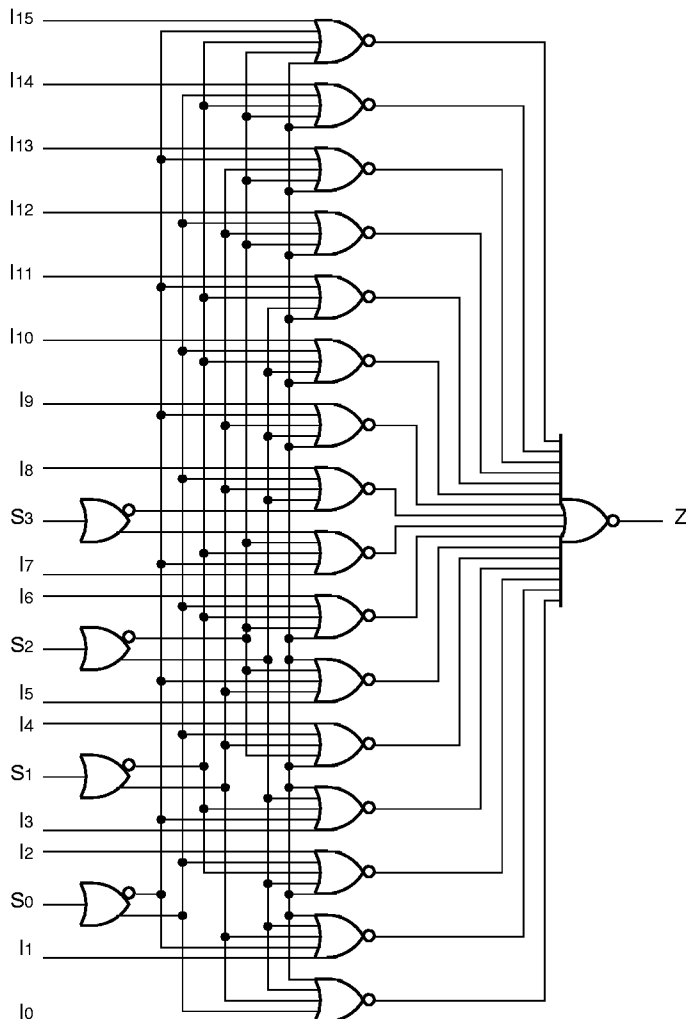


FEATURES

- Max. propagation delay of 1300ps
- IEE min. of -63mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 70% faster than National or Signetics
- 40% lower power than National or Signetics
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERDIP, 24-pin CERPAC and 28-pin PLCC packages

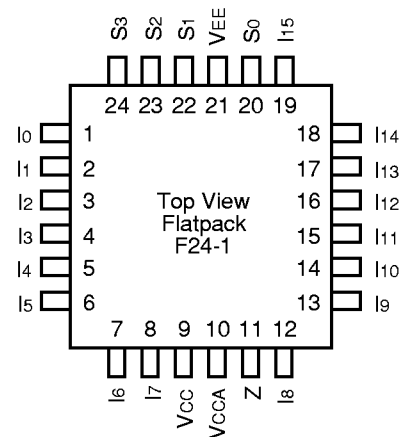
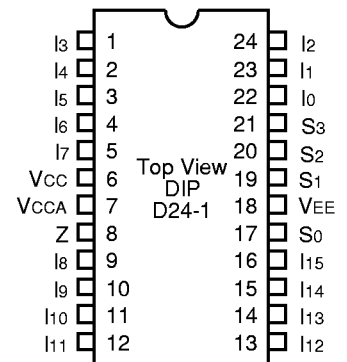
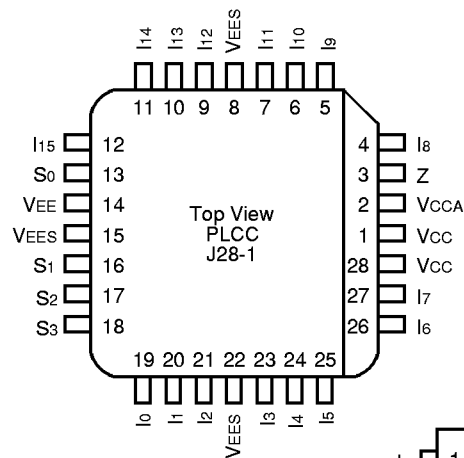
BLOCK DIAGRAM



DESCRIPTION

The SY100S364 is a 16-input multiplexer designed for use in high-performance ECL systems. The four Data Select inputs (S0, S1, S2, S3) determine the bit from the 16 inputs (I_n) that will be passed on to the output as shown in the Truth Table. The output data polarity is the same as the input. The inputs on the device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS



PIN NAMES

Pin	Function
I ₀ – I ₁₅	Data Inputs
S ₀ – S ₃	Select Inputs
Z	Data Output
VEES	VEE Substrate
VCCA	V _{CC0} for ECL Outputs

TRUTH TABLE⁽¹⁾

Select Inputs				Output
S ₀	S ₁	S ₂	S ₃	Z
L	L	L	L	I ₀
H	L	L	L	I ₁
L	H	L	L	I ₂
H	H	L	L	I ₃
L	L	H	L	I ₄
H	L	H	L	I ₅
L	H	H	L	I ₆
H	H	H	L	I ₇
L	L	L	H	I ₈
H	L	L	H	I ₉
L	H	L	H	I ₁₀
H	H	L	H	I ₁₁
L	L	H	H	I ₁₂
H	L	H	H	I ₁₃
L	H	H	H	I ₁₄
H	H	H	H	I ₁₅

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level

DC ELECTRICAL CHARACTERISTICS

VEE = –4.2V to –5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current I _n S ₀ , S ₁ S ₂ , S ₃	—	—	200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	–63	–45	–30	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS
CERDIP

VEE = –4.2V to –5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay I ₀ – I ₁₅ to Output	400	1500	400	1500	400	1500	ps	
t _{PLH} t _{PHL}	Propagation Delay S ₀ , S ₁ to Output	400	1900	400	1900	400	1900	ps	
t _{PLH} t _{PHL}	Propagation Delay S ₂ , S ₃ to Output	400	1700	400	1700	400	1700	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

AC ELECTRICAL CHARACTERISTICS (Continued)

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

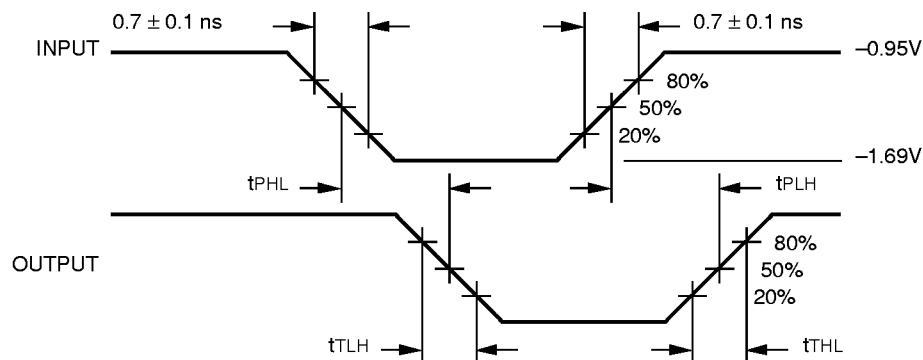
Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay I ₀ – I ₁₅ to Output	400	1400	400	1400	400	1400	ps	
t _{PLH} t _{PHL}	Propagation Delay S ₀ , S ₁ to Output	400	1900	400	1900	400	1900	ps	
t _{PLH} t _{PHL}	Propagation Delay S ₂ , S ₃ to Output	400	1700	400	1700	400	1700	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay I ₀ – I ₁₅ to Output	400	1300	400	1300	400	1300	ps	
t _{PLH} t _{PHL}	Propagation Delay S ₀ , S ₁ to Output	400	1800	400	1800	400	1800	ps	
t _{PLH} t _{PHL}	Propagation Delay S ₂ , S ₃ to Output	400	1600	400	1600	400	1600	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



Propagation Delay and Transition Times

NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S364DC	D24-1	Commercial
SY100S364FC	F24-1	Commercial
SY100S364JC	J28-1	Commercial
SY100S364JCTR	J28-1	Commercial

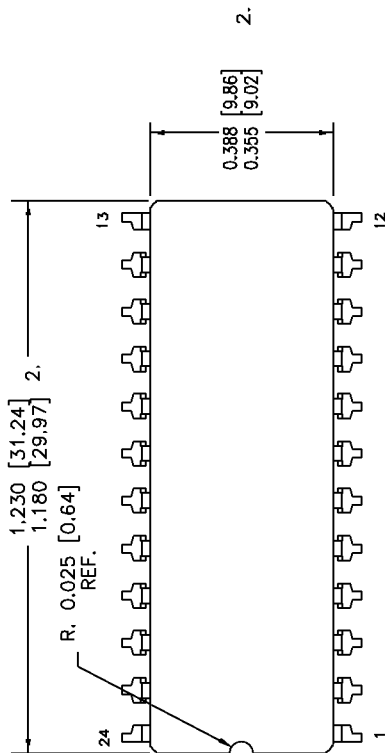
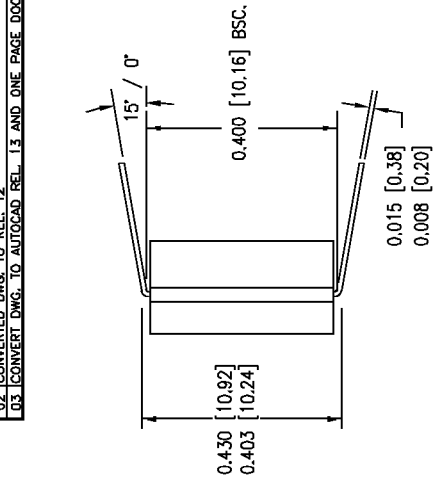
24 LEAD CERDIP (D24-1)

FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT DWG. TO DESIGNER VERSION 4.0 FORMAT.	12/30/93
02	CONVERTED DWG. TO REL. 12	03/15/96
03	CONVERT DWG. TO AUTOCAD REL. 1.3 AND ONE PAGE DOCUMENT.	02/18/98



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
- THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.



3250 SCOTT BOULEVARD
SANTA CLARA CA 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERDIP (400" WIDE) PACKAGE OUTLINE
ORIGINATOR: FERMIN G. LURRITA	02/23/98	QUALITY: MARSHALL WILDER		A	
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					SCALE N/A
					REVISION 03

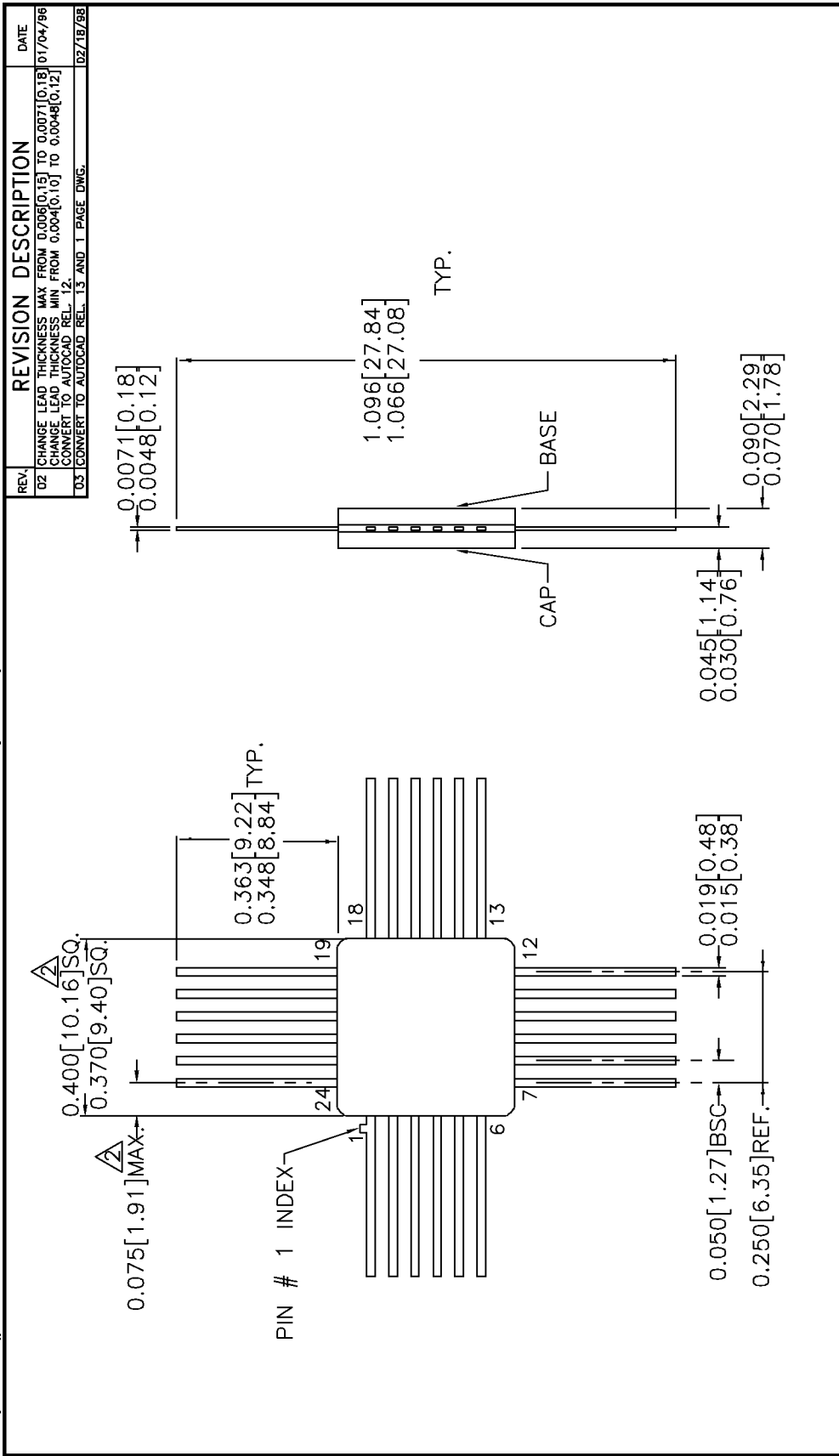
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24 LEAD CERPACK (F24-1)

FILE/REV #: PD0006A03

PD/0006/ASCORP

PAGE 1 OF 1



REV.	REVISION DESCRIPTION	DATE
02	CHANGE LEAD THICKNESS MAX FROM 0.006 [0.15] TO 0.0071 [0.18] CHANGE LEAD THICKNESS MIN FROM 0.004 [0.10] TO 0.0048 [0.12] CONVERT TO AUTOCAD REL. 12.	01/04/96
03	CONVERT TO AUTOCAD REL. 13 AND 1 PAGE DWG.	02/18/98

SYNERGY
SEMICONDUCTOR

3250 SCOTT BOULEVARD
SANTA CLARA, CA 95054
TEL: 408-980-9191
FAX: 408-587-7878

24 LEAD CERPACK
PACKAGE OUTLINE

APPROVALS: DATE: APPROVALS: DATE: APPROVALS: DATE: APPROVALS: DATE:
ORIGINATOR: FERNIN G. URRUTIA 02/23/98 QUALITY: MARSHALL WILDER
CHK'D: WON CHANG DOCUMENT CONTROL: BRIAN SANFLEPPD
RELEASE DATE:

SIZE: A
SCALE: IN/A
REVISION: 03

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- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
 2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

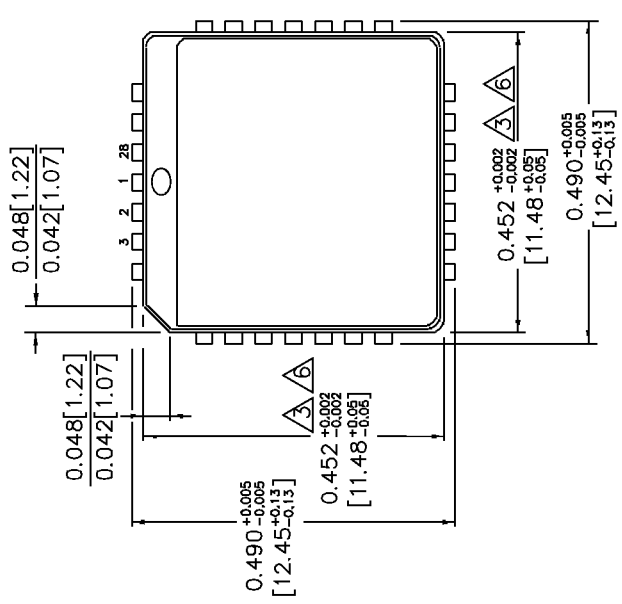
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PD/0008/ASCORP

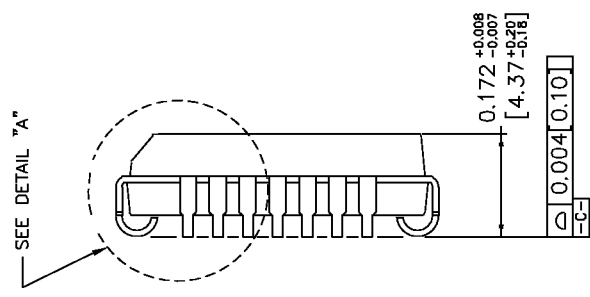
PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION A.0. FORMAT AND COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450[11.43] TO 0.443[11.25]. TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34653 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 15 AND ONE PAGE DOCUMENT.	02/18/98

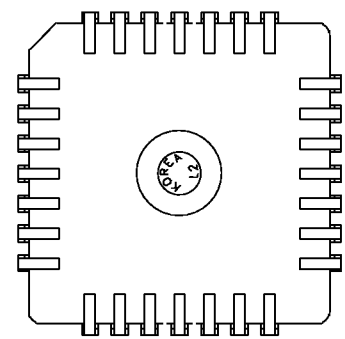
TOP VIEW



SIDE VIEW

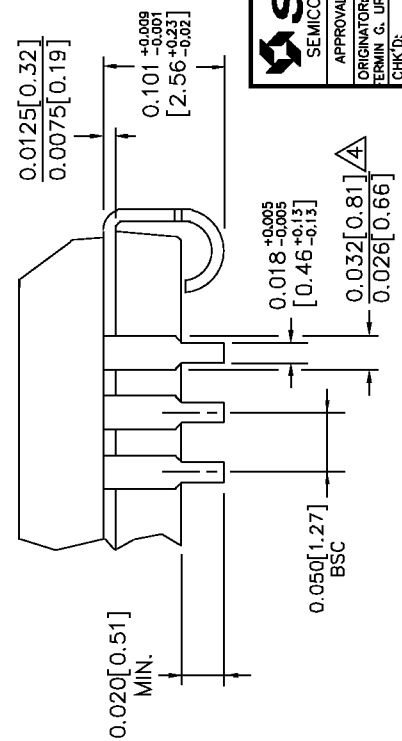


BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



SYNERGY
SEMICONDUCTOR

3250 SCOTT BOULEVARD
SANTA CLARA, CA. 95054
TEL: 408-960-9191
FAX: 408-367-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	28 LEAD PLCC
ORIGINATOR: ERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

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SCALE: N/A
REVISION: 03