15

Electrical Specifications

This chapter specifies the following electrical behavior of the 21150:

- PCI electrical conformance
- Absolute maximum ratings
- dc specifications
- ac timing specifications

15.1 PCI Electrical Specification Conformance

The 21150 PCI pins conform to the basic set of PCI electrical specifications in the *PCI Local Bus Specification, Revision 2.1.* See that document for a complete description of the PCI I/O protocol and pin ac specifications.

15.2 Absolute Maximum Ratings

The 21150 is specified to operate at a maximum frequency of 33 MHz at a junction temperature (T_j) not to exceed 125°C. Table 15–1 lists the absolute maximum ratings for the 21150. These are stress ratings only; extended exposure to the maximum ratings may affect the reliability of the device.

Table 15–1 Absolute Maximum Ratings

Parameter	Minimum	Maximum
T_j	—	125°C
T_a	—	70°C
P_{WC}	—	1.2 W @ 33 MHz
Storage temperature range	–55°C	125°C

15.3 dc Specifications

Table 15–2 defines the dc parameters met by all 21150 signals under normal operating conditions.

Table 15–2 dc Parameters

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{cc}	Supply voltage	—	3.0	3.6	V
V_{il}	Low-level input voltage[1]	—	–0.5	0.3 V_{cc}	V
V_{ih}	High-level input voltage[1]	—	0.5 V_{cc}	V_{cc} + 0.5 V	V
V_{ol}	Low-level output voltage[2]	I_{out} = 1500 µA	—	0.1 V_{cc}	V
V_{ol5V}	Low-level output voltage[3]	I_{out} = 6 mA	—	0.55	V
V_{oh}	High-level output voltage[2]	I_{out} = –500 µA	0.9 V_{cc}	—	V
V_{oh5V}	High-level output voltage[3]	I_{out} = –2 mA	2.4	—	V
I_{il}	Low-level input leakage current[1,4]	0 < V_{in} < V_{cc}	—	±10	µA
C_{in}	Input pin capacitance	—	—	10.0	pF
C_{IDSEL}	**p_idsel** pin capacitance	—	—	8.0	pF
C_{clk}	**p_clk**, **s_clk** pin capacitance	—	5.0	12.0	pF

[1]Guarantees meeting the specification for the 5-V signaling environment.

[2]For 3.3-V signaling environment.

[3]For 5-V signaling environment.

[4]Input leakage currents include high-Z ouput leakage for all bidirectional buffers with tristate outputs.

Note

In Table 15–2, currents into the chip (chip sinking) are denoted as positive (+) current. Currents from the chip (chip sourcing) are denoted as negative (–) current.

15.4 ac Timing Specifications

The next sections specify the following:

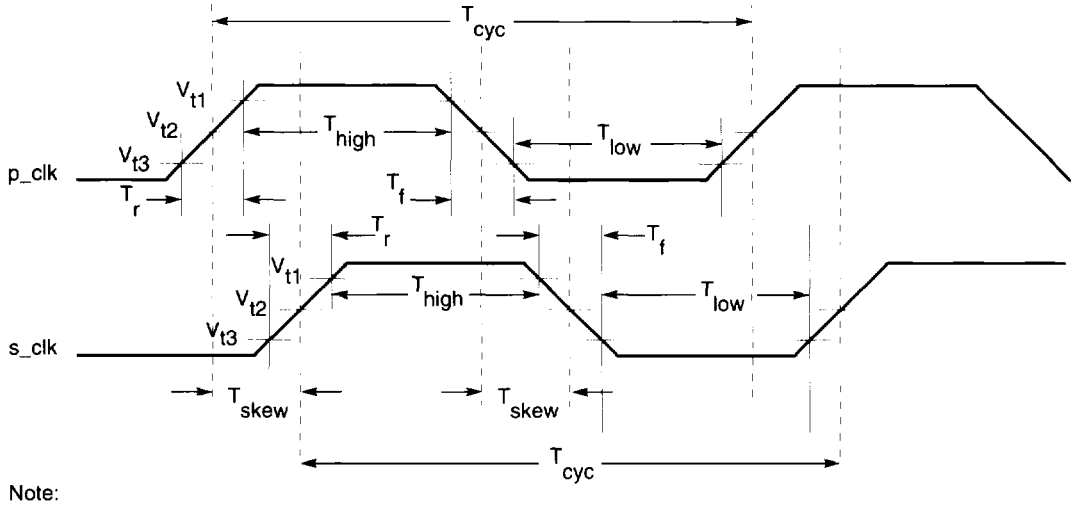
- Clock timing specifications
- PCI signal timing specifications
- Reset timing specifications
- **gpio** timing specifications
- JTAG timing specifications

15.4.1 Clock Timing Specifications

The ac specifications consist of input requirements and output responses. The input requirements consist of setup and hold times, pulse widths, and high and low times. Output responses are delays from clock to signal. The ac specifications are defined separately for each clock domain within the 21150.

Figure 15–1 shows the ac parameter measurements for the **p_clk** and **s_clk** signals, and Table 15–3 specifies **p_clk** and **s_clk** parameter values for clock signal ac timing. See also Figure 15–2 for a further illustration of signal timing.

Figure 15–1 PCI Clock Signal ac Parameter Measurements



Note:

V_{t1} – 2.0 V for 5-V clocks; 0.5 V_{cc} for 3.3-V clocks

V_{t2} – 1.5 V for 5-V clocks; 0.4 V_{cc} for 3.3-V clocks

V_{t3} – 0.8 V for 5-V clocks; 0.3 V_{cc} for 3.3-V clocks

LJ-04738.AI4

15.4 ac Timing Specifications

Table 15–3 PCI Clock Signal ac Parameters

Symbol	Parameter	Minimum	Maximum	Unit
T_{cyc}	**p_clk**, **s_clk** cycle time	30	∞	ns
T_{high}	**p_clk**, **s_clk** high time	11	—	ns
T_{low}	**p_clk**, **s_clk** low time	11	—	ns
	p_clk, **s_clk** slew rate[1]	1	4	V/ns
T_{sclk}	Delay from **p_clk** to **s_clk**	0	7	ns
T_{sclkr}	**p_clk** rising to **s_clk_o** rising	0	5	ns
T_{sclkf}	**p_clk** falling to **s_clk_o** falling[2]	0	5	ns
T_{dskew}	**s_clk_0** duty cycle skew from **p_clk** duty cycle[2]	—	0.750	ns
T_{skew}	**s_clk_0<x>** to **s_clk_0<y>**	—	0.500	ns

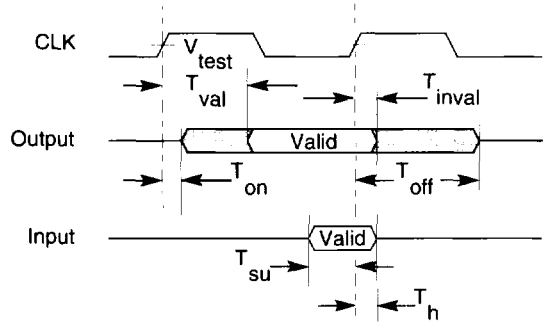
[1]0.2 V_{cc} to 0.6 V_{cc}.

[2]Measured with 30-pF lumped load.

15.4.2 PCI Signal Timing Specifications

Figure 15–2 and Table 15–4 show the PCI signal timing specifications.

Figure 15–2 PCI Signal Timing Measurement Conditions



Note:
V_{test} – 1.5 V for 5-V signals; 0.4 V_{cc} for 3.3-V signals

LJ-04739.AI4

15.4 ac Timing Specifications

Table 15–4 PCI Signal Timing

Symbol	Parameter	Minimum	Maximum	Unit
T_{val}	CLK to signal valid delay—bused signals [1.2.3]	2	11	ns
$T_{val(ptp)}$	CLK to signal valid delay—point-to-point [1.2.3]	2	12	ns
T_{on}	Float to active delay[1.2]	2	—	ns
T_{off}	Active to float delay[1.2]	—	28	ns
T_{su}	Input setup time to CLK—bused signals [1.2.3]	7	—	ns
$T_{su(ptp)}$	Input setup time to CLK—point-to-point [1.2.3]	10, 12	—	ns
T_h	Input signal hold time from CLK[1.2]	0	—	ns

[1]See Figure 15–2.

[2]All primary interface signals are synchronized to **p_clk**. All secondary interface signals are synchronized to **s_clk**.

[3]Point-to-point signals are **p_req_l**, **s_req_l<8:0>**, **p_gnt_l**, and **s_gnt_l<8:0>**.
Bused signals are **p_ad**, **p_cbe_l**, **p_par**, **p_perr_l**, **p_serr_l**, **p_frame_l**, **p_irdy_l**, **p_trdy_l**, **p_lock_l**, **p_devsel_l**, **p_stop_l**, **p_idsel**, **s_ad**, **s_cbe_l**, **s_par**, **s_perr_l**, **s_serr_l**, **s_frame_l**, **s_irdy_l**, **s_trdy_l**, **s_lock_l**, **s_devsel_l**, and **s_stop_l**.

15.4.3 Reset Timing Specifications

Table 15–5 shows the reset timing specifications for **p_rst_l** and **s_rst_l**.

Table 15–5 Reset Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{rst}	**p_rst_l** active time after power stable	1	—	µs
$T_{rst-clk}$	**p_rst_l** active time after **p_clk** stable	100	—	µs
$T_{rst-off}$	**p_rst_l** active-to-output float delay	—	40	ns
T_{srst}	**s_rst_l** active after **p_rst_l** assertion	—	40	ns
$T_{srst-on}$	**s_rst_l** active time after **s_clk** stable	100	—	µs
T_{dsrst}	**s_rst_l** deassertion after **p_rst_l** deassertion	20	25	Cycles
	p_rst_l slew rate[1]	50	—	mV/ns

[1]Applies to rising (deasserting) edge only.

15.4.4 gpio Timing Specifications

Table 15–6 shows the **gpio** timing specifications. See also Figure 15–2.

Table 15–6 gpio Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{vgpio}	**s_clk**-to-**gpio** output valid	2	12	ns
T_{gon}	**gpio** float-to-active delay	2	—	ns
T_{goff}	**gpio** active-to-float delay	—	28	ns
T_{gsu}	**gpio**-to-**s_clk** setup time	7	—	ns
T_{gh}	**gpio** hold time after **s_clk**	0	—	ns
T_{gcval}	**s_clk**-to-**gpio<0>** shift clock output valid	—	13.5	ns
T_{gcyc}	**gpio<0>** cycle time	30	∞	ns
T_{gsval}	**gpio<0>**-to-**gpio<2>** shift control output valid	—	8	ns
T_{msu}	**msk_in** setup time to **gpio<0>**	15	—	ns
T_{mh}	**msk_in** hold time after **gpio<0>**	0	—	ns

15.4.5 JTAG Timing Specifications

Table 15–7 shows the JTAG timing specifications.

Table 15–7 JTAG Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{jf}	**tck** frequency	0	10	MHz
T_{jp}	**tck** period	100	∞	ns
T_{jht}	**tck** high time	45	—	ns
T_{jlt}	**tck** low time	45	—	ns
T_{jrt}	**tck** rise time[1]	—	10	ns
T_{jft}	**tck** fall time[2]	—	10	ns
T_{js}	**tdi**, **tms** setup time to **tck** rising edge	10	—	ns
T_{jh}	**tdi**, **tms** hold time from **tck** rising edge	25	—	ns
T_{jd}	**tdo** valid delay from **tck** falling edge[3]	—	30	ns
T_{jfd}	**tdo** float delay from **tck** falling edge	—	30	ns

[1]Measured between 0.8 V and 2.0 V.
[2]Measured between 2.0 V and 0.8 V.
[3]C_1 = 50 pF.