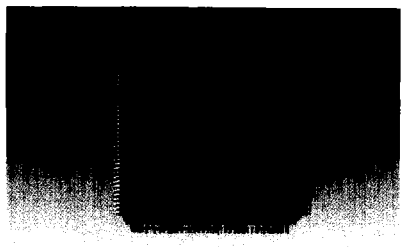
CONTROLLER ICs for OPTICAL DISK

AK8702 MO Disk Controller



144pin LQFP (20×20×1.6mm)

① Disk formats supported
- 90mm 1X, 2X (512byte/sector)
- 130mm 1X, 2X, 3X, 4X (512byte/sector, 1024byte/sector)
- HS format (2408byte/sector)

② SCSI interface
- Connects directly to single ended SCSI bus
- Connectable to differential SCSI bus
- Complies with ANSI SCSI-1 and SCSI-2
- Transfer rate: Synchronous transfer max. 10Mbyte/sec.
  Asynchronous transfer max. 5Mbyte/sec.

③ Drive (Endec) Interface
- Transfer rate: max. 6.67Mbyte/sec. (53Mbps)

④ High speed Reed-Solomon encoding/decoding
- On the fly hardware error correction of up to 6.67Mbye/sec. with maximum number of errors
- Error correction of 8 bytes/interleave
- Programmable error threshold

⑤ Buffer DRAM interface
- Support to 16Mbytes of DRAM
- Support of x1, x4, x8, x9 bit DRAM configuration
- ring buffer manager with full/empty warning/abort
- Slidable 4k DRAM window access from microprocessor

⑥ Microprocessor interface
- Connectable to Motorola/Intel type microprocessor
- Support of Address Data Mux/Demux bus

⑦ 3 Low power modes

⑧ Package: 144 pin LQFP

AK8712 MO Disk Endec/Formatter

① Disk Formats Supported
- 90mm 1X (128MB), 2X (230MB), 5X (640MB)
- 130mm 1X (650MB), 2X (1.3GB), 3X (2GB), 4X (2.6GB)

② Programmable Formatter Function
- selectable sector size: 512, 1024, 2048 Bytes/sector
- VF03, SYNC and RESYNC pattern generation
- programmable Sector Mark, Address Mark, SYNC pattern and RESYNC pattern detection window
- variable threshold voting for Sector Mark, Address Mark, Address ID, SYNC pattern and RESYNC pattern detection
- variable write/erase data transmission start timing to optical drive

③ ENDEC Function
- selectable RLL (2,7) or RLL (1,7) encoding/decoding

④ High speed operation
- reference clock rate: Max. 90M channel-bits/sec (When 3V-CMOS level interface is used)

⑤ Various command operations

⑥ Variable timing pulse output
- general purpose pulse output: 4 channels

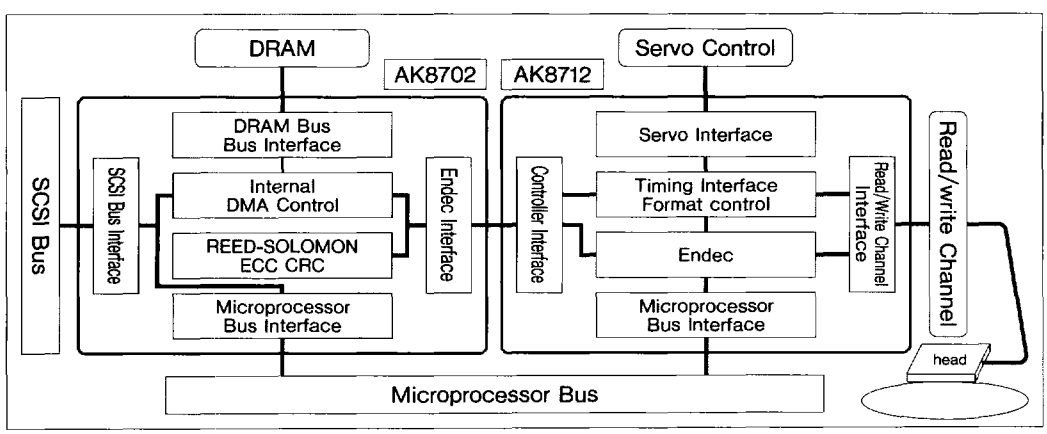
⑦ Microprocessor Interface
- connectable to Motorola/Intel type microprocessors
- support of Address Data Mux/Demux bus

⑧ Optical disk controller interface
- 8 bits parallel data bus with parity option

⑨ ID output interface
- current address ID can be read out directly

⑩ Low power mode

⑪ Package: 100 pin LQFP (14×14×1.6mm)



AK8702/12 BLOCK DIAGRAM