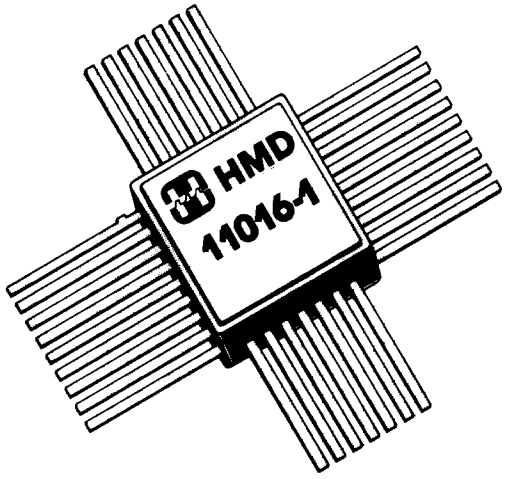
GaAs DIGITAL IC
DIVIDE BY 2/4/8 BINARY COUNTER
HMD-11016-1 DC — 2.0 GHz OPERATION

PRODUCT DATA 12050/ NOVEMBER 1987

HARRIS MICROWAVE SEMICONDUCTOR



TRUTH TABLE

CLR	ENABLE	÷N OUT	DATA IN	FUNCTION
H	L	÷N	DI	Outputs ÷N
H	H	Latch	DI	Outputs latched
L	X	L	DI	Outputs low

NOTE: Master Clear, Data Enable = Logical High 0.0 V to -0.8 V; Logical Low -2.0 V.

LOGIC DIAGRAM

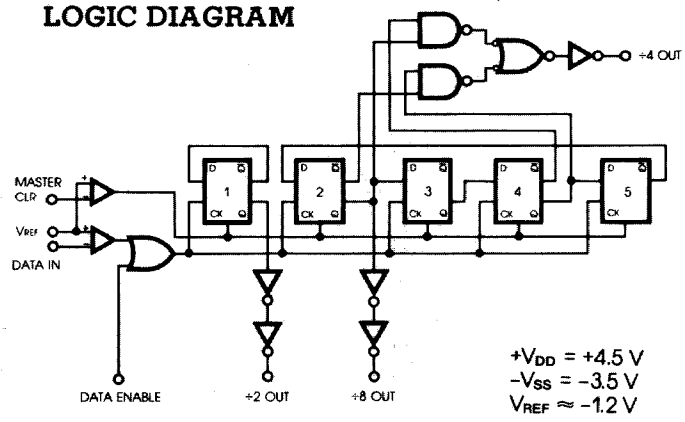


FIGURE 1

FEATURES

- ☐ 2.0 GHz data input rate
- ☐ ECL compatible and GaAs compatible I/Os
- ☐ Synchronous operation with simultaneous divide by 2, 4, and 8 outputs
- ☐ Asynchronous master clear and enable for down counter operation
- ☐ 50 ohm impedance system operation
- ☐ Single ended input/output
- ☐ Metal flatpack packaging for optimum performance in GHz transmission systems
- ☐ Reliable Ti/Pt/Au metallization system
- ☐ Temperature range: -55°C to +85°C

GENERAL DESCRIPTION

The HMD-11016-1 is a Gallium Arsenide Digital Integrated Circuit which has been designed by Harris Microwave Semiconductor to perform binary counter and fixed divide functions at input data rates in excess of those available with silicon-based units. Capable of specified performance over an expanded temperature range, the HMD-11016-1 performs fixed divide by two, four, and eight, and supplies these three outputs simultaneously to facilitate bit-steering applications. A data enable input permits the unit to be used as a (count down) binary counter.

Its compatibility with ECL and other GaAs products afford its use in a broad range of signal processing applications previously only possible at reduced throughput rates. Housed in a hermetic package designed to minimize parasitic and cross talk performance degradation, the HMD-11016-1 is suitable for use in applications requiring subnanosecond system response times and reliable operation.

The HMD-11016-1 is a member of the Harris Microwave Semiconductor HMD-11 family of small and medium scale GaAs ICs.

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FUNCTION DESCRIPTION

The HMD-11016-1 contains five D-type flip-flops. These flip-flops are fully synchronous and are driven in parallel through Data In. The HMD-11016-1 acts as a binary counter 2/4/8 divider which accepts data inputs at frequencies up to 1800 MHz minimum. The first flip-flop is used as a binary element for the divide-by-two function with outputs at one half data rate input. The remaining flip-flops are used to develop the divide-by-eight output. The divide-by-four function is derived from the different internal phases of the divide-by-eight function with an output at one-fourth the data rate input. A separate reference voltage, V_{REF} (with $^{6}10 = A$) must be supplied to the device. This reference voltage will provide input tuning capability for maximum frequency response, including performance across temperature ranges. V_{REF} is typically -0.4 V, but can be adjusted to optimize device performance.

DC CHARACTERISTICS: V_{DD} = +4.5 V, V_{SS} = -3.5 V

SYMBOL	PARAMETERS	LIMITS TYP	UNITS	CONDITIONS T_A = 25°C
I_{IH}	Input Current High	10	μA	$V_{IN} = V_{IH}$
I_{DD}	Supply Current	350	mA	Input & Output Open
I_{SS}	Supply Current	250	mA	Input & Output Open
V_{REF}	Reference Voltage	-0.4 ±0.1	V	$I_{REF} \leq 10\mu A$, ECL Level
V_{OH}	Output Logical High	-0.7	V	50 Ω Output Load
V_{OL}	Output Logical Low	-1.8	V	50 Ω Output Load

DYNAMIC CHARACTERISTICS: V_{DD} = +4.5 V, V_{SS} = -3.5 V, $V_{REF} \approx$-0.4 V

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS T_A = 25°C
t_{PLH}, t_{PHL}	Propagation Delay[1]		1000		ps	See Figure 5
Data In	Max. Data Input Rate	1800	2000		MHz	See Figure 5
t_{TLH}, t_{THL}	Transition Time 20% to 80%, 80% to 20%		150		ps	See Figure 5
t_{QNH}	Clear to Q Out High		200		ps	See Figure 5 @ 2000 MHz
t_{QNL}	Clear to Q Out Low		200		ps	See Figure 5 @ 2000 MHz

NOTE: 1. Refer to Figure 2 for definition of propagation delay measurements.

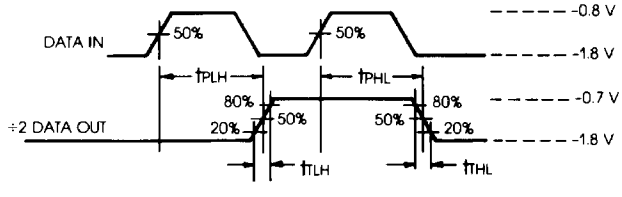


FIGURE 2 — TYPICAL WAVEFORM, DATA IN, DATA DIVIDE BY 2 (50Ω TERMINATION)

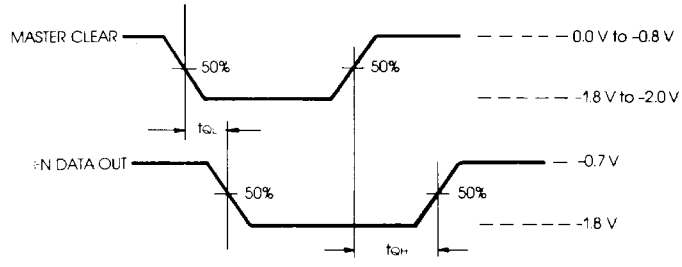
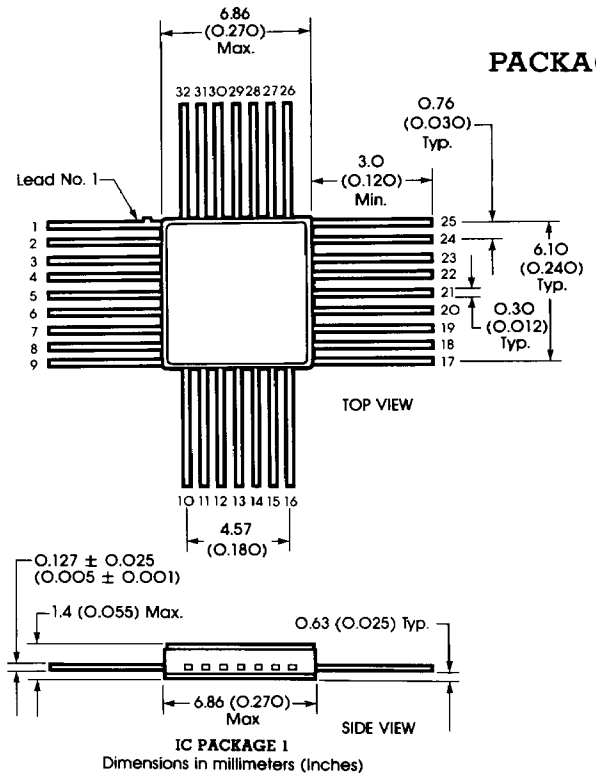


FIGURE 3 — ASYNCHRONOUS MASTER CLEAR (50 Ω TERMINATION)

PACKAGE/PIN CONFIGURATION



IC PACKAGE 1
Dimensions in millimeters (Inches)

PIN NO.	SYMBOL & FUNCTION		PIN NO.	SYMBOL & FUNCTION	
1	GND	Ground (RF)	17	GND	Ground (RF)
2	DE	Data Enable	18	NC	No Connection
3	GND	Ground (RF)	19	GND	Ground (RF)
4	V_{REF}	User Supplied Reference Voltage	20	DI	Data Input
			21	GND	Ground (RF)
5	GND	Ground (RF)	22	MC	Master Clear
6	÷2	÷2(Q) Output	23	GND	Ground (RF)
7	GND	Ground (RF)	24	NC	No Connection
8	÷8	÷8(Q) Output	25	GND	Ground (RF)
9	GND	Ground (RF)	26	GND	Ground (RF)
10	GND	Ground (RF)	27	$+V_{DD}$	Supply Voltage
11	÷4	÷4(Q) Output	28	GND	Ground (DC)
12	GND	Ground (RF)	29	$-V_{SS}$	Supply Voltage
13	$-V_{SS}$	Supply Voltage	30	GND	Ground (RF)
14	GND	Ground (DC)	31	NC	No Connection
15	$+V_{DD}$	Supply Voltage	32	GND	Ground (RF)
16	NC	No Connection			

NOTES:
1. Grounding Pins: 1, 3, 5, 7, 9, 10, 12, 14, 17, 19, 21, 23, 25, 26, 28, 30, 32.
2. Pins 14 & 28 are for DC returns, all others require RF grounding only.

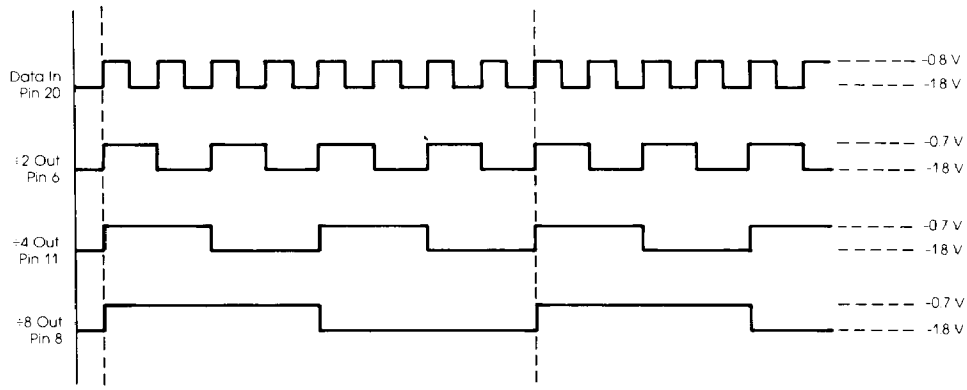
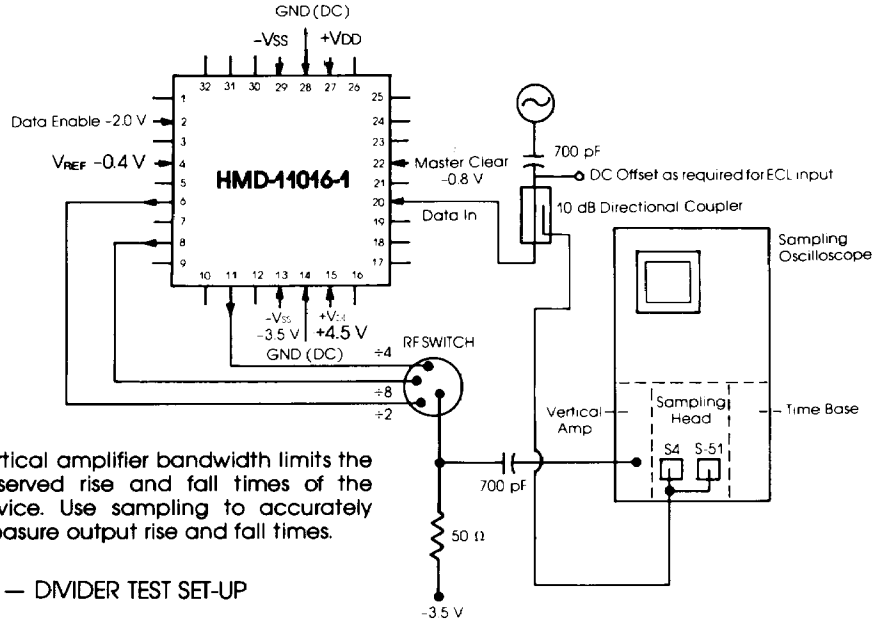


FIGURE 4 — DIVIDER OUTPUT WAVEFORM TIMING (50Ω TERMINATION)



NOTE: Vertical amplifier bandwidth limits the observed rise and fall times of the device. Use sampling to accurately measure output rise and fall times.

FIGURE 5 — DIVIDER TEST SET-UP

PRODUCT RATINGS

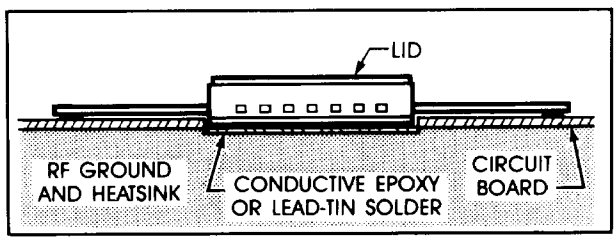
SYMBOL	PARAMETERS	MAXIMUM RATINGS[1]
V_{DD}	Drain Supply Voltage	+5.2 V
V_{SS}	Source Supply Voltage	-4.0 V
I_{OUT}	Output Current	60 mA
P_{DSS}	Power Dissipation	3.0 W
T_{STG}	Storage Temperature Range	-55°C to +150°C
T_{CASE}	Case Base Temperature Range	-55°C to +85°C

1. Permanent damage may result from operation at conditions beyond maximum ratings.

IC MOUNTING PROCEDURES

It is imperative that adequate heatsinking of the IC package be provided in the application circuit. The chip is die attached directly to the bottom of the case, and both the bottom and lid are grounded.

- The primary avenue for heat removal is through the bottom of the case to a heatsink at ground potential. Voids and gaps in the contact between the case and the heatsink are to be avoided.
- An electrically conductive attachment material is recommended. A conductive epoxy, such as Abel Stick 36-2, 88-1 (or equivalent), or a lead-tin solder (with flux) may be used.
- Supplemental heatsinking for the case lid and forced air cooling can lower the device temperature further.



IC HANDLING PROCEDURES

Permanent damage to the device can result from inadequate protection against excessive voltages on the device due to static charge buildup, test equipment transients and inductive pickup. Grounding of equipment and personnel during the handling and testing of GaAs ICs, and control of the unit's test conditions and environment, should be standard procedures.

Elimination or reduction of damage due to static charge or other causes can be accomplished as follows:

- Use conductive work stations. Metallic or conductive plastic tops on work benches connected to ground help eliminate static buildup.
- Ground all handling equipment and soldering iron tips.
- Ground all handling personnel with a conductive bracelet through 1M ohm to ground. The 1M ohm resistor helps protect the handler from electroshock.
- Certain materials, highly dielectric in nature, will hold or aid in the generation of a static charge. Smocks, clothing, and shoes of these insulating materials (notably nylon) should not be worn in areas where devices are handled. Natural materials such as cotton, etc. should be used to minimize charge generation capacity.
- Control relative humidity to as high a level as practical (RH 50%).
- Ionized air blowers reduce charge buildup in areas where ground is not possible or desirable.
- Devices should be in conductive carriers during all phases of transport. Leads may be shorted by metallic carriers, conductive foam or foil.
- Mount and remove GaAs ICs with power removed.
- Do not exceed the maximum product ratings specified.

APPLICATIONS INFORMATION

- All unused device inputs should be connected to RF ground to prevent electrostatic charge damage.
- In order to prevent high frequency oscillations, a 0.1 μf capacitor is recommended between the IC's ground and voltage supplies.
- It is recommended that for best performance, microstrip, stripline or coplanar transmission lines be used.
- When driving ECL, stub lengths can be extended up to 1 inch. The termination resistor should be connected to -3.5 volts for full ECL.
- When laying out components, the designer must meet two conditions. First, R_T must terminate the transmission line at only one point. Second, any unterminated stub lengths must be kept under 0.25 inches for driving GaAs circuits.
- V_{REF} of -0.4 V ±0.1 V must be supplied to the GaAs devices in order to fine-tune their maximum Data In performance, including performance across operating temperature range.
- IC inputs and outputs are matched for use with 50 ohm impedance systems (35 to 65 ohms). Output lines can drive 35 to 65 ohms terminating resistor loads and up to 1 pf of capacitance (at 125 ps rise and fall times).

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