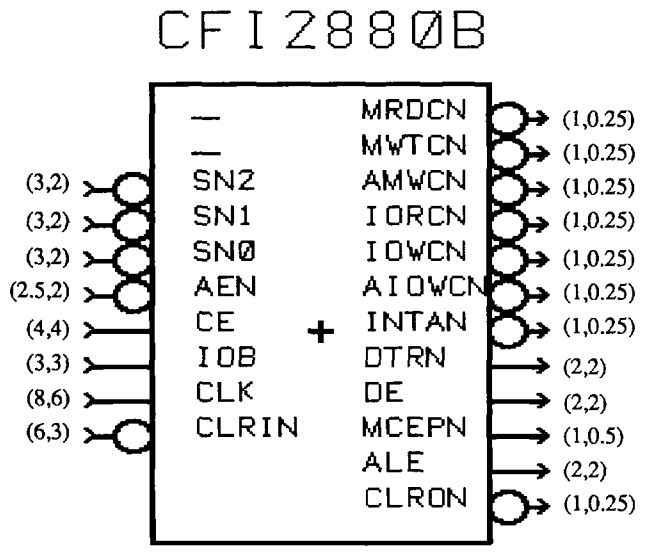
**GENERAL DESCRIPTION:** INTEL 8288 - BUS CONTROLLER

CFI2880B is designed to be fully compatible with I8288A Bus Controller with the exceptions that two I/O pins—CLRIN, CLRON—are added to reset the internal state machine, commands have no HIGH-Z outputs, and AEN enables output commands immediately after it is active (LOW). CLRIN is the asynchronous clear input which resets the megafunction to T1 state. CLRON is the clear output, which goes HIGH when no command comes in (status bits stay HIGH) for more than two cycles. The user can hook it to CLRIN so that no extra signal is required to reset the state machine. To reset the state machine, the user can also connect the output of a power-on-reset cell to CLRIN. CFI2880B needs to be reset only at the beginning. Further control of the state machine is not recommended. Three-state outputs can be implemented by using AEN as the three-state control signal. Outputs are enabled when it is LOW. All inputs and outputs have the same polarities as in the I8288. AEN is active LOW and CE is active HIGH. For further functional descriptions, the user should refer to I8288 datasheet.

**PIN CONNECTION DIAGRAM:**




**FEATURES:**

- Compatible with the I8288A Bus Controller

**EQUIVALENT USED GATES:** 148 GATES
(for rough area estimates)

**THIS MEGAFUNCTION CONSISTS OF :**
148 soft-coded gates.

**POWER:** NOT AVAILABLE.

**FAULT COVERAGE(%):** 100%

This megafunction was designed to be 100% functionally compatible as specified in the vendor's data book. However, LSI LOGIC makes no warranty that this megafunction behaves identically to the standard part. It is the user's responsibility to assure that the megafunction operates correctly in his/her ASIC design and meets desired system requirements.

INPUTS ( Loadings in transistor pairs)

| Name | Loading | Description |
|---|---|---|
| SN2:0 | 3 | Status inputs |
| AEN | 2.5 | Address enable signal, active Low |
| CE | 4 | Command enable input |
| IOB | 3 | Input/Output bus mode select signal |
| CLK | 8 | Clock |
| CLRIN | 6 | External asynchronous clear signal, active Low |

OUTPUTS

| Name | ( #p , #n ) | Description |
|---|---|---|
| MRDCN | ( 1 , .25) | Memory read command, active Low |
| MWTCN | ( 1 , .25) | Memory write command, active Low |
| AMWCN | ( 1 , .25) | Advanced memory write command, active Lo |
| IORCN | ( 1 , .25) | I/O read command, active Low |
| IOWCN | ( 1 , .25) | I/O write command, active Low |
| AIOWCN | ( 1 , .25) | Advanced I/O write command, active Low |
| INTAN | ( 1 , .25) | Interrupt acknowledge, active Low |
| DTRN | ( 2 , 2 ) | Data transmit/receive, Low means receive |
| DE | ( 2 , 2 ) | Data enable |
| MCEPN | ( 1 , 0.5) | MASTER CASCADE ENABLE OR PERIPHERAL DATA enable, function is defined by IOB |
| ALE | ( 2 , 2 ) | Address latch enable |
| CLRON | ( 1 , .25) | Clear signal, it goes low when SN2:0 sta high for more than 2 cycles |

SWITCHING CHARACTERISTICS

| Symbol | Parameter | Delay(in ns) | Comment |
|---|---|---|---|
| TSVCH | Status active setup time | 7.7 | |
| TCHSV | Status inactive hold time | 2.1 | |
| TSHCL | Status inactive setup time | 9.5 | |
| TCLSH | Status active hold time | 2.1 | |
| TCVNV | Control active delay | 15.7 (max) | 8.3 (min) |
| TCVNX | Control inactive delay | 15.7 (max) | 8.3 (min) |
| TCLLH,TCLMCH | ALE, MCE active delay | 11.2 | (from CLK) |
| TSVLH,TSVMCH | ALE, MCE active delay | 11.8 | (from status) |
| TCHLL | ALE inactive delay | 9.5 (max) | 8.9 (min) |
| TCLML | Command active delay | 12.9 (max) | 6.8 (min) |
| TCLMH | Command inactive delay | 12.9 (max) | 6.8 (min) |
| TCHDTL | Direction control active delay | 4.4 | |
| TCHDTH | Direction control inactive delay | 4.4 | |
| TAELCH | Command enable time | 8.2 | |
| TAEHCZ | Command disable time | 8.2 | |
| TAEVNV | AEN to DE | 4.3 | |
| TCEVNV | CEN to DE, PDEN | 5.2 | |
| TCELRH | CEN to command | 9.0 | |
| TCLRO | CLK to CLRON delay | 8.1 | |
| TSVRO | Status to CLRON delay | 5.9 | |

*All timings are based on 10K, nominal conditions with 2 output loadings.