HD74HC674 ● 16-bit Shift Register

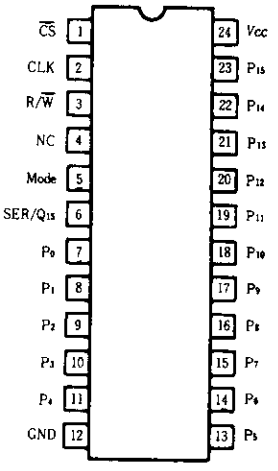
The HD74HC674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (data I/O) port provides access for entering serial data or reading the shift-register word in a recirculating loop.

The device has four basic modes of operation:

1) Hold (do nothing)
2) Write (serially via input/output)
3) Read (serially)
4) Load (parallel via data inputs)

Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

■ PIN ARRANGEMENT

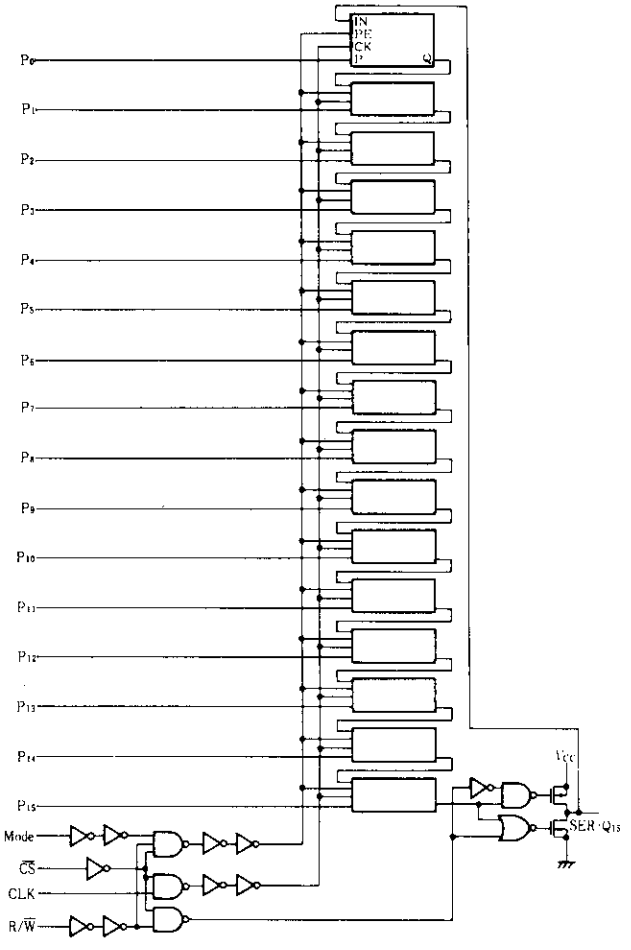


(Top View)

■ FEATURES

- High Speed Operation: t_{pd} (CLK to SER/Q_{15})=17ns typ. (C_L=50pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: V_{CC}=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: I_{CC} (static)=4μA max. (Ta=25°C)

■ LOGIC DIAGRAM



■ FUNCTION TABLE

Inputs				SER/	Operation
$\overline{CS}$	R/$\overline{W}$	Mode	CLK	Q15	
H	×	×	×	Z	Do nothing
L	L	×	↓	Z	Shift and Write (Serial load)
L	H	L	↓	Q14n	Shift and Read
L	H	H	↓	P15	Parallel load

■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta=25°C min	Ta=25°C typ	Ta=25°C max	Ta=−40~+85°C min	Ta=−40~+85°C max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OH}=−20μA	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		I_{OH}=−6 mA	4.18	—	—	4.13	—	
		6.0		I_{OH}=−7.8 mA	5.68	—	—	5.63	—	
	V_{OL}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OL}=20μA	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		I_{OL}=6 mA	—	—	0.26	—	0.33	
		6.0		I_{OL}=7.8 mA	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	V_{in}=V_{CC} or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in}=V_{CC} or GND, I_{out}=0 μA		—	—	4.0	—	40	μA
Off-State Output Current	I_{OZ}	6.0	V_{in}=VIH or VIL, V_{out}=V_{CC} or GND		—	—	±0.5	—	±5	μA

■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C min.	typ.	max.	Ta=−40~+85°C min.	max.	Unit
Maximum Clock Frequency	f_{max}	2.0		—	—	5	—	4	MHz
		4.5		—	—	27	—	21	
		6.0		—	—	32	—	25	
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	Clock to SER/Q_{15}	—	—	200	—	250	ns
		4.5		—	17	40	—	50	
		6.0		—	—	34	—	43	
Output Enable Time	t_{ZH} t_{ZL}	2.0		—	—	150	—	190	ns
		4.5		—	12	30	—	38	
		6.0		—	—	26	—	33	
Output Disable Time	t_{HZ} t_{LZ}	2.0		—	—	150	—	190	ns
		4.5		—	14	30	—	38	
		6.0		—	—	26	—	33	
Pulse Width	t_w	2.0		80	—	—	100	—	ns
		4.5		16	6	—	20	—	
		6.0		14	—	—	17	—	
Setup Time	t_{su}	2.0	SER/Q_{15} to Clock	100	—	—	125	—	ns
		4.5		20	—	—	25	—	
		6.0		17	—	—	21	—	
	t_{su}	2.0	P to Clock	100	—	—	125	—	ns
		4.5		20	—	—	25	—	
		6.0		17	—	—	21	—	
	t_{su}	2.0	Mode to Clock	100	—	—	125	—	ns
		4.5		20	—	—	25	—	
		6.0		17	—	—	21	—	
	t_{su}	2.0	R/W or CS to Clock	100	—	—	125	—	ns
		4.5		20	—	—	25	—	
		6.0		17	—	—	21	—	
Hold Time	t_h	2.0	Clock to SER/Q_{15}	5	—	—	5	—	ns
		4.5		5	—	—	5	—	
		6.0		5	—	—	5	—	
	t_h	2.0	Clock to P	5	—	—	5	—	ns
		4.5		5	—	—	5	—	
		6.0		5	—	—	5	—	
	t_h	2.0	Clock to Mode	5	—	—	5	—	ns
		4.5		5	—	—	5	—	
		6.0		5	—	—	5	—	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	60	—	75	ns
		4.5		—	4	12	—	15	
		6.0		—	—	10	—	13	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF