YAMAHA

YMU765

MA-5
Mobile Audio 5

Outline

YMU765 is a synthesizer LSI for mobile phones that realize advanced game sounds of Java application program etc. This LSI has a built-in speaker amplifier, and thus, is an ideal device for outputting sounds that are used by mobile phones in addition to game sounds and ringing melodies that are replayed by a synthesizer.

The synthesizer section adopts the “Stereophonic Hybrid Synthesizer System” which is given advantages of both FM synthesizers and Wave Table synthesizers to allow simultaneous generation of up to 32 FM voices and 32 Wave Table voices. Furthermore, the stream playback function, and the time-variant low pass filter function by AL (Analog Lite) synthesizer have also on board.

Since FM synthesizer is able to present countless voices by specifying parameters with only several tens of bytes, memory capacity and communication band can be saved, and thus, the device exhibits the features in operating environment of mobile phones such as allowing distribution of arbitrary melodies with voices.
On the other hand, Wave Table synthesizer can pronounce the voice built in ROM and arbitrary ADPCM/PCM voices from sequencer by the download of the melody with voices etc..

YMU765 has a built-in hardware sequencer that helps to realize a complex play without heavily loading the host CPU. In addition, it is possible to create more highly efficient applications by the function of time-variant low pass filter. Moreover, the device also has a built-in circuit for controlling vibrators and LEDs synchronizing with play of music.

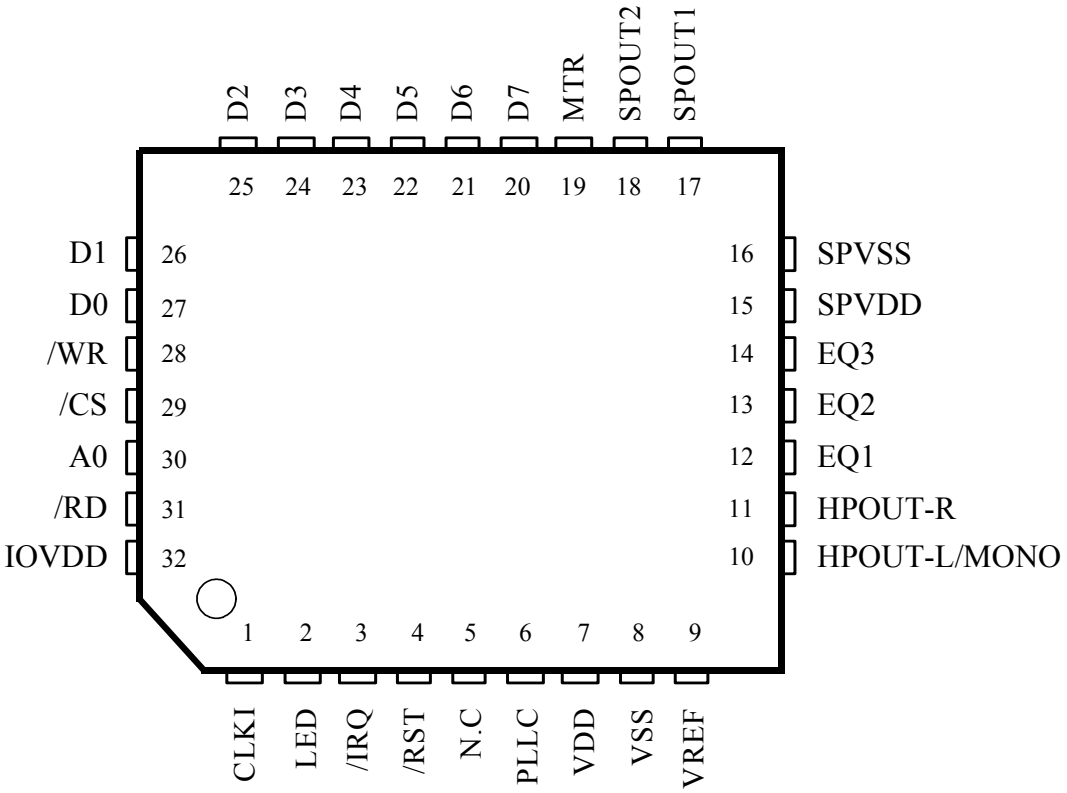
Features

- Built-in the hybrid synthesizer, and possible to generate 64 tones simultaneously as maximum.
- The time fluctuation low pass filter function by AL (Analog Lite) synthesizer is on board.
- Stream replay with ADPCM / PCM is possible.
- Has built-in default voices for FM and Wave Table synthesizers in the ROM, and the voices can be downloaded to RAM.
- Equipped with speaker amplifier and equalizer circuit.
- Equipped with a stereophonic output terminal for headphone.
- Equipped with vibration control circuit, and LED lighting control circuit.
- Has built-in PLL and inputting of master clock up to 27 MHz is possible and compiles with the TCXO (Temperature Compensated Crystal Oscillator).
- Contains a 16-bit stereophonic D/A converter.
- Has power down mode.
- Power supply for core 2.65V ~ 3.30V
- Power supply for I/O 1.65V ~ VDD
- Power supply for speaker amplifier VDD ~ 4.50V
- 32-pin QFN plastic package. The plating of pins is lead-free. (YMU765-QZ)

YAMAHA CORPORATION

YMU765 CATALOG
CATALOG No : LSI-4MU765A3
2003.11

Pin configuration



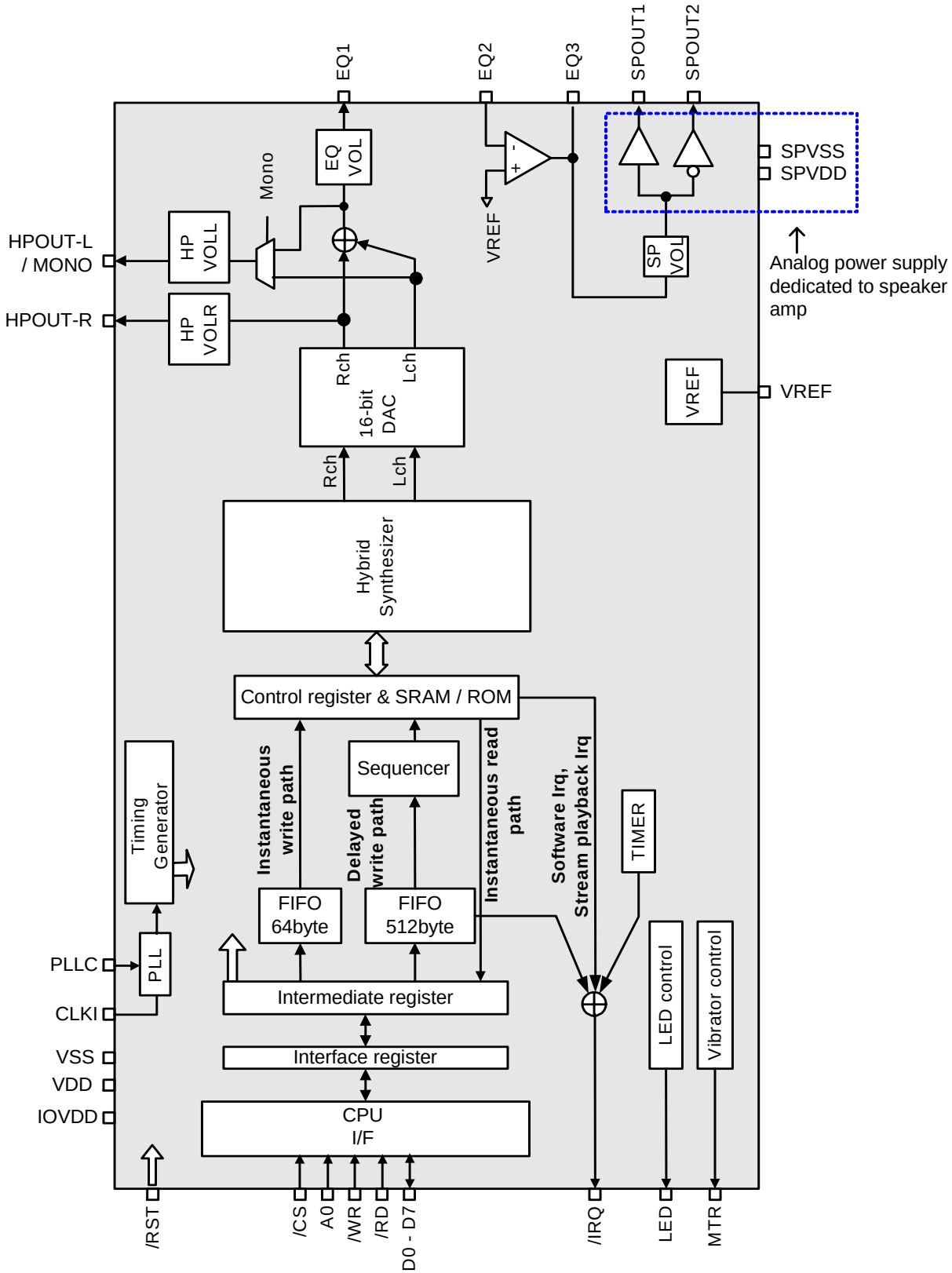
<32pin QFN Top View>

Pin functions

No.	Pin name	I/O	Power supply	Function
1	CLKI	Ish	VDD	Clock input (1.5 MHz ~ 27 MHz) Correspond with TCXO.
2	LED	O	IOVDD	External LED control
3	/IRQ	O	IOVDD	Interrupt output
4	/RST	Ish	IOVDD	Hardware reset input
5	N.C	–	–	No Connection (Be sure to use without connection.)
6	PLLC	A	VDD	Connection of capacitor for built-in PLL Connect a series connection of 1000 pF capacitor and 3.3 kΩ resistor between this pin and VSS(*). (*)Directly connect VSS used here and VSS of 8th pin.
7	VDD	–	–	Power supply (2.65 ~ 3.30V) Connect 0.1 µF and 4.7 µF capacitors between this pin and VSS.
8	VSS	–	–	Ground
9	VREF	A	VDD	Analog reference voltage: Connect 0.1 µF capacitor between this pin and VSS.
10	HPOUT-L / MONO	A	VDD	Headphone output Lch (Can be used as MONO output)
11	HPOUT-R	A	VDD	Headphone output Rch
12	EQ1	A	VDD	Equalizer pin 1
13	EQ2	A	VDD	Equalizer pin 2
14	EQ3	A	VDD	Equalizer pin 3
15	SPVDD	–	–	Speaker amplifier analog power supply (VDD ~ 4.50V) Connect 0.1 µF and 4.7 µF capacitors between this pin and SPVSS.
16	SPVSS	–	–	Speaker amplifier analog ground
17	SPOUT1	A	SPVDD	Speaker connection pin 1
18	SPOUT2	A	SPVDD	Speaker connection pin 2
19	MTR	O	IOVDD	External motor control pin
20	D7	I/O	IOVDD	CPU I/F data bus 7
21	D6	I/O	IOVDD	CPU I/F data bus 6
22	D5	I/O	IOVDD	CPU I/F data bus 5
23	D4	I/O	IOVDD	CPU I/F data bus 4
24	D3	I/O	IOVDD	CPU I/F data bus 3
25	D2	I/O	IOVDD	CPU I/F data bus 2
26	D1	I/O	IOVDD	CPU I/F data bus 1
27	D0	I/O	IOVDD	CPU I/F data bus 0
28	/WR	I	IOVDD	CPU I/F write enable
29	/CS	I	IOVDD	CPU I/F chip select
30	A0	I	IOVDD	CPU I/F address signal
31	/RD	I	IOVDD	CPU I/F read enable
32	IOVDD	–	–	Pin power supply (1.65 ~ VDD)

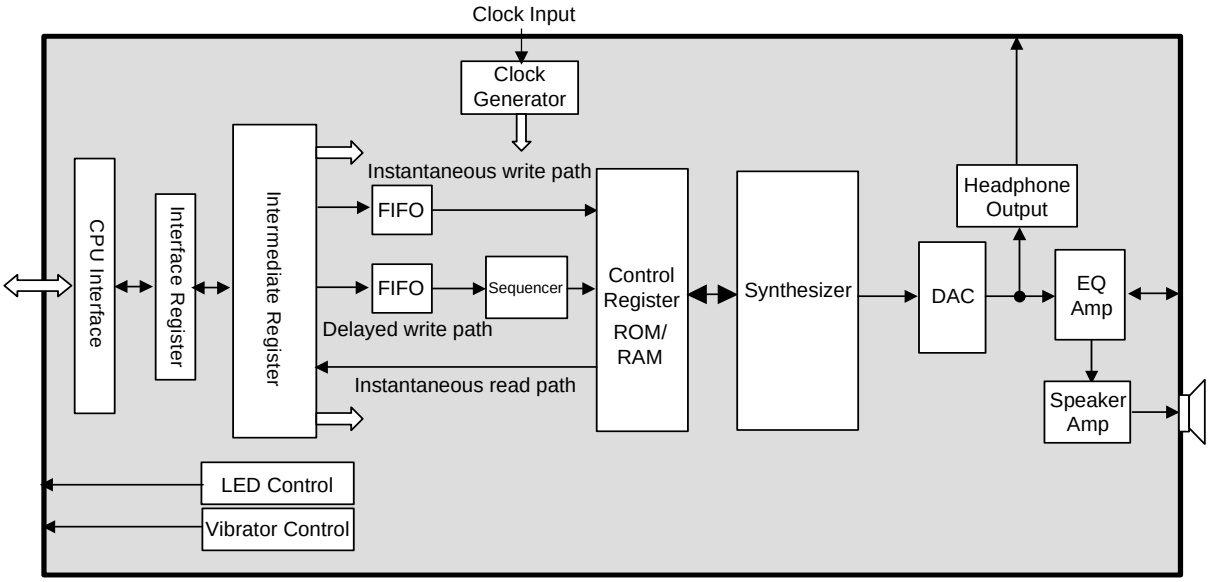
A : Analog pin Ish : Schmitt input

Block diagram



Outline of blocks

This section outlines functions of blocks contained in this device and flow of signals.



CPU interface

CPU interface is an 8-bit parallel type.
It assumes that a total of 13 pins of 4 control signals (/WR, /RD, /CS, A0 pin), 8 data bus (D0 to D7), and 1 Interrupt pin (/IRQ) are connected to the external CPU.
This block controls the writing and reading of data by the input polarity of control signal.

Interface register

This register is able to access directly from the external CPU. There are 2 bytes spaces.
The Intermediate register can be accessed through the Interface register.

Intermediate register

This register is accessed through the Interface register.
It is composed to access a latter control register and ROM/SRAM through Intermediate register.
This register is called the “Intermediate register” since this exists in the middle of the Interface register and the Control register.
In the Intermediate register, there are some registers to control various functions.

Control register, ROM/SRAM

The Control register and ROM/SRAM are accessed from “Instantaneous write register”, “Delayed write register”, and “Instantaneous read register” in the Intermediate register.
In the Control register, there is a register to control the following synthesizer mainly.
The voice parameter for FM (GM 128 voices + DRUM 40 voices) and Wave data for WT are stored in ROM.
SRAM is used at the download of arbitrary FM voice parameter and Wave data for WT.
Moreover, it is used as storing buffer at the stream playback of PCM/ADPCM.

FIFO

This is an abbreviation of “First In First Out” means the memory which data is read in order of written.
There are 2 paths to write into FIFO in the Intermediate register.
The “Instantaneous write path” is for accessing the Control register and ROM/SRAM immediately, also “Delayed write path” is for accessing the Control register after managing time through the sequencer.
FIFO size of Instantaneous path is 64-byte, and its size of Delayed path is 512-byte.

Sequencer

This is for interpreting the contents of data which was written into the Delayed write path.

Generally, “Music data” is written into the Delayed write path. It interprets the contents of music data and controls the synthesizer after sequencer, and then plays the music.

Hybrid synthesizer

This device contains a built-in Polyphonic synthesizer that adopts a stereophonic hybrid system that generates up to 64 tones.

FM synthesizer, WT (Wave Table) synthesizer, Stream playback, and AL (Analog Lite) synthesizer are available.

LED, Vibrator control

It is possible to synchronize an LED and vibrator with a play, and to control. A synchronous control to a play is also possible.

Clock generating block

This device supports a clock input ranging from 1.5 MHz to 27 MHz. (Stop = 0 Hz is possible at power down.)

It is a block to generate a clock which is needed inside of LSI in the PLL.

DAC

It converts digital signals from a synthesizer and a digital audio section into analog signals. The length of a data is 16bits.

Headphone output

There is Stereophonic analog output for Headphone. The monaural output is also possible.

EQ amplifier

The change of Filter characteristic and gain is possible by adjusting the resistors and external parts.

Speaker amplifier

A speaker amplifier, which has maximum output power of 580 mW at SPVDD=3.6V, is integrated this device.

There is a volume to adjust output level in the first part of amplifier.

Electrical Characteristics

■ Absolute maximum rating

Item	Symbol	Min.	Max.	Unit
SPVDD pin, power supply voltage (Speaker amplifier section)	SPVDD	-0.3	6.0	V
VDD pin, power supply voltage	VDD	-0.3	4.2	V
IOVDD pin, power supply voltage	IOVDD	-0.3	4.2	V
SPOUT1, SPOUT2 pin, applied voltage	V_{INSP}	-0.3	SPVDD+0.3	V
Analog input voltage	V_{INA}	-0.3	VDD+0.3	V
Digital input voltage 1 (*1)	V_{IND1}	-0.3	IOVDD+0.3	V
Digital input voltage 2 (*2)	V_{IND2}	-0.3	VDD+0.3	V
Permissible loss (*3)	Pd		1197	mW
Storage temperature	T_{STG}	-50	125	°C

[Condition] VSS = SPVSS = 0V

(*1) Target pin: D0 ~ D7, /CS, A0, /WR, /RD, /RST

(*2) Target pin: CLKI

(*3) Top= 25 °C, and glass epoxy PCB (30mm × 100mm × 1.0mm) is installed.
When operating above Top= 25 °C, permissible loss decreases 12 mW per 1 °C.

■ Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
SPVDD operating voltage (Speaker amplifier section)	SPVDD	VDD	3.60	4.50	V
VDD operating voltage	VDD	2.65	3.00	3.30	V
IOVDD operating voltage	IOVDD	1.65	1.80	VDD	V
Operating ambient temperature	T_{OP}	-20	25	85	°C

[Condition] VSS = SPVSS = 0V

■ Power consumption

Item	Conditions	Typ.	Max.	Unit
Power consumption of VDD+IOVDD	Normal operation (*1)	40		mA
At Silent sound generated SPVDD side		4		mA
At the time of output 400mW / 8ohm load SPVDD side		210		mA
Power down mode Ta = +25°C	VDD+IOVDD+SPVDD (*2)	0.5	2	µA
Power down mode Ta = +85°C	VDD+IOVDD+SPVDD (*2)		10	µA

(*1) VDD=IOVDD=3.00V, SPVDD=3.60V, T_{OP}=25°C

(*2) VDD=IOVDD=3.30V, SPVDD=4.50V
/CS input pin is fixed to V_{IH}=IOVDD, the other input pins are V_{IL}=VSS and V_{IH}=(IO)VDD.

■ **DC characteristics**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage “H” level 1	V_{IH}	(*1)	0.65 × IOVDD			V
Input voltage “L” level 1	V_{IL}	(*1)			0.35 × IOVDD	V
Input voltage “H” level 2	V_{IH}	(*2)	0.75 × IOVDD			V
Input voltage “L” level 2	V_{IL}	(*2)			0.25 × IOVDD	V
Input voltage “H” level 3	V_{IH}	(*3)	0.70 × VDD			V
Input voltage “L” level 3	V_{IL}	(*3)			0.30 × VDD	V
Output voltage “H” level	V_{OH}	(*4) I_{OH} = (*5)	0.80 × IOVDD			V
Output voltage “L” level	V_{OL}	(*4) I_{OL} = (*5)			0.20 × IOVDD	V
Schmitt width 1	Vsh1	/RST pin		0.10×IOVDD		V
Schmitt width 2	Vsh2	CLKI pin		0.10×VDD		V
Input leakage current	IL		-1		1	µA
Input capacity	CI				10	pF

[Condition] T_{OP}=-20 ~ 85°C, VDD=2.65 ~ 3.30V, IOVDD=1.65 ~ VDD[V], Capacitor load=50 pF

(*1) Target pin: D0 ~ D7, /CS, A0, /WR, /RD

(*2) Target pin: /RST

(*3) Target pin: CLKI (In the case of CMOS mode)

(*4) Target pin: D0 ~ D7, /IRQ, LED, MTR

(*5) /IRQ, D0 ~ D7, are I_{OH}= –1 mA, I_{OL}= +1 mA

LED, MTR are I_{OH} = –4 mA, I_{OL}= +4 mA

However, when IOVDD is less than 2.65V, D0 ~ D7, /IRQ, LED, and MTR become I_{OH}=-0.2mA and I_{OL}=+0.2mA.

■ AC characteristics

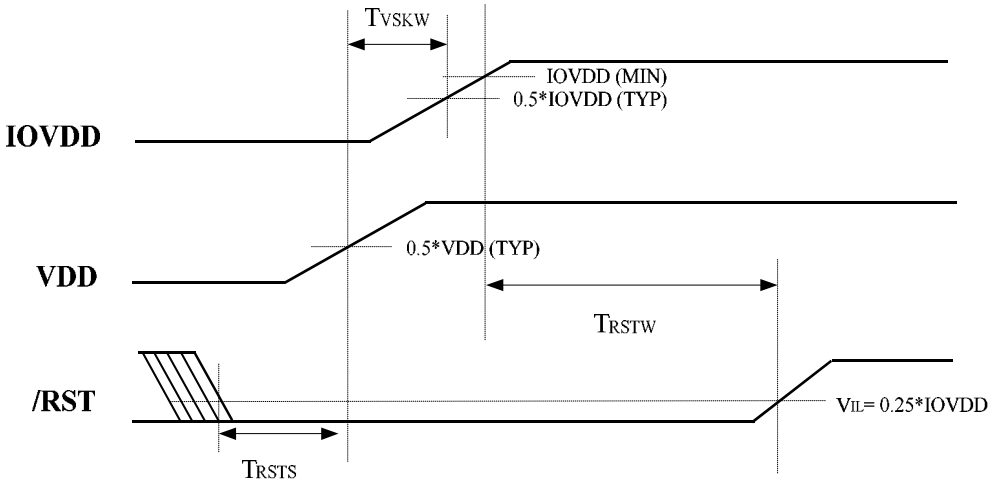
Reset and clock timing

○ /RST, CLKI (CMOS mode), other input signals

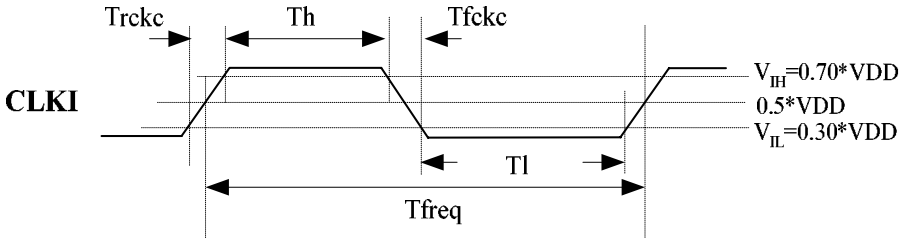
Item	Symbol	Min.	Typ.	Max.	Unit
/RST "L" pulse width	T_{RSTW}	100			µs
/RST (indefinite → L) setup time	T_{RSTS}	0			µs
VDD - IOVDD rise time difference	T_{VSKW}	0		3	ms
CLKI frequency	1 / Tfreq	1.5		27	MHz
CLKI rise / fall time	Trckc / Tfckc			30	ns
CLKI High time	Th	15			ns
CLKI Low time	Tl	15			ns
Input signals other than CLKI rise / fall time	Tr / Tf			20	ns

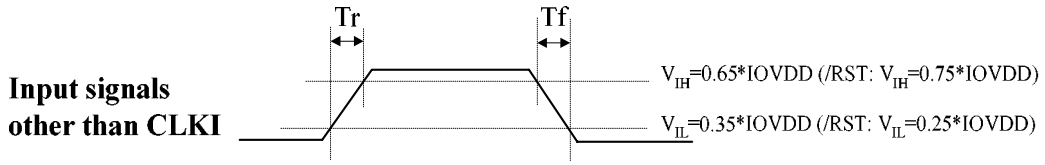
[Condition] T_{OP}=-20 ~ 85°C, VDD=2.65 ~ 3.30V, IOVDD=1.65 ~ VDD[V], Capacitor load=50 pF

The input to Clock can be stopped (=0Hz) during reset period and power down state (DP0=1).
However, the input level is to be H or L, and input of intermediate level is prohibited.
When VDD and IOVDD are used by respectively different power supply, make sure to rise from VDD first.



The reset width is defined as the time from the moment IOVDD has risen to 1.65V.
/RST has to be settled at "L" level at the time VDD has risen to 50%.



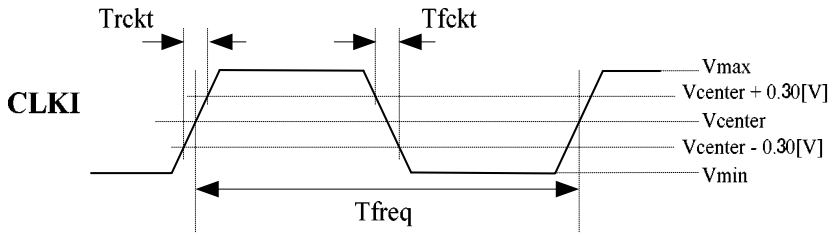


○ CLKI (TCXO mode)

Item	Symbol	Min.	Typ.	Max.	Unit
CLKI frequency	1 / Tfreq	1.5		27	MHz
CLKI rise / fall time	Trckt , Tfckt			250	ns
CLKI amplitude H (1.5MHz ≤ CLKI frequency ≤ 20MHz)	Vmax - Vcenter	0.30		0.35 × VDD	V
CLKI amplitude L (1.5MHz ≤ CLKI frequency ≤ 20MHz)	Vcenter - Vmin	0.30		0.35 × VDD	V
CLKI amplitude H (20MHz < CLKI frequency ≤ 27MHz)	Vmax - Vcenter	0.45		0.35 × VDD	V
CLKI amplitude L (20MHz < CLKI frequency ≤ 27MHz)	Vcenter - Vmin	0.45		0.35 × VDD	V
Wait time to stable operation (*1)	Twait	2			ms
Feedback resistance	Rck	30	45	63	kΩ

[Condition] T_{OP}=-20 ~ 85°C, VDD=2.65 ~ 3.30V, Capacitor load=50pF

(*1) : The value at the AC coupling of TCXO parts and the CLKI pin by the capacity of 1000pF.



- At the items of CLKI amplitude H/L, its spec differs with CLKI frequency.
- The voltage level which Duty of CLKI becomes 50% (High time = Low time) is defined as Vcenter.
- The measurement point of Trckt and Tfckt differs with CLKI frequency.
  1.5MHz ≤ CLKI frequency ≤ 20MHz: it is defined by a time change of Vcenter+0.3[V] and Vcenter-0.3[V].
  20MHz < CLKI frequency ≤ 27MHz: it is defined by a time change of Vcenter+0.45[V] and Vcenter-0.45[V]
- The timing observation level of Tfreq is to be Vcenter (Duty=50%).

CPU interface timing

The AC characteristics of a CPU interface are measured on condition as follows.

The input conditions at the time of measurement : V_{IH} = 0.8×IOVDD, V_{IL}=0.2×IOVDD

The measurement points : V_{IH} = 0.65×IOVDD, V_{IL}=0.35×IOVDD

V_{OH} = 0.65×IOVDD, V_{OL}=0.35×IOVDD

● CPU interface 1 (In the case of IOVDD≧2.65V)

(Write cycle)

Item	Symbol	Min	Max.	Unit
Address setup time	T_{ADS}	50		ns
Address hold time	T_{ADH}	0		ns
Chip select setup time	T_{CSS}	50		ns
Chip select hold time	T_{CSH}	0		ns
Write pulse width	T_{WW}	50		ns
Data setup time	T_{WDS}	30		ns
Data hold time	T_{WDH}	0		ns

[Condition] T_{OP}=-20 ~ 85°C, VDD=IOVDD=2.65 ~ 3.30V, Capacitor load=50 pF

(Read cycle)

Item	Symbol	Min	Max.	Unit
Access time from /RD pin	T_{ACCRD}		70	ns
Access time from /CS pin	T_{ACCCS}		70	ns
Access time from /A0 pin	T_{ACCA0}		70	ns
Data hold time from /RD pin	T_{DHRD}	0		ns
Data hold time from /CS pin	T_{DHCS}	0		ns
Data hold time from A0 pin	T_{DHA0}	0		ns
High-impedance transition time from /RD pin	T_{DZRD}		30	ns
High-impedance transition time from /CS pin	T_{DZCS}		30	ns

[Condition] T_{OP}=-20 ~ 85°C, VDD=IOVDD=2.65 ~ 3.30V, Capacitor load=50 pF

I_{OH}= -1.0mA, I_{OL}= +1.0mA (D0 ~ D7 pin)

● CPU interface 2 (In the case of IOVDD < 2.65V)

(Write cycle)

Item	Symbol	Min	Max.	Unit
Address setup time	T_{ADS}	50		ns
Address hold time	T_{ADH}	0		ns
Chip select setup time	T_{CSS}	50		ns
Chip select hold time	T_{CSH}	0		ns
Write pulse width	T_{WW}	50		ns
Data setup time	T_{WDS}	50		ns
Data hold time	T_{WDH}	0		ns

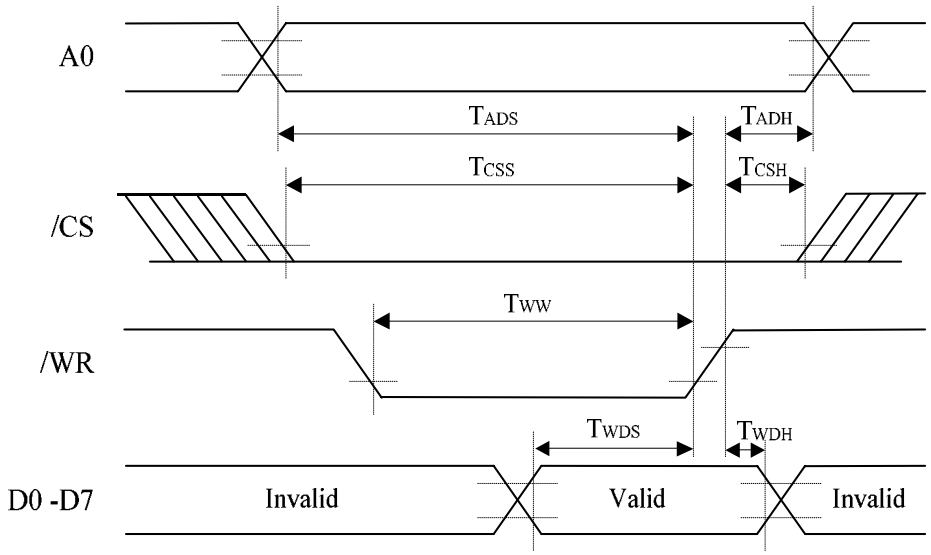
[Condition] T_{OP}=-20 ~ 85°C, VDD=2.65 ~ 3.30V, IOVDD=1.65 ~ less than 2.65V, Capacitor load=30 pF

(Read cycle)

Item	Symbol	Min	Max.	Unit
Access time from /RD pin	T_{ACCRD}		80	ns
Access time from /CS pin	T_{ACCCS}		80	ns
Access time from /A0 pin	T_{ACCA0}		80	ns
Data hold time from /RD pin	T_{DHRD}	0		ns
Data hold time from /CS pin	T_{DHCS}	0		ns
Data hold time from A0 pin	T_{DHA0}	0		ns
High-impedance transition time from /RD pin	T_{DZRD}		50	ns
High-impedance transition time from /CS pin	T_{DZCS}		50	ns

[Condition] T_{OP}=-20 ~ 85°C, VDD=2.65 ~ 3.30V, IOVDD=1.65 ~ less than 2.65V, Capacitor load=30 pF
I_{OH}= -0.2mA, I_{OL}= +0.2mA (D0 ~ D7 pin)

Write cycle



Note :

T_{ADH} : The hold time of A0 pin, which is defined with respect to the point where the rise of /WR has reached 0.65*IOVDD under the condition that both two specifications (T_{CSH} , T_{WDH}) are secured more than minimum value (=0ns).

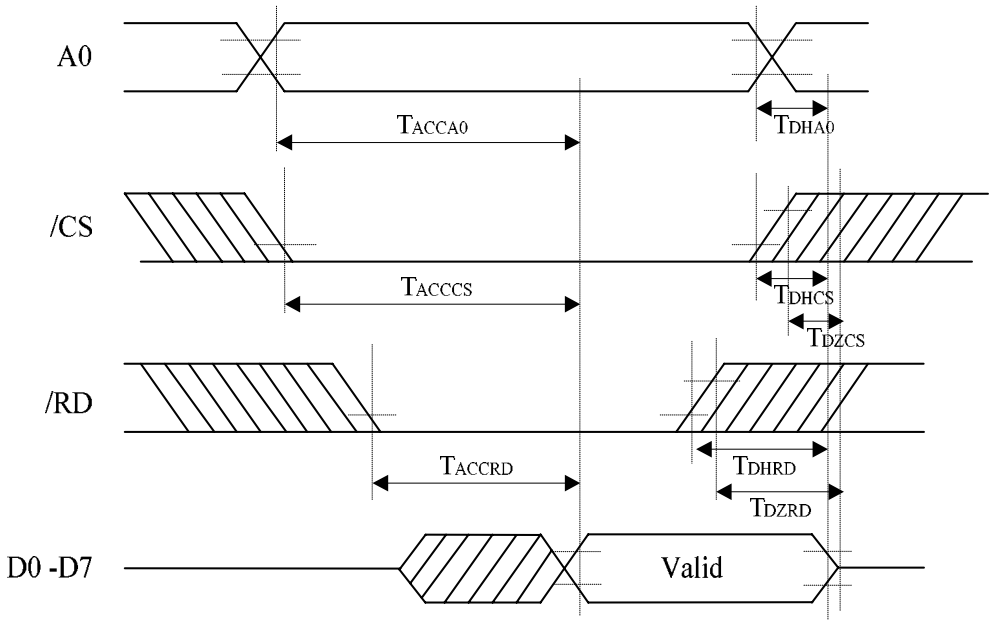
T_{CSH} : The hold time of /CS pin, which is defined with respect to the point where the rise of /WR has reached 0.65*IOVDD under the condition that both two specifications (T_{ADH} , T_{WDH}) are secured more than minimum value (=0ns).

T_{WDH} : The hold time of D0 ~ D7 pins, which is defined with respect to the point where the rise of /WR has reached 0.65*IOVDD under the condition that both two specifications (T_{ADH} , T_{CSH}) are secured more than minimum value (=0ns).

T_{ADS} : The hold time of A0 pin, which is defined with respect to the point where /WR has become invalid (0.35*IOVDD) under the condition that all of three specifications (T_{CSS}, T_{WW}, T_{WDS}) are secured more than minimum value.

T_{CSS} : The hold time of /CS pin, which is defined with respect to the point where /WR has become invalid (0.35*IOVDD) under the condition that all of three specifications (T_{ADS}, T_{WW}, T_{WDS}) are secured more than minimum value.

Read cycle



Note :

T_{ACCA0} : The access time until D0 ~ D7 are defined (0.65*IOVDD or 0.35*IOVDD) after A0 is defined (0.65*IOVDD or 0.35*IOVDD).
Considers that /RD and /CS are defined beforehand (*1).

T_{ACCCS} : The access time until D0 ~ D7 are defined (0.65*IOVDD or 0.35*IOVDD) after /CS is defined (0.35*IOVDD).
Considers that A0 and /RD are defined beforehand (*1).

T_{ACCRD} : The access time until D0 ~ D7 are defined (0.65*IOVDD or 0.35*IOVDD) after /RD is defined (0.35*IOVDD).
Considers that A0 and /CS are defined beforehand (*1).

T_{DHRD} : The time (Hold time) until D0 ~ D7 continue to output valid data after the timing (=0.35*IOVDD) /RD becomes disable from enable under the condition that A0 and /CS secure sufficient hold time (*2).

T_{DHCS} : The time (Hold time) until D0 ~ D7 continue to output valid data after the timing (=0.35*IOVDD) /CS becomes disable from enable under the condition that A0 and /RD secure sufficient hold time (*2).

T_{DHA0} : The time (Hold time) until D0 ~ D7 continue to output valid data after the timing (=0.65*IOVDD or 0.35*IOVDD) A0 becomes disable from enable under the condition that /RD and /CS secure sufficient hold time (*2).

T_{DZRD} : The time until D0 ~ D7 become high impedance status after /RD becomes disable (=0.65*IOVDD) under the condition that A0 and /CS secure sufficient hold time (*2).

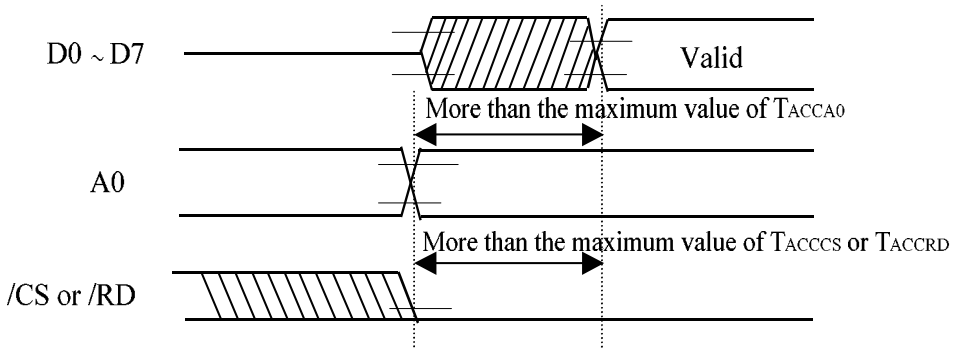
T_{DZCS} : The time until D0 ~ D7 become high impedance status after /CS becomes disable (=0.65*IOVDD) under the condition that A0 and /RD secure sufficient hold time (*2).

(*1) "~ defined beforehand." means,

In the case of /CS : The status that /CS is defined (0.35*IOVDD) before more than the time of T_{ACCCS} with respect to the point where D0 ~ D7 are defined (0.65*IOVDD or 0.35*IOVDD).

In the case of /RD : The status that /RD is defined (0.35*IOVDD) before more than the time of T_{ACCRD} with respect to the point where D0 ~ D7 are defined (0.65*IOVDD or 0.35*IOVDD).

In the case of A0 : The status that A0 is defined (0.35*IOVDD or 0.65*IOVDD) before more than the time of T_{ACCA0} with respect to the point where D0 ~ D7 are defined (0.65*IOVDD or 0.35*IOVDD).



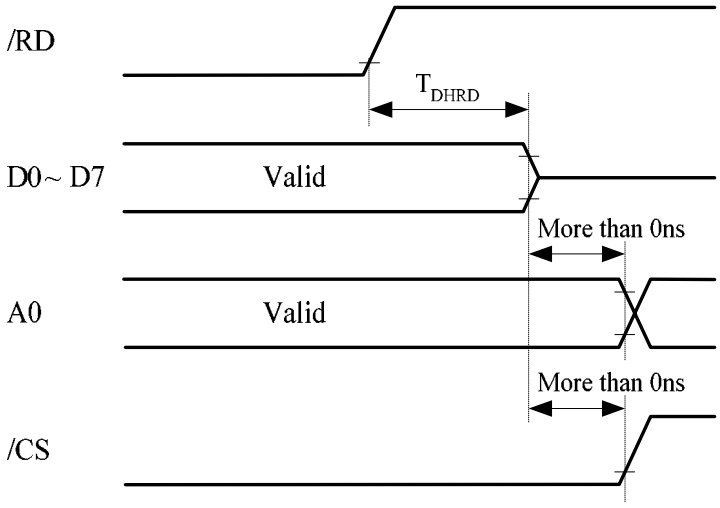
(*2) "~ sufficient hold time" means,

At T_{DHRD} measurement: The status that the enable time of A0 and /CS pins input are secured more than 0ns with respect to the point where D0 ~ D7 can not hold valid data.

At T_{DHCS} measurement: The status that the enable time of A0 and /RD pins input are secured more than 0ns with respect to the point where D0 ~ D7 can not hold valid data.

AT T_{DHA0} measurement: The status that the enable time of /CS and /RD pins input are secured more than 0ns with respect to the point where D0 ~ D7 can not hold valid data.

(Example: At T_{DHRD} measurement)



■ Analog characteristics

Conditions of T_{OP}=25°C, VDD=3.00V, IOVDD=1.80V, and SPVDD=3.60V apply to all items.

○ SP amplifier

Item	Min.	Typical	Max.	Unit
Gain setting (fixed)		±2		times
Min. load resistance (RL)		8		Ω
Max. output voltage amplitude (RL=8Ω)		6.0		Vp-p
Max. output power (RL=8Ω, THD+N≤1.0%)		580		mW
THD + N (RL=8Ω, f=1 kHz, output = 400mW)		0.025		%
Noise at no signal (A-filter: weighting filter)		-90		dBV
PSRR (f=1 kHz)		90		dB
Amplitude center potential (VSEL2, VSEL1 =0, 0)		0.6×VDD		V
(VSEL2, VSEL1 =0, 1)		0.5×VDD		V
(VSEL2, VSEL1 =1, 0)		0.67×VDD		V
Differential output voltage		10	50	mV
Max. load capacity connectable to SPOUT1 and SPOUT2 pin (*)			1000	pF

(*) : The maximum of 1000pF can be connected to SPOUT1 pin, and the maximum of 1000pF can be connected to SPOUT2 pin.

○ EQ amplifier

Item	Min.	Typical	Max.	Unit
Gain settable range			30	dB
Max. output voltage amplitude		2.7		Vp-p
THD + N (f=1 kHz)			0.05	%
Noise at no signal (A-filter)		-90		dBV
Input impedance	10			MΩ
Feedback resistance between EQ2 and EQ3	20			kΩ

○ SP Volume

Item	Min.	Typical	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
THD + N (f=1 kHz)			0.05	%

○ EQ Volume

Item	Min.	Typical	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise at no signal (A-filter)		-90		dBV
Max. output current	120			μA
Max. output voltage amplitude		1.5		Vp-p
Output impedance		300	600	Ω

○ HP Volume

Item	Min.	Typical	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise at no signal (A-filter)		-90		dBV
Max. output current	120			μA
Max. output voltage amplitude		1.5		Vp-p
Output impedance		300	600	Ω

○ VREF

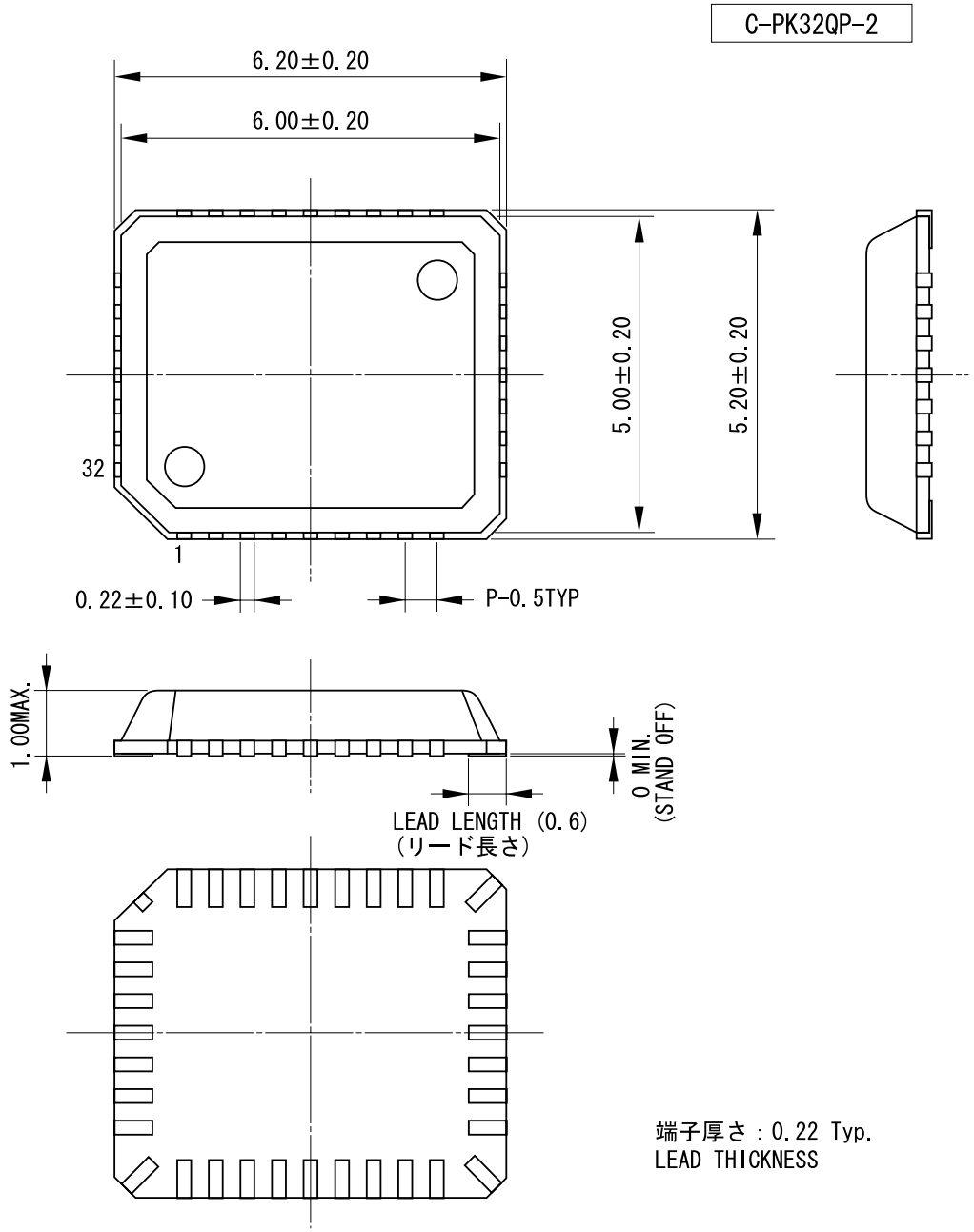
Item	Min.	Typical	Max.	Unit
VREF voltage		0.5×VDD		V

○ DAC

Item	Min.	Typical	Max.	Unit
Resolution		16		Bit
Full scale output voltage		1.5		Vp-p
THD+N (f= 1 kHz)			0.5	%
Noise at no signal (A-filter)		-85	-80	dBV
Frequency response (f=50Hz to 20 kHz)	-3.0 (*)		+0.5	dB

(*): Reduction of response in high frequency range caused by aperture effect

External dimensions of package



モールドコーナー形状は、この図面と若干異なるタイプのものもあります。
カッコ内の寸法値は参考値とする。
モールド外形寸法はバリを含まない。
単位(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.
The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

注) 表面実装LSIは保管条件及び、半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせ下さい。
Note: The LSIs for surface mount need special consideration on storage and soldering conditions.
For detailed information, Please contact your nearest Yamaha agent.

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AGENCY

YAMAHA CORPORATION

Address inquiries to:
Semiconductor Sales & Marketing Department

■ Head Office 203, Matsunokijima, Toyooka-mura
Iwata-gun, Shizuoka-ken, 438-0192, Japan
Tel. +81-539-62-4918 Fax. +81-539-62-5054

■ Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8568, Japan
Tel. +81-3-5488-5431 Fax. +81-3-5488-5088

■ Osaka Office 3-12-12, Minami Senba, Chuo-ku,
Osaka City, Osaka, 542-0081, Japan
Tel. +81-6-6252-6221 Fax. +81-6-6252-6229

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