MSM514402B/BL

1,048,576-Word × 4-Bit DYNAMIC RAM : STATIC COLUMN MODE TYPE

DESCRIPTION

The MSM514402B/BL is a new generation dynamic RAM organized as 1,048,576-word × 4-bit. The technology used to fabricate the MSM514402B/BL is OKI's CMOS silicon gate process technology. The device operates at a single 5V power supply. Its I/O pins are TTL compatible.

FEATURES

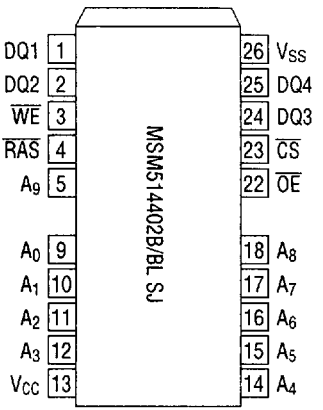
- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 1,048,576-word × 4-bit organization
- Single 5V power supply, ±10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate
- Refresh: 1024 cycles/16ms, 1024 cycles/128ms (L-version)
- $\overline{CS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$-only refresh capability
- Multibit test mode capability
- Package:

26-Pin 300mil	Plastic SOJ	(SOJ26-P-300)
20-Pin 400mil	Plastic ZIP	(ZIP20-P-400-W1)
26-Pin 300mil	Plastic TSOP	(TSOP26-P-300-K/L)

PRODUCT FAMILY

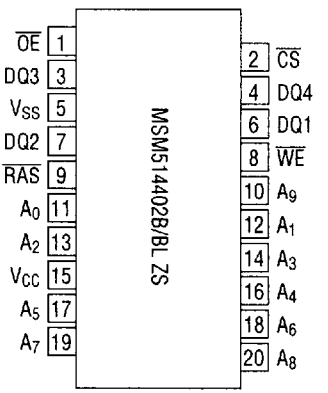
Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM514402B/BL-60	60ns	30ns	15ns	15ns	110ns	550mW	5.5mW/ 1.1mW (L-version)
MSM514402B/BL-70	70ns	35ns	20ns	20ns	130ns	495mW	
MSM514402B/BL-80	80ns	40ns	20ns	20ns	150ns	440mW	
MSM514402B/BL-10	100ns	50ns	25ns	25ns	180ns	385mW	

PIN CONFIGURATION (TOP VIEW)

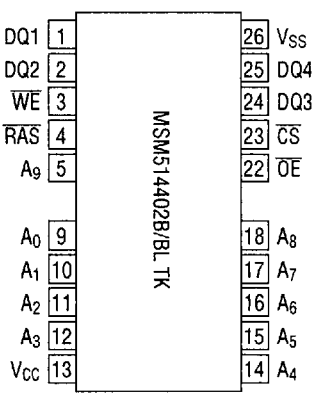


26-PIN SOJ

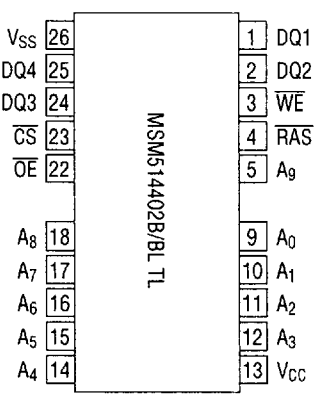
SJ=300mil



20-PIN ZIP



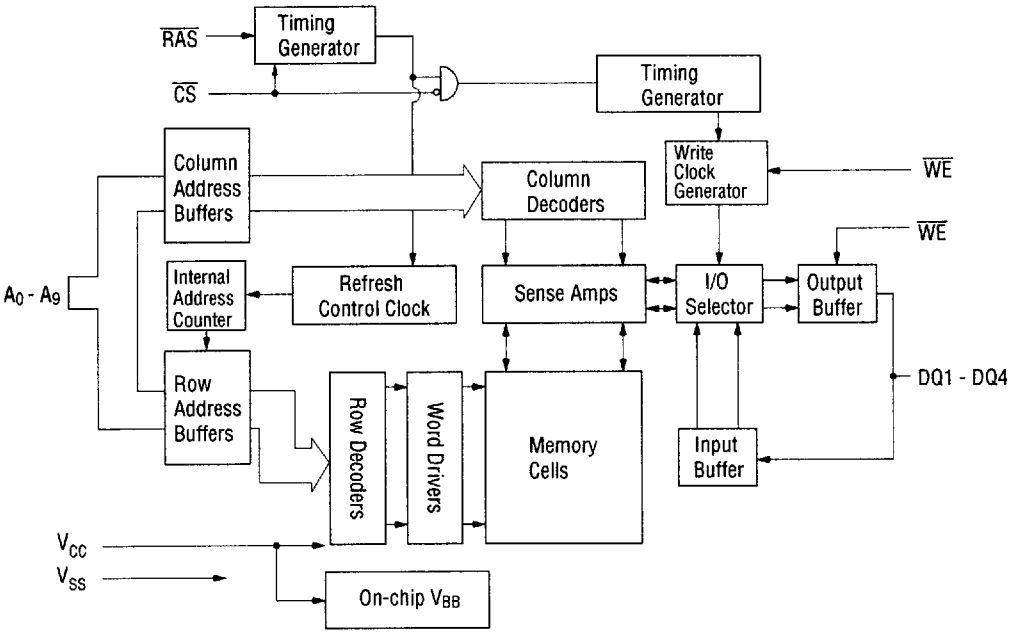
26-PIN TSOP
(K TYPE)



26-PIN TSOP
(L TYPE)

Pin Name	Function
A_0 - A_9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
DQ1 - DQ4	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (5V)
V_{SS}	Ground (0V)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	−55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

Capacitance

(V_{CC} = 5V ± 10%, Ta = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 - A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ4)	$C_{I/O}$	—	7	pF

DC Characteristics

(V_{CC} = 5 V ± 10%, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MSM514402B/BL-60		MSM514402B/BL-70		MSM514402B/BL-80		MSM514402B/BL-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = −5.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V ≤ V_I ≤ 6.5V; All Other Pins not Under test = 0V	−10	10	−10	10	−10	10	−10	10	µA	
Output Leakage Current	I_{LO}	DQ_i Disable 0V ≤ V_O ≤ 5.5 V	−10	10	−10	10	−10	10	−10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ Cycling, t_{RC} = Min.	—	100	—	90	—	80	—	70	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CS}$ = V_{IH}	—	2	—	2	—	2	—	2	mA	1
		$\overline{RAS}$, $\overline{CS}$ ≥ V_{CC} − 0.2V	—	1	—	1	—	1	—	1		
			—	200	—	200	—	200	—	200	µA	1, 4
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CS}$ = V_{IH} t_{RC} = Min.	—	100	—	90	—	80	—	70	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH} $\overline{CS}$ = V_{IL} DQi = Enable	—	5	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{CS}$ Before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ Cycling $\overline{CS}$ Before $\overline{RAS}$	—	100	—	90	—	80	—	70	mA	1, 2
Average Power Supply Current (Static Column Mode)	I_{CC9}	$\overline{RAS}$ = V_{IL}, Address Cycling, t_{SC} = Min.	—	90	—	80	—	70	—	60	mA	1
Average Power Supply Current (Battery Backup)	I_{CC10}	t_{RC} = 125 µs $\overline{CS}$ Before $\overline{RAS}$ $\overline{RAS}$ Cycling t_{RAS} ≤ 1µs	—	300	—	300	—	300	—	300	µA	1, 2, 3, 4

Notes : 1. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V, −1.0V ≤ V_{IL} ≤ 0.2V.

AC Characteristics (1/2)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 3, 12, 13

Parameter	Symbol	MSM514402B/BL-60		MSM514402B/BL-70		MSM514402B/BL-80		MSM514402B/BL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
Read Modify Write Cycle Time	t_{RMW}	150	—	180	—	200	—	240	—	ns	
Static Column Mode Cycle Time	t_{SC}	35	—	40	—	45	—	55	—	ns	
Static Column Mode Read Modify Write Cycle Time	t_{SRMW}	80	—	95	—	105	—	130	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	4, 5, 6
Access Time from $\overline{CS}$	t_{CAC}	—	15	—	20	—	20	—	25	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	35	—	40	—	50	ns	4, 6, 7
Access Time from Last Write	t_{ALW}	—	55	—	65	—	75	—	95	ns	4, 7
Access Time from $\overline{OE}$	t_{OEA}	—	15	—	20	—	20	—	25	ns	4
Data Output Enable Time Reference to $\overline{WE}$	t_{OW}	—	20	—	20	—	20	—	25	ns	4
Output Low Impedance Time from $\overline{CS}$	t_{CLZ}	0	—	0	—	0	—	0	—	ns	
Data Output Hold Time Reference to Column Address	t_{AOH}	5	—	5	—	5	—	5	—	ns	
Output Buffer Turn-off Delay Time	t_{OFF}	0	15	0	20	0	20	0	25	ns	8
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	15	0	20	0	20	0	25	ns	8
Transition Time	t_T	3	50	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	
Refresh Period (L-version)	t_{REF}	—	128	—	128	—	128	—	128	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Static Column Mode)	t_{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	t_{ROH}	15	—	20	—	20	—	25	—	ns	
$\overline{CS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CS}$ Pulse Width	t_{CS}	15	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	50	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 3, 12, 13

Parameter	Symbol	MSM514402B/BL-60		MSM514402B/BL-70		MSM514402B/BL-80		MSM514402B/BL-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Column Address Hold Time Reference to $\overline{RAS}$ (Write Cycle)	t_{AWR}	50	—	55	—	60	—	75	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	75	—	85	—	95	—	115	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	50	—	ns	
Column Address Hold Time Reference to $\overline{RAS}$ Precharge	t_{AH}	10	—	10	—	10	—	10	—	ns	
Column Address Hold Time Reference to $\overline{WE}$	t_{AHLW}	55	—	65	—	75	—	95	—	ns	
Last Write to Column Address Delay Time	t_{LWAD}	20	25	20	30	20	35	25	45	ns	7
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	0	—	ns	9
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	10	—	10	—	10	—	15	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	15	—	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	15	—	20	—	20	—	25	—	ns	
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	45	—	50	—	60	—	75	—	ns	
Write Invalid Time	t_{WI}	10	—	10	—	10	—	10	—	ns	
Write Command Hold Time (D_{OUT} Disable)	t_{WH}	0	—	0	—	0	—	0	—	ns	10
Write Command to $\overline{CS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	ns	
$\overline{CS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	45	—	45	—	55	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	60	—	65	—	80	—	ns	10
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	95	—	105	—	130	—	ns	10
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	ns	11
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	50	—	55	—	60	—	75	—	ns	
$\overline{OE}$ to Data-in Delay Time	t_{OED}	15	—	20	—	20	—	25	—	ns	
$\overline{CS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	5	—	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CS}$ Set-up Time ($\overline{CS}$ Before $\overline{RAS}$)	t_{CSR}	5	—	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CS}$ Hold Time ($\overline{CS}$ Before $\overline{RAS}$)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{CS}$ Precharge Time (Refresh Counter Test)	t_{CPT}	30	—	35	—	40	—	50	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CS}$ Before $\overline{RAS}$)	t_{WRP}	10	—	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CS}$ Before $\overline{RAS}$)	t_{WRH}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode)	t_{WSR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode)	t_{WHR}	10	—	10	—	10	—	10	—	ns	

Notes:

1. An initial pause of 200μs is required after power-up followed by eight or more initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is achieved. In case of using internal refresh counter, eight or more $\overline{CS}$ before $\overline{RAS}$ initialization cycles is required.

2. The AC measurements assume $t_T = 5$ ns.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels of input signals for timing measurement. Transition times are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

5. Operating within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{AA}.

6. Operating within the t_{RAD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, the access time is controlled exclusively by t_{AA}.

7. Operating within the t_{LWAD} (Max.) limit insures that t_{ALW} (Max.) can be met. t_{LWAD} (Max.) is specified as a reference point only. If t_{LWAD} is greater than the specified t_{LWAD} (Max.) limit, the access time is controlled exclusively by t_{AA}.

8. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

9. Either the t_{RRH} of t_{RCH} must be satisfied for a read cycle.

10. t_{WCS}, t_{WH}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; If $t_{WCS} \geq t_{WCS}$ (Min.) and $t_{WH} \geq t_{WH}$ (Min.) the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (Min.), tRWD ≥ tRWD (Min.) and tAWD ≥ tAWD (Min.), the cycle is read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

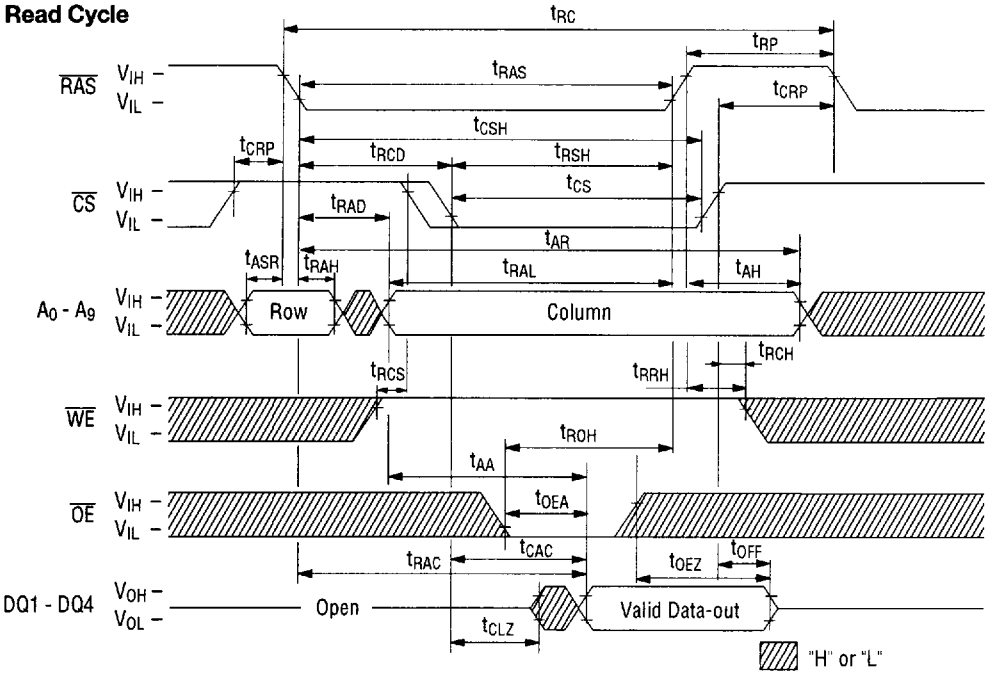
11. These parameters are referenced to $\overline{CS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a $\overline{OE}$ control write cycle or a read modify write cycle.

12. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remain in effect until the exit cycle is generated. In a test mode CA0 is not used and each I/O pin now accesses 2 bit locations.
    Since all 4 I/O pins are used, a total of 8 data bits can be written in parallel into the memory array. In a read cycle, if 2 data bits are equal, the I/O pin will indicate a high level.
    If the 2 data bits are not equal, the I/O pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$ only refresh cycle or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle.

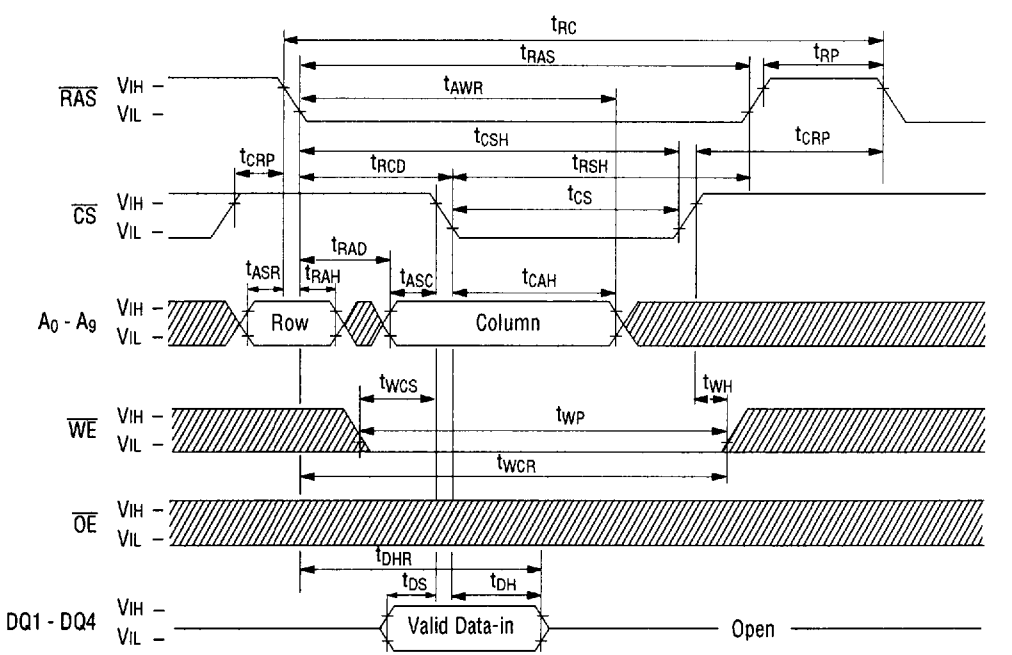
13. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

TIMING WAVEFORM

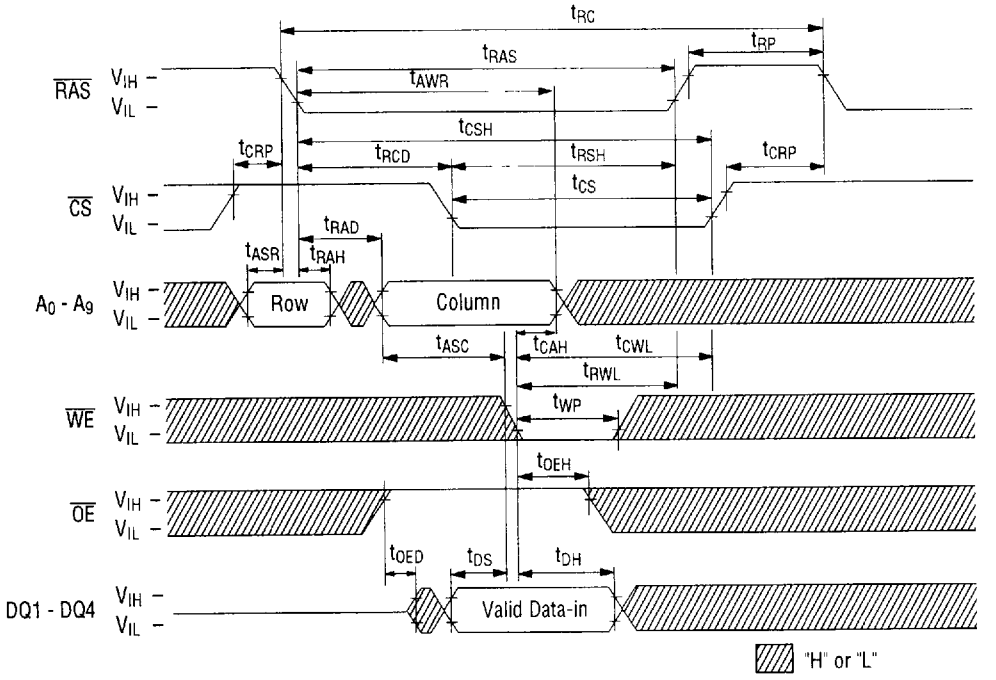
Read Cycle



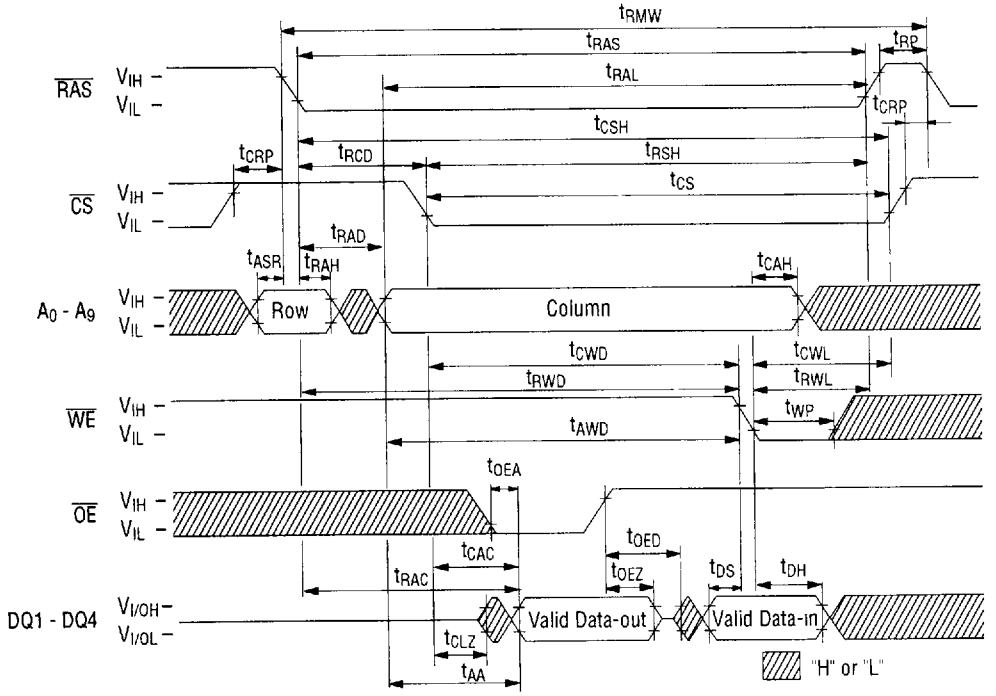
Write Cycle (Early Write)



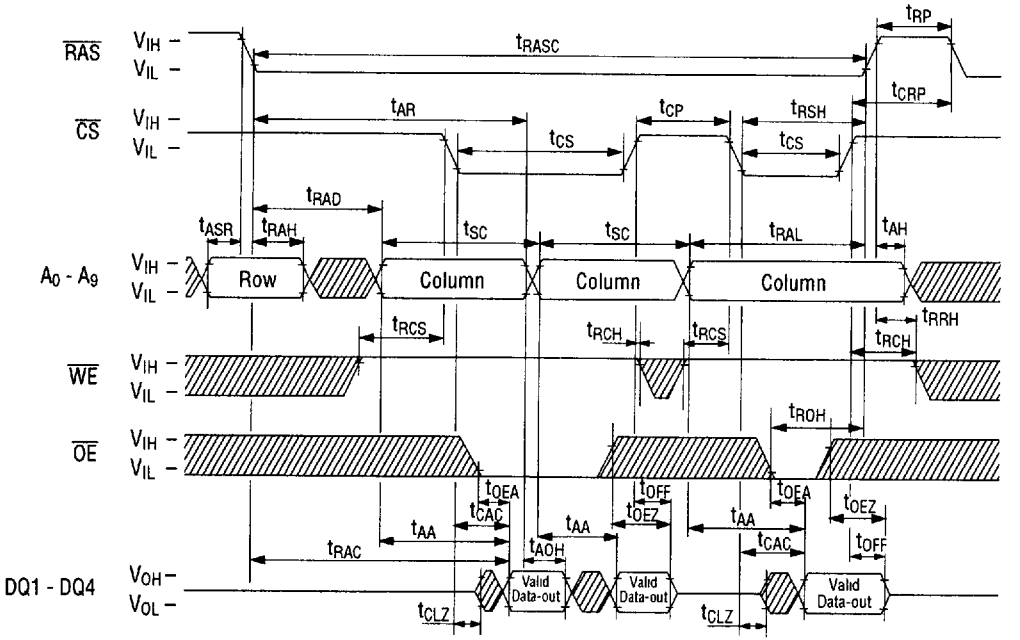
Write Cycle ($\overline{OE}$ Control Write)



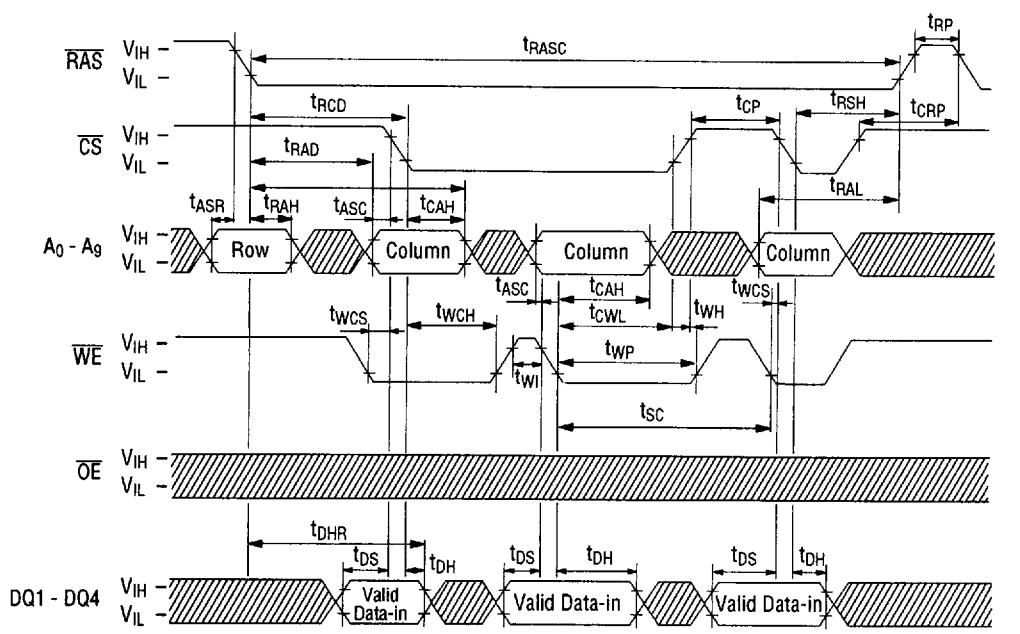
Read Modify Write Cycle



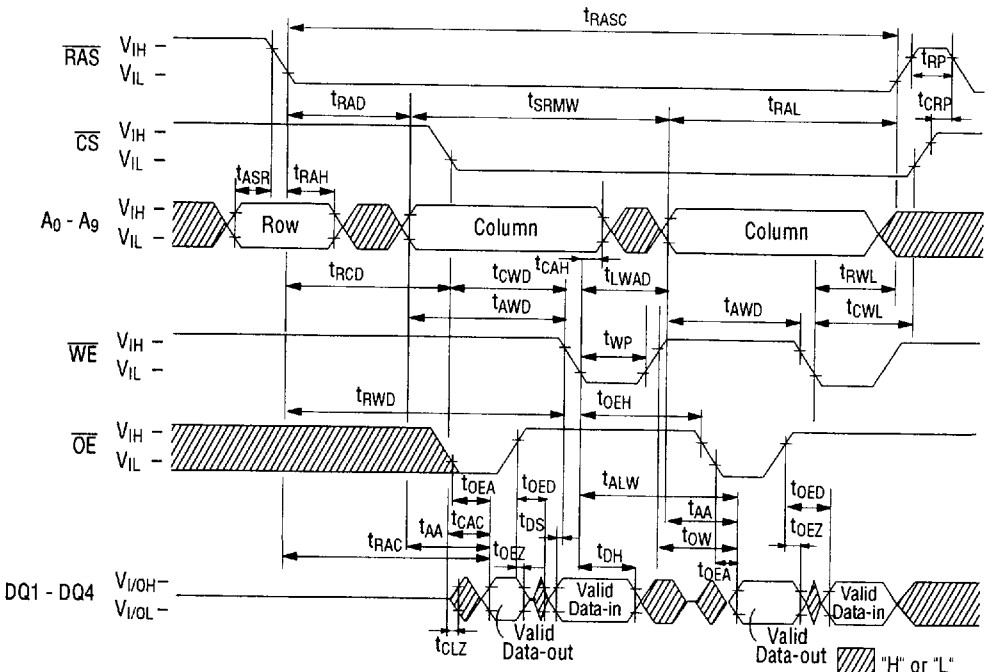
Static Column Mode Read Cycle



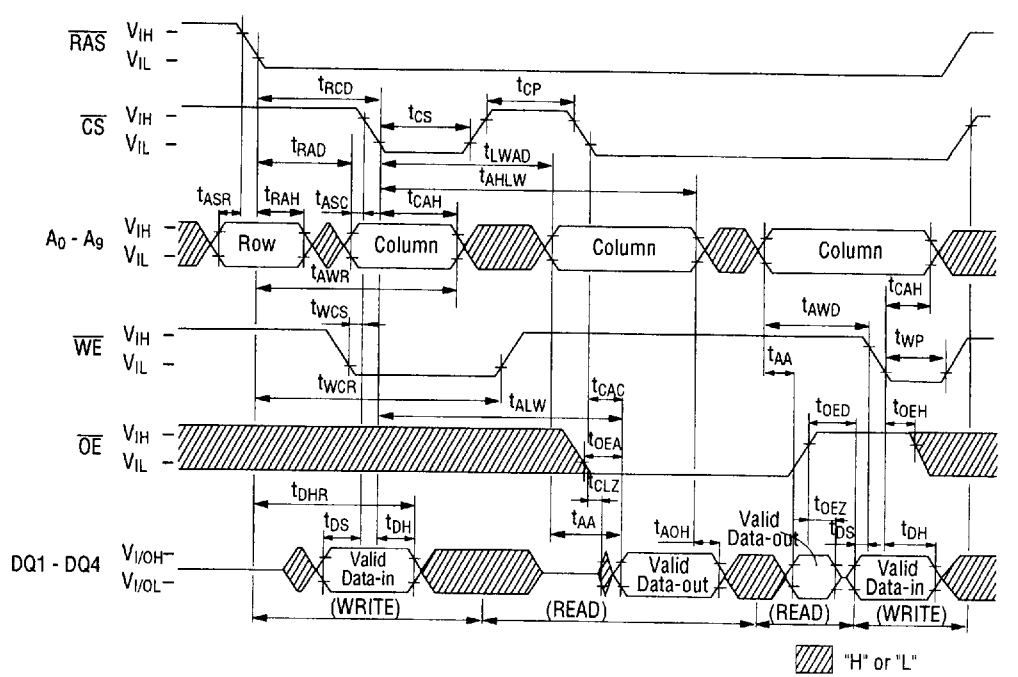
Static Column Mode Write Cycle (Early Write)



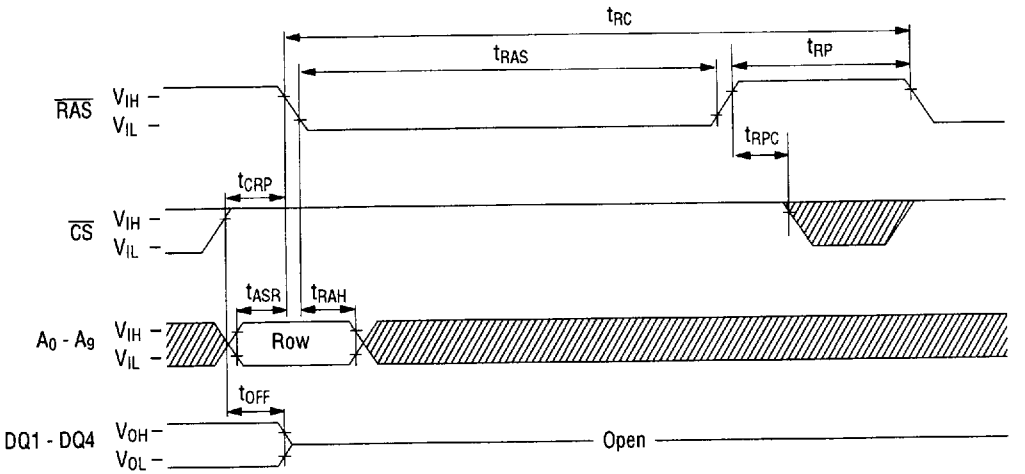
Static Column Mode Read Modify Write Cycle



Static Column Mode Read/Write Mixed Cycle

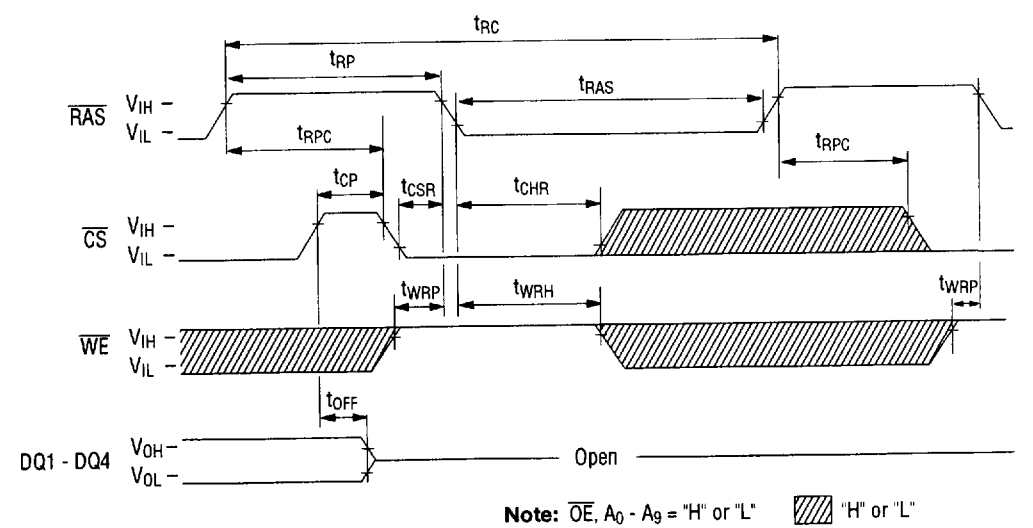


$\overline{RAS}$-only Refresh Cycle



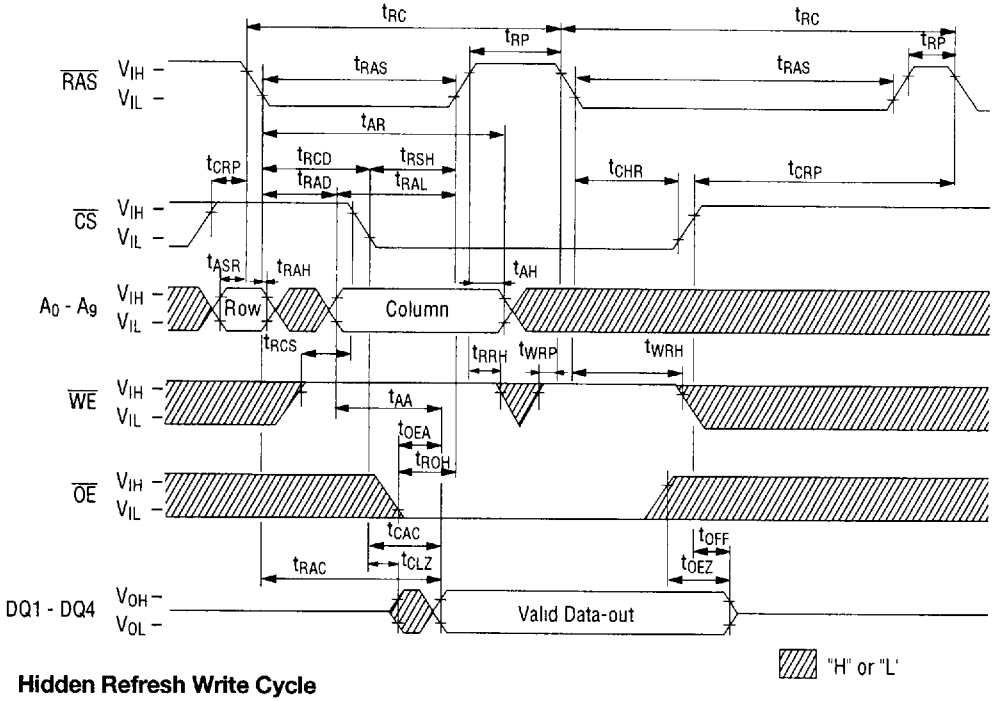
Note: $\overline{WE}$, $\overline{OE}$ = "H" or "L" "H" or "L"

$\overline{CS}$ Before $\overline{RAS}$ Auto-refresh Cycle

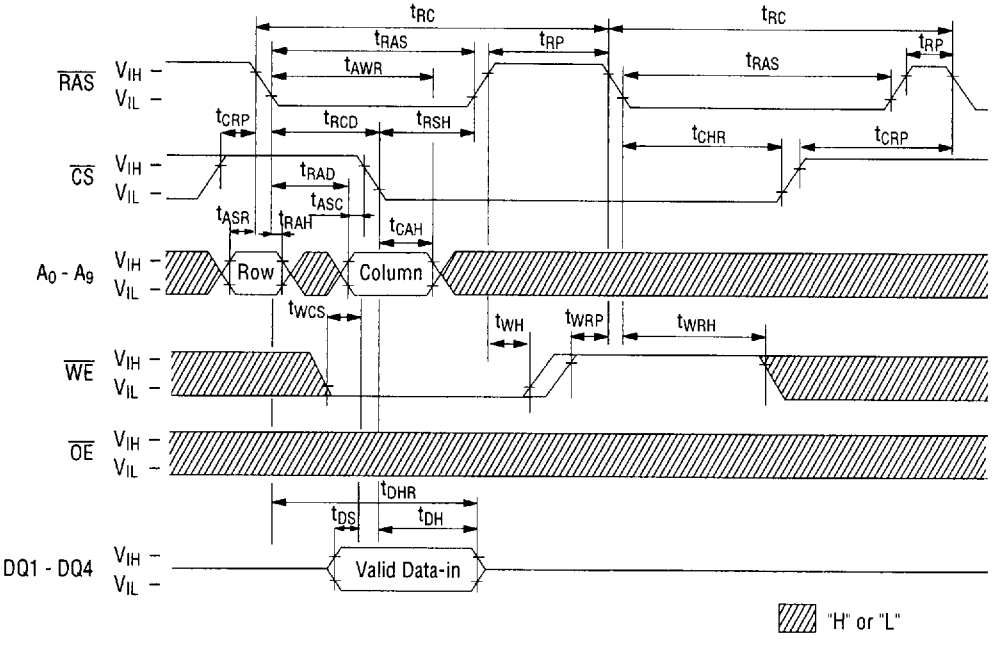


Note: $\overline{OE}$, A_0 - A_9 = "H" or "L" "H" or "L"

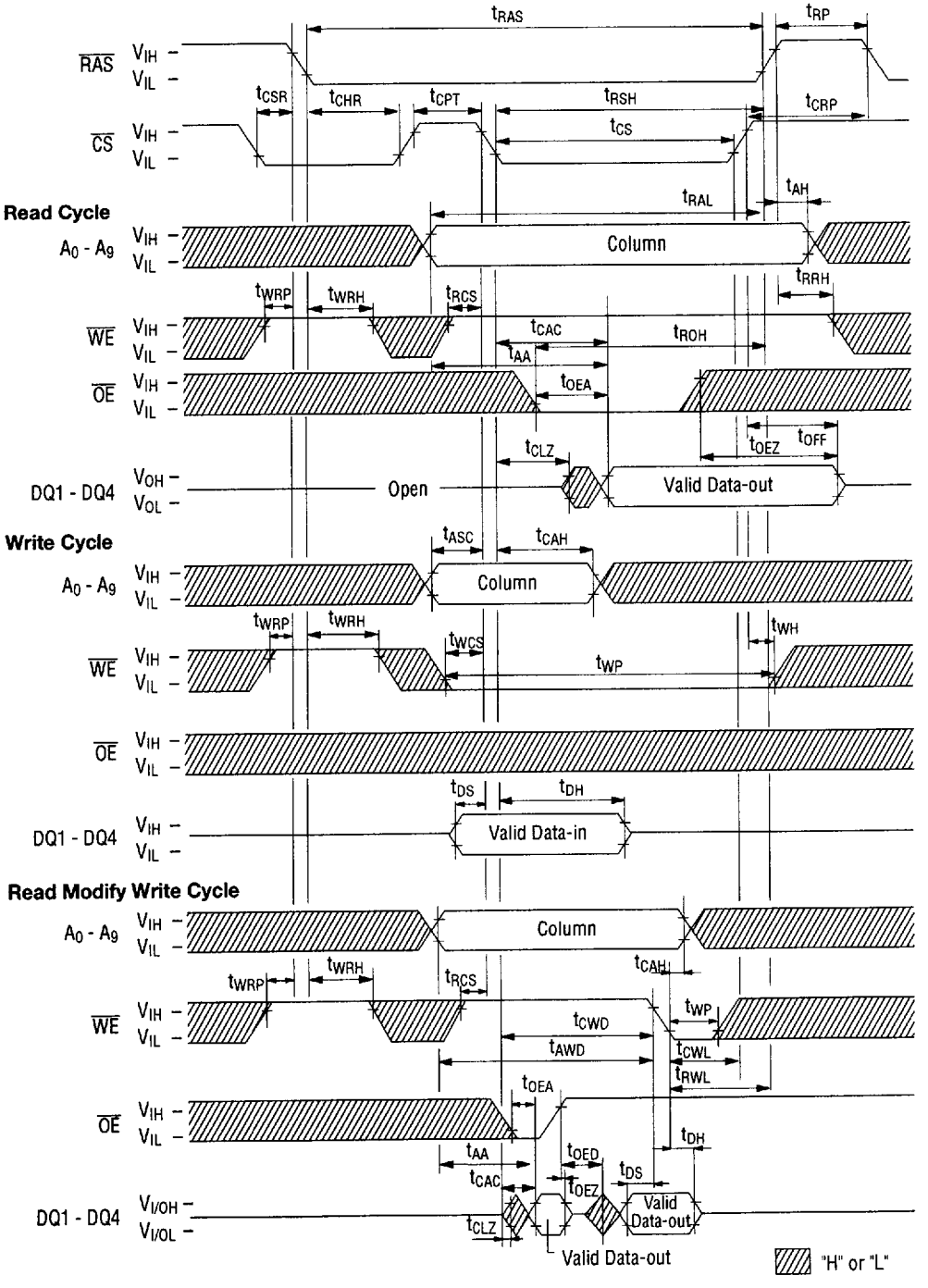
Hidden Refresh Read Cycle



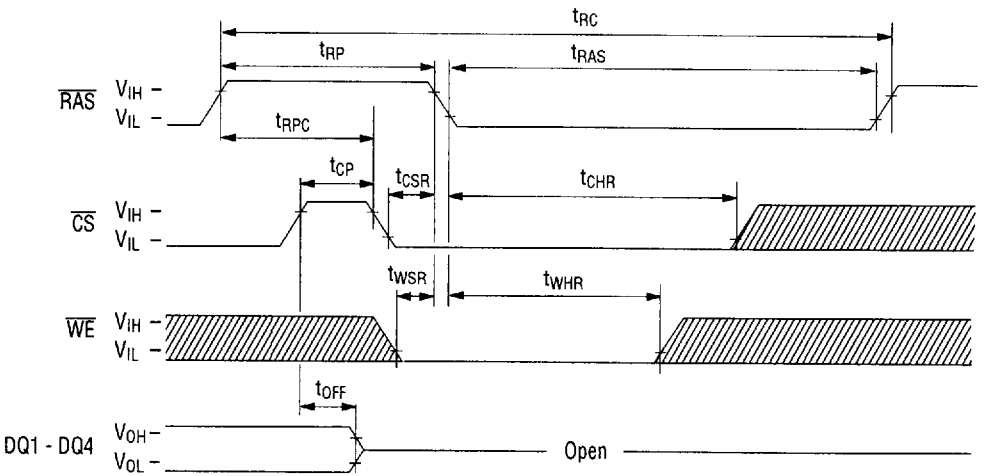
Hidden Refresh Write Cycle



$\overline{CS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle



Test Mode Intiate Cycle



Note: $\overline{OE}$, A_0 - A_9 = "H" or "L" "H" or "L"