

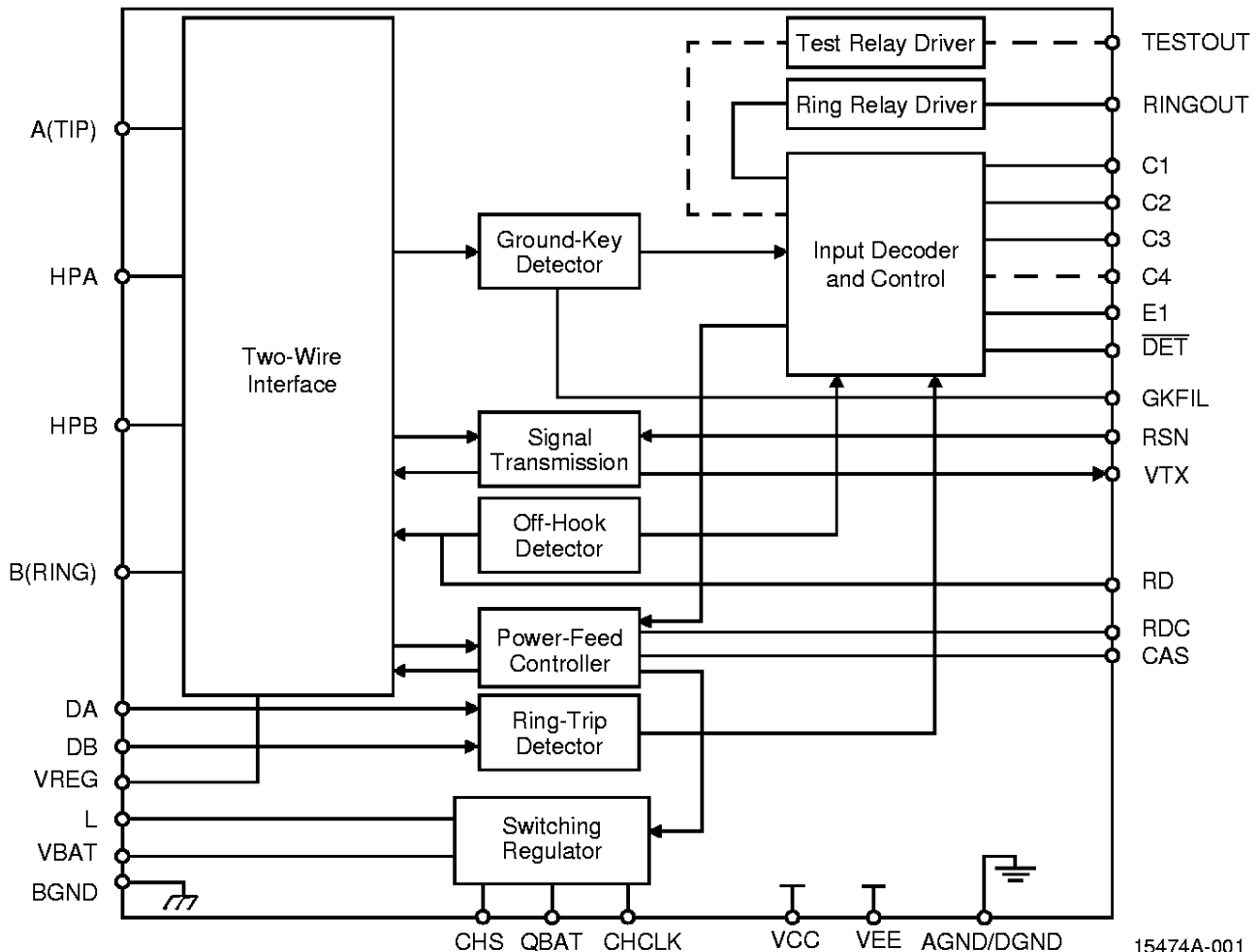
# Am7942

## Subscriber Line Interface Circuit

### DISTINCTIVE CHARACTERISTICS

- Programmable constant-current feed
- Receive current gain = 200
- Programmable loop-detect threshold
- Low standby power
- Performs polarity reversal
- Ground-key detector
- Pin for external ground-key noise filter capacitor
- Test relay driver option (PLCC only)
- Tip Open state for ground-start lines
- -19 V to -58 V battery operation
- Ideal for PBX and KTS applications
- On-chip switching regulator for low-power dissipation
- Can be used with or without the on-chip switching regulator
- Two-wire impedance set by single external impedance
- On-hook transmission

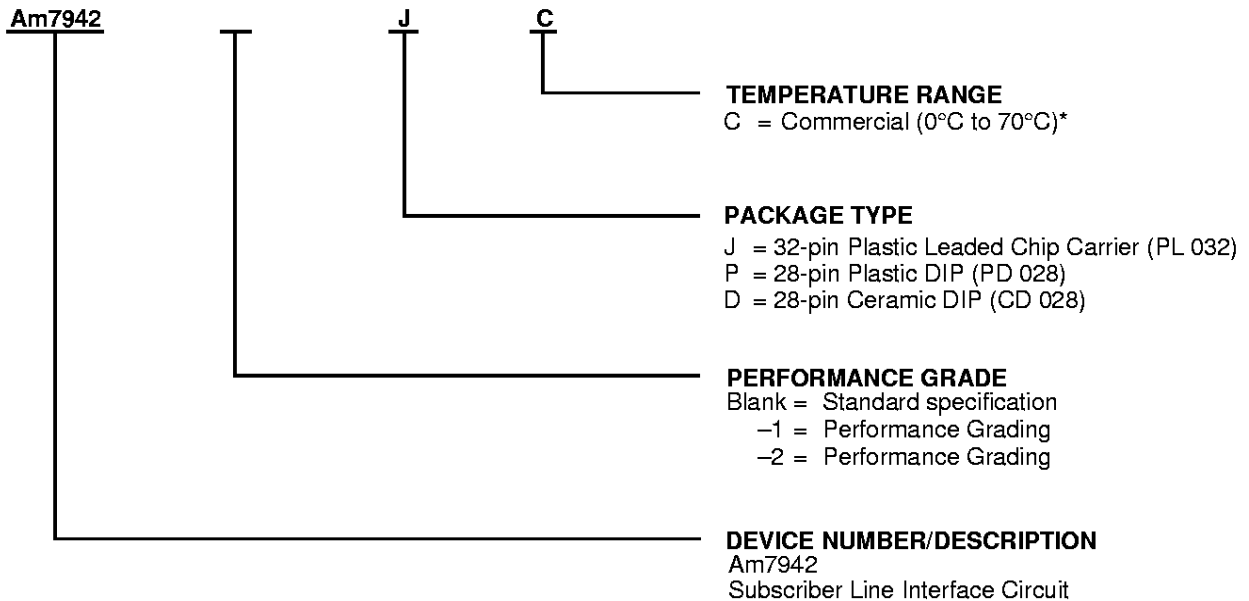
### BLOCK DIAGRAM



**ORDERING INFORMATION**

**Standard Products**

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



| Valid Combinations |    |    |
|--------------------|----|----|
| Am7942             | -1 | DC |
|                    | -2 | JC |
|                    |    | PC |

**Valid Combinations**

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD standard military grade products.

**Note:**

\* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from -40°C to +85°C is guaranteed by characterization and periodic sampling of production units.



## PIN DESCRIPTIONS

| Pin Names | Type                   | Description   |
|-----------|------------------------|---|
| AGND/DGND | Gnd                    | Analog and Digital ground.  |
| A(TIP)    | Output                 | Output of A(TIP) power amplifier.   |
| BGND      | Gnd                    | Battery (power) ground.   |
| B(RING)   | Output                 | Output of B(RING) power amplifier.  |
| C3–C1     | Input                  | Decoder. TTL compatible. C3 is MSB and C1 is LSB.   |
| C4        | Input                  | Test Relay Driver Command. TTL compatible. A logic Low enables the driver. See Note 3.  |
| CAS       | Capacitor              | Anti-saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.   |
| CHCLK     | Input                  | Chopper Clock. Input to switching regulator (TTL compatible). Freq = 256 kHz (typ). See Note 1.   |
| CHS       | Input                  | Chopper Stabilization. (See Note 1) Connection for external chopper stabilizing components.   |
| DA        | Input                  | Ring-trip negative. Negative input to ring-trip comparator.   |
| DB        | Input                  | Ring-trip positive. Positive input to ring-trip comparator.   |
| DET       | Output                 | Switchhook detector. When enabled, a logic Low indicates the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E1). The output is open-collector with a built-in 15 k $\Omega$ pull-up resistor.                                       |
| E1        | Input                  | Ground-Key Enable. E1 = High connects the ground-key detector to DET. E1 = Low connects the off-hook or ring-trip detector to DET.  |
| GKFIL     | —                      | Connection for external ground-key, noise-filter capacitor. See Notes 2 and 3.  |
| HPA       | Capacitor              | High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.  |
| HPB       | Capacitor              | High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.   |
| L         | Output<br>(See Note 1) | Switching Regulator Power Transistor. Connection point for filter inductor and anode of catch diode. Has up to 60 V of pulse waveform on it and must be isolated from sensitive circuits. Keep the diode connections short because of the high currents and high di/dt. |
| QBAT      | Battery                | Quiet Battery. (See Note 1). Filtered battery supply for the signal processing circuits   |
| RD        | Resistor               | Detector resistor. Detector threshold set and filter pin.   |
| RDC       | Resistor               | DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN).   |
| RINGOUT   | Output                 | Ring Relay Driver. Open-collector driver with emitter internally connected to BGND.   |
| RSN       | Input                  | Receive Summing Node. The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 500 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.                                   |
| TESTOUT   | Output                 | Test Relay Driver. Open collector driver with emitter internally connected to BGND. See Note 3.   |
| TP        | Thermal                | Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation                                |
| VBAT      | Battery                | Battery supply.   |
| VCC       | Power                  | +5 V power supply.  |
| VEE       | Power                  | –5 V power supply.  |
| VREG      | Input                  | Regulated Voltage. (See Note 1.) Provides negative power supply for power amplifiers. Connection point for inductor, filter capacitor, and chopper stabilization.   |
| VTX       | Output                 | Transmit Audio. This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.  |

**Notes:**

1. All pins, except CHCLK, connect to VBAT when using SLIC without a switching regulator. CHCLK is connected to AGND/DGND.
2. To prevent noise pickup by the detection circuits when using Ground-Key Detect state (E1 = logical 1), a 3300 pF minimum bypass capacitor is recommended between the GKFIL pin and ground.
3. Not available on standard 28-pin DIP package.

## ABSOLUTE MAXIMUM RATINGS

|   |                                     |
|---|-------------------------------------|
| Storage temperature   | −55°C to +150°C                     |
| V <sub>CC</sub> with respect to AGND/DGND   | −0.4 V to +7.0 V                    |
| V <sub>EE</sub> with respect to AGND/DGND   | +0.4 V to −7.0 V                    |
| V <sub>BAT</sub> with respect to AGND/DGND  | +0.4 V to −70 V                     |
| <b>Note:</b> Rise time of V <sub>BAT</sub> (dv/dt) must be limited to 27 V/μs or less when Q <sub>BAT</sub> bypass = 0.33 μF. |                                     |
| BGND with respect to AGND/DGND  | +1.0 V to −3.0 V                    |
| A(TIP) or B(RING) to BGND:  |                                     |
| Continuous  | −70 V to +1.0 V                     |
| 10 ms (f = 0.1 Hz)  | −70 V to +5.0 V                     |
| 1 μs (f = 0.1 Hz)   | −90 V to +10 V                      |
| 250 ns (f = 0.1 Hz)   | −120 V to +15 V                     |
| Current from A(TIP) or B(RING)  | ±150 mA                             |
| Voltage on RINGOUT  | BGND to 70 V above Q <sub>BAT</sub> |
| Voltage on TESTOUT  | BGND to 70 V above Q <sub>BAT</sub> |
| Current through relay drivers   | 60 mA                               |
| Voltage on ring-trip inputs<br>(DA and DB)  | V <sub>BAT</sub> to 0 V             |
| Current into ring-trip inputs   | ±10 mA                              |
| Peak current into regulator<br>switch (L pin)   | 150 mA                              |
| Switcher transient peak off<br>voltage on L pin   | +1.0 V                              |
| C4–C1, E1, CHCLK to<br>AGND/DGND  | −0.4 V to V <sub>CC</sub> + 0.4 V   |
| Maximum power dissipation, T <sub>A</sub> (see note)  | 70°C                                |
| In 28-pin ceramic DIP package   | 2.58 W                              |
| In 28-pin plastic DIP package   | 1.4 W                               |
| In 32-pin PLCC package  | 1.74 W                              |

**Note:** Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

|                                   |                    |
|-----------------------------------|--------------------|
| Ambient temperature               | 0°C to +70°C*      |
| V <sub>CC</sub>                   | 4.75 V to 5.25 V   |
| V <sub>EE</sub>                   | −4.75 V to −5.25 V |
| V <sub>BAT</sub>                  | −19 V to +58 V◆    |
| AGND/DGND                         | 0 V                |
| BGND with respect to<br>AGND/DGND | −100 mV to +100 mV |
| Load Resistance on VTX to ground  | 10 kΩ min          |

The Operating Ranges define those limits between which the functionality of the device is guaranteed.

\* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from −40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

◆ Can be used without switching regulator components in this range of battery voltages, provided maximum power dissipation specifications are not exceeded.

## ELECTRICAL CHARACTERISTICS

| Description  | Test Conditions (See Note 1)   | Min       | Typ                     | Max                     | Unit     | Note                    |
|--|--|-----------|-------------------------|-------------------------|----------|-------------------------|
| Analog ( $V_{TX}$ ) output impedance   |  | 3         |                         |                         | $\Omega$ | 4                       |
| Analog ( $V_{TX}$ ) output offset  | 0°C to +70°C   | -1*<br>-2 | -35<br>-35<br>-30       | +35<br>+35<br>+30       | mV       | 4                       |
|  | -40°C to +85°C   | -1*<br>-2 | -40<br>-40<br>-35       | +40<br>+40<br>+35       |          |                         |
| Analog (RSN) input impedance   | 300 Hz to 3.4 kHz  |           | 1                       | 20                      | $\Omega$ |                         |
| Longitudinal impedance at A or B   |  |           |                         | 35                      |          |                         |
| Overload level   | 4-wire<br>2-wire   | -2.5      |                         | +2.5                    | Vpk      | 2                       |
| <b>Transmission Performance, 2-Wire Impedance (See Test Circuit D)</b>   |  |           |                         |                         |          |                         |
| 2-wire return loss   | 300 Hz to 3400 Hz  | 26        |                         |                         | dB       | 4, 10                   |
| <b>Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C); <math>R_L = 600 \Omega</math></b>   |  |           |                         |                         |          |                         |
| Longitudinal to metallic L-T, L-4  | 200 Hz to 1 kHz<br>normal polarity 0°C to +70°C<br>normal polarity -40°C to +85°C<br>reverse polarity  |           | 52<br>63<br>58<br>54    |                         | dB       | 1, 2<br>1, 2, 4<br>1, 2 |
|  | 1 kHz to 3.4 kHz<br>normal polarity 0°C to +70°C<br>normal polarity -40°C to +85°C<br>reverse polarity |           | 52<br>58<br>54<br>54    |                         |          | 1, 2<br>1, 2, 4<br>1, 2 |
| Longitudinal signal generation 4-L   | 300 Hz to 800 Hz<br>Reverse polarity   | -1*<br>-2 | 40<br>40<br>42          |                         |          |                         |
| Longitudinal current capability per wire   | Active state   | all*      |                         | 28                      | mArms    |                         |
|  | OHT state  | all       |                         | 18                      |          |                         |
| <b>Insertion Loss (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B)</b><br>BAT = -48 V, $R_{LDC} = R_{LAC} = 600 \Omega$ ; BAT = -24 V, $R_{LDC} = 300 \Omega$ , $R_{LAC} = 600 \Omega$ |  |           |                         |                         |          |                         |
| Gain accuracy  | 0 dBm, 1 kHz<br>0°C to +70°C   | -1*<br>-2 | -0.15<br>-0.15<br>-0.10 | +0.15<br>+0.15<br>+0.10 | dB       |                         |
|  | 0 dBm, 1 kHz<br>-40°C to +85°C   | -1*<br>-2 | -0.20<br>-0.20<br>-0.15 | +0.20<br>+0.20<br>+0.15 |          | —<br>4<br>—             |
| Variation with frequency   | 300 Hz to 3400 Hz<br>Relative to 1 kHz<br>0°C to +70°C   | -1*<br>-2 | -0.15<br>-0.15<br>-0.10 | +0.15<br>+0.15<br>+0.10 | dB       |                         |
|  | 300 Hz to 3400 Hz<br>Relative to 1 kHz<br>-40°C to +85°C   | -1*<br>-2 | -0.20<br>-0.20<br>-0.15 | +0.20<br>+0.20<br>+0.15 |          | —<br>—<br>4             |

**Note:**

\*P.G. = Performance Grade

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

| Description  | Test Conditions (See Note 1)                                | Min  | Typ                     | Max                     | Unit | Note                 |
|--|---|--|-------------------------|-------------------------|------|----------------------|
| Gain tracking  | 0°C to +70°C<br>+7 dBm to -55 dBm<br>Reference: -0 dBm      | -0.10  |                         | +0.10                   | dB   |                      |
|  | -40°C to +85°C<br>+7 dBm to -55 dBm<br>Reference: -0 dBm    | -0.15  |                         | +0.15                   |      | 4<br>4<br>—          |
| <b>Balance Return Signal (4- to 4-Wire, See Test Circuit B)</b><br>BAT = -48 V, R <sub>LDC</sub> = R <sub>LAC</sub> = 600 Ω; BAT = -24 V, R <sub>LDC</sub> = 300 Ω, R <sub>LAC</sub> = 600 Ω |   |  |                         |                         |      |                      |
| Gain accuracy  | 0 dBm, 1 kHz<br>0°C to +70°C                                | -1*<br>-2  | -0.15<br>-0.15<br>-0.10 | +0.15<br>+0.15<br>+0.10 | dB   | —<br>3<br>—          |
|  | 0 dBm, 1 kHz<br>-40°C to +85°C                              | -1*<br>-2  | -0.20<br>-0.20<br>-0.15 | +0.20<br>+0.20<br>+0.15 |      | —<br>3, 4<br>3, 4    |
| Variation with frequency   | 300 Hz to 3400 Hz<br>Relative to 1 kHz<br>0°C to +70°C      |  | -0.10                   | +0.10                   | dB   | 3                    |
|  | 300 Hz to 3400 Hz<br>Relative to 1 kHz<br>-40°C to +85°C    |  | -0.15                   | +0.15                   |      | 3<br>3<br>3, 4       |
| Gain tracking  | 0°C to +70°C<br>+3 dBm to -55 dBm<br>Reference: 0 dBm       |  | -0.10                   | +0.10                   | dB   | 3                    |
|  | -40°C to +85°C<br>+3 dBm to -55 dBm<br>Reference: 0 dBm     |  | -0.15                   | -0.15                   |      | 3, 4                 |
| Group delay  | f = 1 kHz   |  | 5.3                     |                         | μs   | 4, 12                |
| <b>Total Harmonic Distortion (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B)</b><br>BAT = -48 V, R <sub>LDC</sub> = R <sub>LAC</sub> = 600 Ω                                      |   |  |                         |                         |      |                      |
| Harmonic distortion<br>300 Hz to 3400 Hz   | 0 dBm   |  | -64                     | -50                     | dB   |                      |
|  | +7 dBm  |  | -55                     | -40                     |      |                      |
| <b>Idle Channel Noise</b><br>BAT = -48 V, R <sub>LDC</sub> = R <sub>LAC</sub> = 600 Ω; BAT = -24 V, R <sub>LDC</sub> = 300 Ω, R <sub>LAC</sub> = 600 Ω                                       |   |  |                         |                         |      |                      |
| C-message weighted noise   | 2-wire, 0°C to +70°C<br>2-wire, -40°C to +85°C              |  | +7                      | +10<br>+12              | dBmC | 4<br>4               |
|  | 4-wire, 0°C to +70°C<br>4-wire, -40°C to +85°C              |  | +7                      | +10<br>+12              |      | 4<br>4               |
| Psophometric weighted noise  | 2-wire, 0°C to +70°C<br>2-wire, -40°C to +85°C              |  | -83                     | -80<br>-78              | dBmp | —<br>4               |
|  | 4-wire, 0°C to +70°C<br>4-wire, -40°C to +85°C              |  | -83                     | -80<br>-78              |      | —<br>4               |
| <b>Single Frequency Out-of-Band Noise (See Test Circuit E)</b>   |   |  |                         |                         |      |                      |
| Metallic   | 4 kHz to 9 kHz<br>9 kHz to 1 MHz<br>256 kHz and harmonics** |  | -76<br>-76<br>-63       |                         | dBm  | 4<br>4, 5, 8<br>4, 5 |
|  | Longitudinal  | 1 kHz to 15 kHz<br>Above 15 kHz<br>256 kHz and harmonics** |                         | -70<br>-85<br>-57       |      | 4<br>4, 5, 8<br>4, 5 |

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

| Description  | Test Conditions (See Note 1)  | Min                  | Typ               | Max                 | Unit | Note           |
|--|---|----------------------|-------------------|---------------------|------|----------------|
| <b>Line Characteristics (See Figures 1a, 1b, 1c)</b>   |   |                      |                   |                     |      |                |
| Short loops, Active state                              | Battery = -24 V, R <sub>LDC</sub> = 300 Ω<br>Battery = -43 V, R <sub>LDC</sub> = 600 Ω<br>Battery = -48 V, R <sub>LDC</sub> = 600 Ω   | 32.4                 | 35.0              | 37.6                | mA   | 4, 9<br>4<br>— |
| Long loops, Active state                               | Battery = -24 V, R <sub>LDC</sub> = 640 Ω<br>Battery = -43 V, R <sub>LDC</sub> = 1300 Ω<br>Battery = -48 V, R <sub>LDC</sub> = 1900 Ω | 20.0<br>23.0<br>18.0 |                   |                     |      | 4, 9<br>4<br>— |
| OHT state  | Battery = -24 V, R <sub>LDC</sub> = 600 Ω<br>Battery = -48 V, R <sub>LDC</sub> = 600 Ω  | 15.5                 | 17.5              | 19.5                |      | 4, 9<br>—      |
| Loop current   | Tip Open state, R <sub>L</sub> = 0<br>Disconnect state, R <sub>L</sub> = 0  |                      |                   | 1.0                 |      |                |
| I <sub>L</sub> LIM (ITip and IRing)                    | Tip and ring shorted to GND   |                      | 70                | 105                 |      |                |
| <b>Power Dissipation Battery, Normal Loop Polarity</b> |   |                      |                   |                     |      |                |
| On-hook Open Circuit state                             | Battery = -24 V, w/o switching reg.<br>Battery = -48 V, with switching reg.   |                      | 30<br>35          | 75<br>100           | mW   | 9<br>—         |
| On-hook OHT state                                      | Battery = -24 V, w/o switching reg.<br>Battery = -48 V, with switching reg.   | 100                  | 175<br>135        | 225                 |      | 9<br>—         |
| On-hook Active state                                   | Battery = -24 V, w/o switching reg.<br>Battery = -48 V, with switching reg.   |                      | 135<br>180        | 225<br>300          |      | 9<br>—         |
| Off-hook OHT state<br>R <sub>L</sub> = 50 Ω            | Battery = -24 V, w/o switching reg.<br>Battery = -48 V, with switching reg.   |                      | 500<br>400        | 800<br>750          |      | 9<br>—         |
| Off-hook Active state<br>R <sub>L</sub> = 50 Ω         | Battery = -24 V, w/o switching reg.<br>Battery = -48 V, with switching reg.   |                      | 800<br>800        | 1100<br>1000        |      | 9<br>—         |
| <b>Supply Currents, Battery = -24 V or -48 V</b>       |   |                      |                   |                     |      |                |
| V <sub>CC</sub> on-hook supply current                 | Open Circuit state<br>OHT state<br>Active state   |                      | 3.0<br>6.0<br>7.5 | 4.5<br>10.0<br>12.0 | mA   | 9              |
| V <sub>EE</sub> on-hook supply current                 | Open Circuit state<br>OHT state<br>Active state   |                      | 1.0<br>2.2<br>2.7 | 2.3<br>3.5<br>6.0   |      |                |
| V <sub>BAT</sub> on-hook supply current                | Open Circuit state<br>OHT state<br>Active state   |                      | 0.4<br>3.0<br>4.0 | 1.0<br>5.0<br>6.0   |      |                |

**Note:**

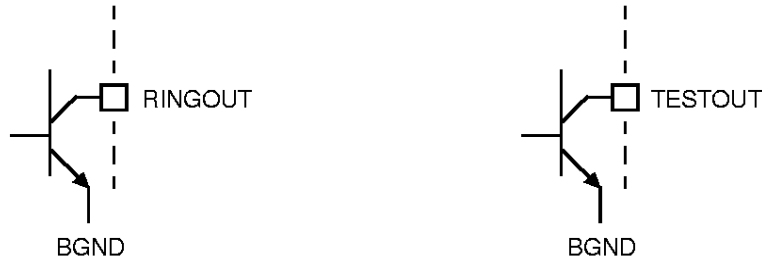
\*\*Applies only when switching regulator is used.

| <b>Power Supply Rejection Ratio (V<sub>RIPPLE</sub> = 50 mVrms)</b> |                   |    |     |     |    |   |
|---|-------------------|----|-----|-----|----|---|
| V <sub>CC</sub>   | 50 Hz to 3.4 kHz  | 25 | 45  |     | dB | 6 |
|   | 3.4 kHz to 50 kHz | 22 | 35  |     |    |   |
| V <sub>EE</sub>   | 50 Hz to 3.4 kHz  | 20 | 40  |     |    |   |
|   | 3.4 kHz to 50 kHz | 10 | 25  |     |    |   |
| V <sub>BAT</sub>  | 50 Hz to 3.4 kHz  | 27 | 45  |     |    |   |
|   | 3.4 kHz to 50 kHz | 20 | 40  |     |    |   |
| Effective int. resistance   | CAS to GND        | 85 | 170 | 255 | kΩ | 4 |

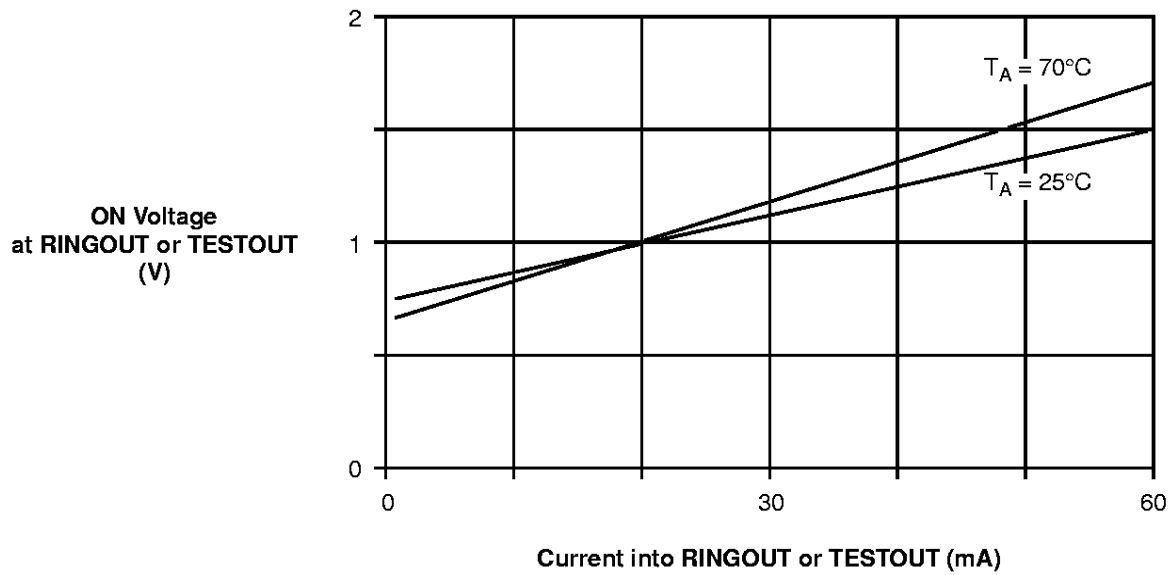
## ELECTRICAL CHARACTERISTICS (CONTINUED)

| Description   | Test Conditions (See Note 1)                                       | Min        | Typ        | Max         | Unit       | Note   |
|---|--|------------|------------|-------------|------------|--------|
| <b>Off-Hook Detector</b>                            |  |            |            |             |            |        |
| Current threshold                                   | $I_{DET} = 365/R_D$  | -20        |            | +20         | %          |        |
| <b>Ground-Key Detector Thresholds, Active State</b> |  |            |            |             |            |        |
| Ground-key resistance threshold                     | Battery = -24 V, B(RING) to GND<br>Battery = -48 V, B(RING) to GND | 1.0<br>2.0 | 2.2<br>5.0 | 4.5<br>10.0 | k $\Omega$ | 9<br>— |
| Ground-key current threshold                        | B(RING) to GND<br>Midpoint to GND                                  |            | 9<br>9     |             | mA         | 7      |
| Effective internal resistance                       | GKFIL to AGND/DGND   | 18         | 36         | 54          | k $\Omega$ | 4      |
| <b>Ring-Trip Detector Input</b>                     |  |            |            |             |            |        |
| Bias current  |  | -5         | -0.05      |             | $\mu$ A    |        |
| Offset voltage                                      | Source resistance = 0 to 2 M $\Omega$                              | -50        | 0          | +50         | mV         | 11     |
| <b>Logic Inputs (C4–C1, E0, E1, and CHCLK)</b>      |  |            |            |             |            |        |
| Input High voltage                                  |  | 2.0        |            |             | V          |        |
| Input Low voltage                                   |  |            |            | 0.8         |            |        |
| Input High current                                  | All inputs except E1   | -75        |            | 40          | $\mu$ A    |        |
| Input High current                                  | Input E1   | -75        |            | 45          |            |        |
| Input Low current                                   |  | -0.4       |            |             | mA         |        |
| <b>Logic Output (<math>\overline{DET}</math>)</b>   |  |            |            |             |            |        |
| Output Low voltage                                  | $I_{OUT} = 0.8$ mA   |            |            | 0.4         | V          |        |
| Output High voltage                                 | $I_{OUT} = -0.1$ mA  | 2.4        |            |             |            |        |
| <b>Relay Driver Outputs (RINGOUT, TESTOUT)</b>      |  |            |            |             |            |        |
| On voltage  | 25 mA sink   |            |            | +1.5        | V          |        |
| Off leakage   | $V_{OH} = +15$ V   |            |            | 100         | $\mu$ A    |        |

RELAY DRIVER SCHEMATICS



15474A-002

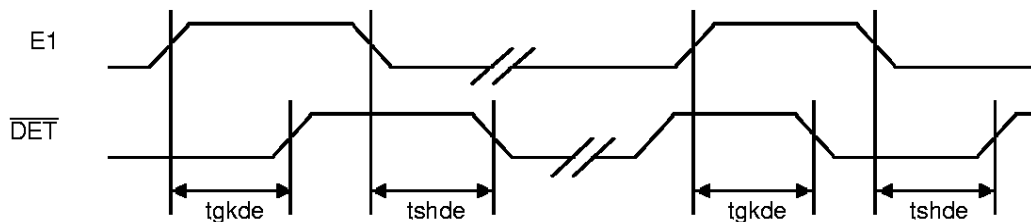


SWITCHING CHARACTERISTICS

| Symbol | Parameter  | Test Conditions  | Temperature Range | Min | Typ | Max | Unit          | Note |
|--------|--|--|-------------------|-----|-----|-----|---------------|------|
| tgkde  | E1 Low to $\overline{\text{DET}}$ High (E0 = 1)  | Ground-Key Detect state<br>$R_L$ open, $R_G$ connected<br>(See Figure H)     | 0°C to +70°C      |     |     | 3.8 | $\mu\text{s}$ | 4    |
|        | -40°C to +85°C                                   |  |                   |     | 4.0 |     |               |      |
| tshde  | E1 Low to $\overline{\text{DET}}$ Low (E0 = 1)   | Switchhook Detect state<br>$R_L = 600 \Omega$ , $R_G$ open<br>(See Figure G) | 0°C to +70°C      |     |     | 1.1 |               |      |
|        | -40°C to +85°C                                   |  |                   |     | 1.6 |     |               |      |
| tshde  | E1 High to $\overline{\text{DET}}$ Low (E0 = 1)  | Switchhook Detect state<br>$R_L = 600 \Omega$ , $R_G$ open<br>(See Figure G) | 0°C to +70°C      |     |     | 1.2 |               |      |
|        | -40°C to +85°C                                   |  |                   |     | 1.7 |     |               |      |
| tshde  | E1 High to $\overline{\text{DET}}$ High (E0 = 1) | Switchhook Detect state<br>$R_L = 600 \Omega$ , $R_G$ open<br>(See Figure G) | 0°C to +70°C      |     |     | 3.8 |               |      |
|        | -40°C to +85°C                                   |  |                   |     | 4.0 |     |               |      |

SWITCHING WAVEFORMS

E1 to  $\overline{\text{DET}}$

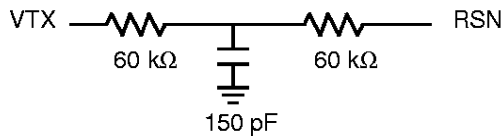


**Note:**  
All delays measured at 1.4 V levels.

15474A-003

**Notes:**

1. Unless otherwise noted, test conditions are  $BAT = -48\text{ V}$ ,  $V_{CC} = +5\text{ V}$ ,  $V_{EE} = -5\text{ V}$ ,  $R_L = 600\ \Omega$ ,  $C_{HP} = 0.33\ \mu\text{F}$ ,  $R_{DC1} = R_{DC2} = 7.14\ \text{k}\Omega$ ,  $C_{DC} = 0.47\ \mu\text{F}$ ,  $R_D = 35.4\ \text{k}\Omega$ ,  $C_{CAS} = 0.47\ \mu\text{F}$ , no fuse resistors,  $R_T = 120\ \text{k}\Omega$ , and  $R_{RX} = 60\ \text{k}\Omega$ . Switching regulator components:  $L = 1\ \text{mH}$ ,  $C_{FIL} = 0.47\ \mu\text{F}$  (see Application Circuit).
2. Overload level is defined when  $THD = 1\%$ .
3. Balance return signal is the signal generated at  $V_{TX}$  by  $V_{RX}$ . This specification assumes the two-wire AC load impedance matches the programmed impedance.
4. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
5. For frequencies below 12 kHz, these tests are performed with a longitudinal impedance of  $90\ \Omega$  and metallic impedance of  $300\ \Omega$ . For frequencies greater than 12 kHz, a longitudinal impedance of  $90\ \Omega$  and a metallic impedance of  $135\ \Omega$  is used. These tests are extremely sensitive to circuit board layout. Please refer to application notes for details.
6. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
7. "Midpoint" is defined as the connection point between two  $300\ \Omega$  series resistors connected between A(TIP) and B(RING).
8. Fundamental and harmonics from 256 kHz switch regulator chopper are not included.
9. For  $-24\text{ V}$  battery, switching regulator is disabled. L, CHS, and VREG pins connected to VBAT pin; CHCLK pin connected to AGND/DGND.
10. Assumes the following  $Z_T$  network:



11. Tested with  $0\ \Omega$  source impedance.  $2\ \text{M}\Omega$  is specified for system design purposes only.
12. Group delay can be considerably reduced by using a  $Z_T$  network such as that shown in Note 10 above. The network reduces the group delay to less than  $2\ \mu\text{s}$ . The effect of group delay on linecard performance may be compensated for by using the QSLAC™ or DSLAC™ device.

**Table 1. SLIC Decoding**

| State | C3 C2 C1 | Two-Wire Status          | DET Output    |            |
|-------|----------|--------------------------|---------------|------------|
|       |          |                          | E1 = 0        | E1 = 1     |
| 0     | 0 0 0    | Open Circuit             | Ring trip     | Ring trip  |
| 1     | 0 0 1    | Ringing                  | Ring trip     | Ring trip  |
| 2     | 0 1 0    | Active                   | Loop detector | Ground key |
| 3     | 0 1 1    | On-Hook TX (OHT)         | Loop detector | Ground key |
| 4     | 1 0 0    | Tip Open                 | Loop detector | —          |
| 5     | 1 0 1    | Reserved                 | Loop detector | —          |
| 6     | 1 1 0    | Active Polarity Reversal | Loop detector | Ground key |
| 7     | 1 1 1    | OHT Polarity Reversal    | Loop detector | Ground key |

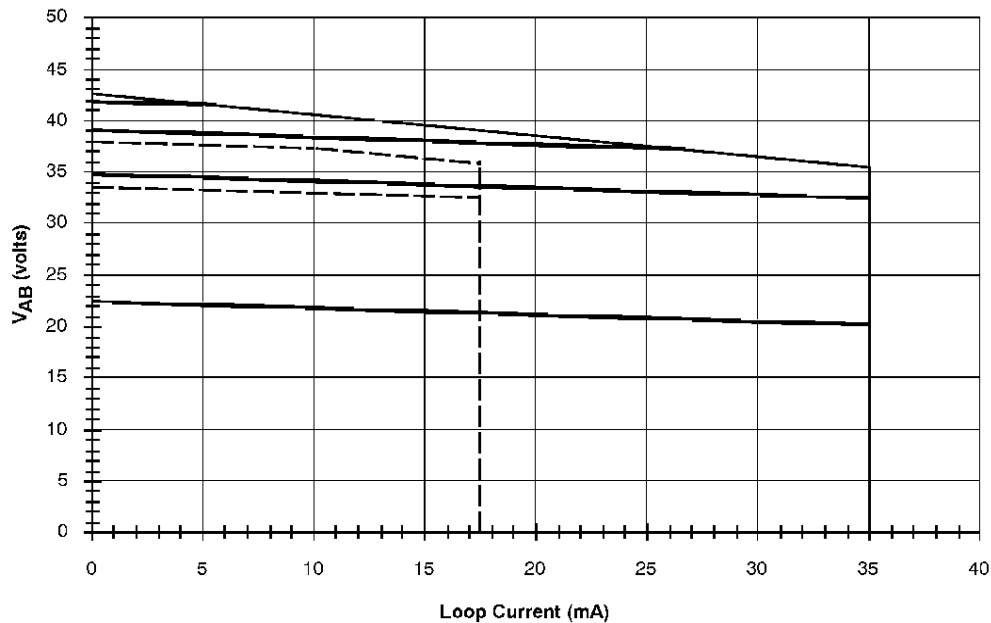
Table 2. User-Programmable Components

|  |   |
|--|---|
| $Z_T = 200(Z_{2WIN} - 2R_F^*)$   | <p><math>Z_T</math> is connected between the VTX and RSN pins. The fuse resistors are <math>R_F</math>, and <math>Z_{2WIN}</math> is the desired 2-wire AC input impedance. When computing <math>Z_T</math>, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.</p> |
| $Z_{RX} = \frac{Z_L}{G_{42L}} \cdot \frac{200Z_T}{Z_T + 200(Z_L + 2R_F)}$  | <p><math>Z_{RX}</math> is connected from <math>V_{RX}</math> to the RSN. <math>Z_T</math> is defined above, and <math>G_{42L}</math> is the desired receive gain.</p>   |
| $R_{DC1} + R_{DC2} = \frac{500}{I_{LOOP}}$ $C_{DC} = 1.5 \text{ ms} \cdot \frac{R_{DC1} + R_{DC2}}{R_{DC1} R_{DC2}}$ | <p><math>R_{DC1}</math>, <math>R_{DC2}</math>, and <math>C_{DC}</math> form the network connected to the RDC pin. <math>R_{DC1}</math> and <math>R_{DC2}</math> are approximately equal. <math>I_{LOOP}</math> is the desired loop current in the constant-current region.</p>  |
| $R_D = \frac{365}{I_T}, \quad C_D = \frac{0.5 \text{ ms}}{R_D}$  | <p><math>R_D</math> and <math>C_D</math> form the network connected from RD to <math>-5 \text{ V}</math>, and <math>I_T</math> is the threshold current between on hook and off hook.</p>   |
| $C_{CAS} = \frac{1}{3.4 \cdot 10^5 \pi f_c}$   | <p><math>C_{CAS}</math> is the regulator filter capacitor, and <math>f_c</math> is the desired filter cut-off frequency.</p>  |

**Note:**

\* $R_{FUSE} = 20 \Omega - 50 \Omega$ , user selectable.

## DC FEED CHARACTERISTICS



$$R_{DC1} + R_{DC2} = R_{DC} = 14.28 \text{ k}\Omega$$

———— Active state  
 - - - - - OHT state

**Notes:**

1. Constant-current region:

Active state:  $I_L = \frac{500}{R_{DC}}$

OHT state:  $I_L = \frac{250}{R_{DC}}$

2. Anti-saturation turn-on (Active state):

a. Battery independent:  $V_{AB} = 35.5 \text{ V}$ ,  $(|V_{BAT}| > 46.2 \text{ V})$

b. Battery tracking:  $V_{AB} = 1.1 |V_{BAT}| - 15$ ,  $(|V_{BAT}| \geq 46.2 \text{ V})$

$V_{AB} = 0.7 |V_{BAT}| + 3.5$ ,  $(|V_{BAT}| < 46.2 \text{ V})$

3. Open circuit voltage:

Active state:  $V_{AB} = 42.6$ ,  $(|V_{BAT}| > 53 \text{ V})$

$V_{AB} = 0.7 |V_{BAT}| + 5.89$ ,  $(|V_{BAT}| \leq 53 \text{ V})$

OHT state,  $V_{AB} = 39.1$ ,  $(|V_{BAT}| > 49.8 \text{ V})$

$V_{AB} = 0.7 |V_{BAT}| + 4.7$ ,  $(|V_{BAT}| \leq 49.8 \text{ V})$

4. Anti-saturation 1 region:

Active state:  $V_{AB} = 46.2 - I_L \left( \frac{R_{DC}}{70.4} \right)$

OHT state:  $V_{AB} = 39.1 - I_L \left( \frac{R_{DC}}{70.4} \right)$

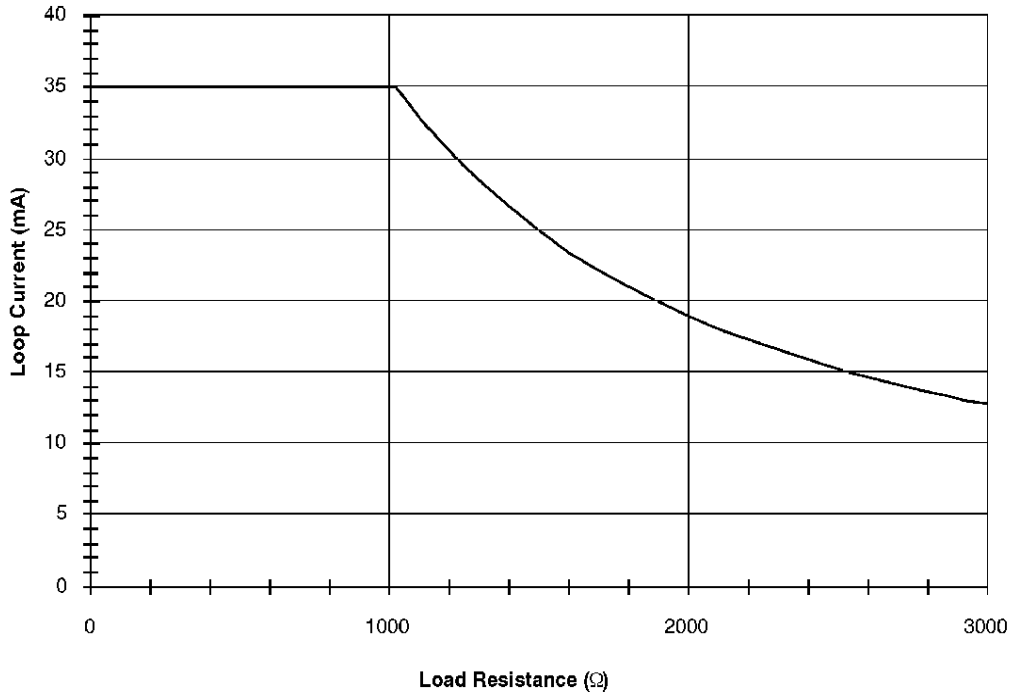
5. Anti-saturation 2 region:

Active state:  $V_{AB} = 0.7 |V_{BAT}| + 5.89 - I_L \left( \frac{R_{DC}}{210} \right)$

OHT state:  $V_{AB} = 0.7 |V_{BAT}| + 4.7 - I_L \left( \frac{R_{DC}}{210} \right)$

a.  $V_A - V_B$  ( $V_{AB}$ ) Voltage vs. Loop Current (Typical)

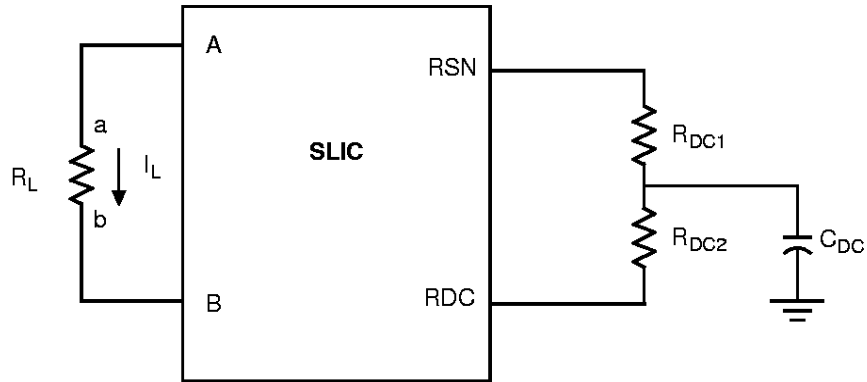
DC FEED CHARACTERISTICS (continued)



$R_{DC1} + R_{DC2} = R_{DC} = 14.28 \text{ k}\Omega$

$V_{BAT} = 47.3 \text{ V}$

b. Loop Current vs. Load Resistance (Typical)



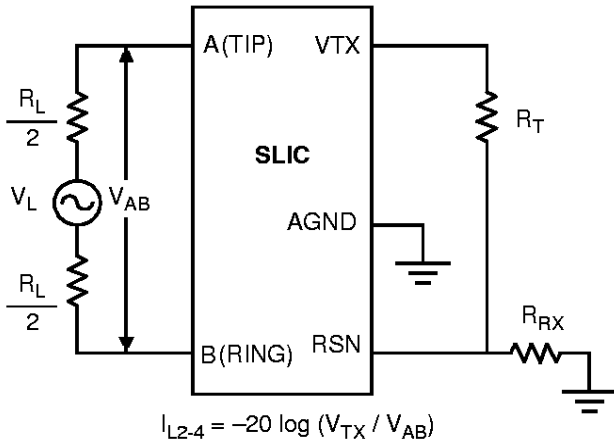
Feed current programmed by  $R_{DC1}$  and  $R_{DC2}$

c. Feed Programming

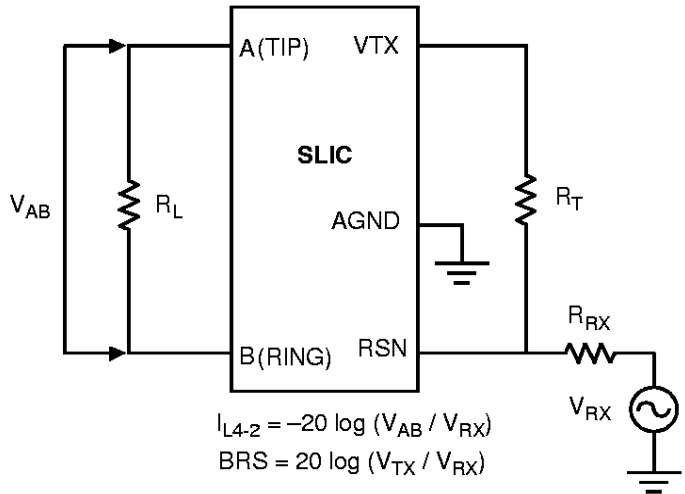
15474A-004

Figure 1. DC Feed Characteristics

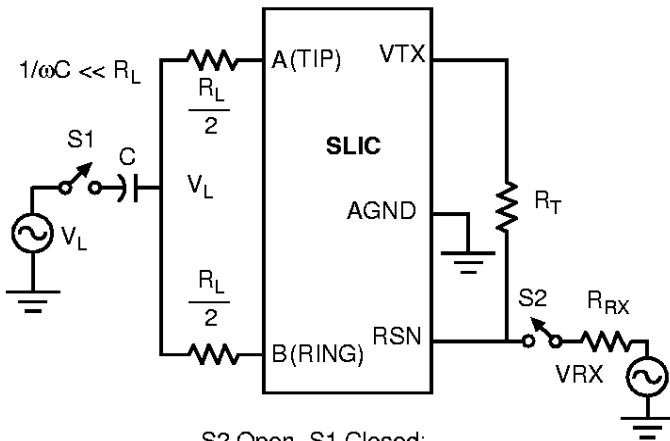
TEST CIRCUITS



A. Two- to Four-Wire Insertion Loss



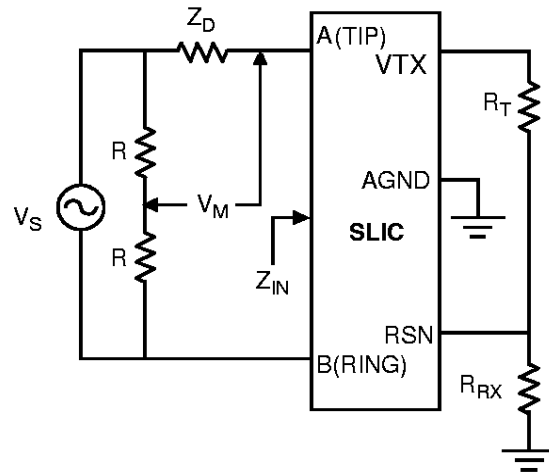
B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:  
 L-T Long. Bal. =  $20 \log (V_{AB} / V_L)$   
 L-4 Long. Bal. =  $20 \log (V_{TX} / V_L)$

S2 Closed, S1 Open:  
 4-L Long. Sig. Gen. =  $20 \log (V_L / V_{RX})$

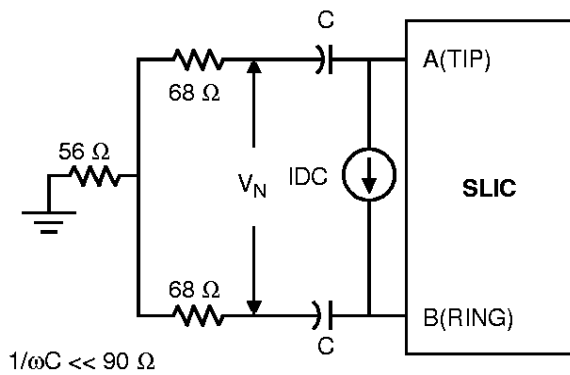
C. Longitudinal Balance



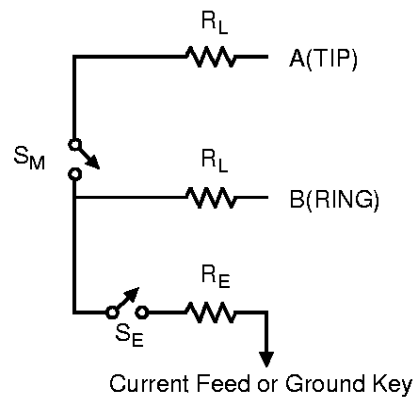
**Note:**  
 $Z_D$  is the desired impedance (e.g., the characteristic impedance of the line).  
 $R_L = -20 \log (2 V_M / V_S)$

D. Two-Wire Return Loss Test Circuit

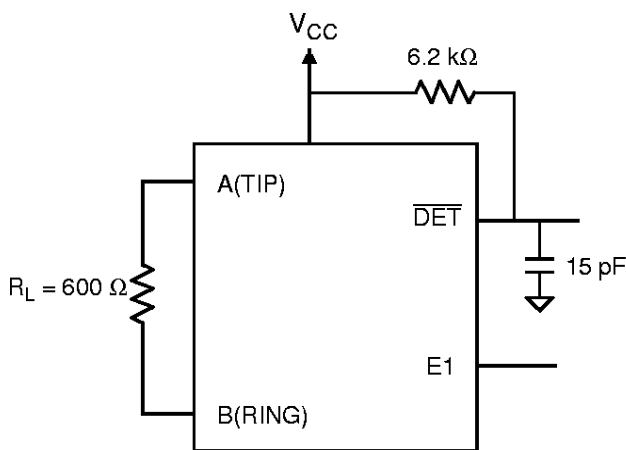
TEST CIRCUITS (continued)



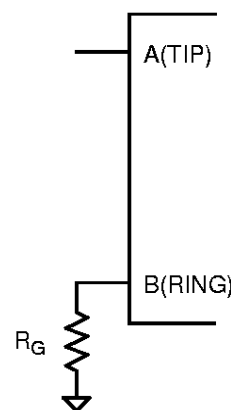
E. Single-Frequency Noise



F. Ground-Key Detection Center Point Test



G. Loop-Detector Switching



$R_G$ : 2 k $\Omega$  at  $V_{BAT} = -48$  V  
 1 k $\Omega$  at  $V_{BAT} = -24$  V

H. Ground-Key Switching

REVISION SUMMARY

Revision C to Revision D

- Minor changes were made to the data sheet style and format to conform to AMD standards.
- Table 1—Some information in the table was revised, including the addition of the Reserved status.

Revision D to Revision E

- Minor changes were made to the data sheet style and format to conform to AMD standards.
- In Pin Description table, inserted/changed TP pin description to: "Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation."

Trademarks

Copyright © 1998 Advanced Micro Devices, All rights reserved.

AMD, the AMD logo and combinations thereof are trademarks of Advanced Micro Devices, Inc.

DSLAC and QSLAC are trademarks of Advanced Micro Devices, Inc.

Product names used in this publication are for identification purposes only and may be trademarks of their respective companies.