TS 83006

BIPOLAR HIGH-SPEED 6-BIT FLASH A/D CONVERTER

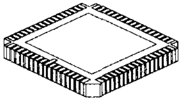
DESCRIPTION

The TS 83006 is a monolithic bipolar 6-bit parallel flash analog-to-digital converter, which is an alternate source for the AD9006 circuit.

The TS 83006 uses 64 parallel comparators to digitize fast moving analog input signals without external sample-and-hold circuits or input buffers. The analog input is designed for −1 V to +1 V operation. The output data includes an overflow bit and complementary data ready signals. Control pins allow to invert the MSB and/or LSBs.

With encode rates up to 600 MHz, the TS 83006 is specified to operate from commercial to military temperature range with an analog input frequency up to 200 MHz, making it ideal for a variety of applications and environments.

The TS 83006 is packaged in an hermetic 68-pin LCCC configuration and is also available in die form.

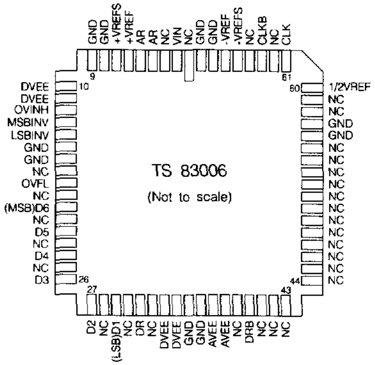


E
LCCC 68
(Leadless Ceramic Chip Carrier)

MAIN FEATURES

- 6-bit resolution.
- 600 MHz sampling rate.
- 30 dB SNR at 200 MHz analog input.
- Power consumption : 1.5 W.
- 550 MHz large signal input bandwidth.
- −55°C / +125°C specified.
- ECL 10 K compatible.
- Overflow bit & bit invert functions.
- Complementary data ready outputs.
- Very low input capacitance : 8 pF.
- No sample & hold required.
- Pin to pin compatible with AD 9006.

PIN CONNECTIONS
(Top view)
LCCC CERAMIC - 68 PINS



Note : For details see «Pin Description»

APPLICATIONS

- Military systems.
- Radar pulse analysis.
- Video digitizing.
- Communication/signal intelligence.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Positive supply voltage (Note 2)	A_R	0.7 to 5.5	V
Negative supply voltage (Note 2)	AV_{EE}, DV_{EE}	− 6 to + 0.3	V
Upper reference voltage	$+V_{REF}$, $+V_{REFS}$	− 1.5 to 1.5	V
Lower reference voltage	$-V_{REF}$, $-V_{REFS}$		
Midscale reference voltage	1/2 V_{REF}		
Analog input voltage	V_{IN}		
Reference voltage range	$+V_{REF}$ to $-V_{REF}$	2.2	V
Clock input voltages	CLK, CLKB	V_{EE} to 0	V
Maximum difference between negative supplies	DV_{EE} to AV_{EE}	± 0.5	V
Digital output current	I_D	20	mA
Midscale reference current	I (1/2 V_{REF})	4	mA
Junction temperature	T_j	+ 175	°C
Storage temperature	T_{stg}	− 65 to + 150	°C
Operating temperature range	T_{case}	− 55 to + 125	°C
Lead temperature (soldering 10 s)	T_{leads}	+ 260	°C
Digital input voltages	LSB_{INV}, MSB_{INV}, OV_{INH}	V_{EE} to 0	V

Note 1 : Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions.
Long exposure to maximum rating may affect device reliability.

Note 2 : With respect to AGND = DGND.

USER WARNING

The power supplies must be applied before all the other signals to prevent damage from occuring on the device.

To prevent reliability problem and dynamic performance damage, high speed transition on power supply must be avoided.

SPECIFICATIONS

Electrical operating characteristics

$AV_{EE} = DV_{EE} = -5.2\ V$; $AR = 3\ V$; $R_L = 100\ \Omega$ to $-2\ V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	T_{case}	Test level	Min.	Typ.	Max.	Unit
RESOLUTION			6			Bits
DIGITAL INPUTS AND OUTPUTS						
Logic compatibility				ECL 10 K		
Clock inputs						
• Logic «0» voltage	full	IV			– 1.5	V
• Logic «1» voltage	full	IV	– 1.1			V
Output data						
• Logic «0» voltage (Note 1)	full	II, D			– 1.5	V
• Logic «1» voltage (Note 2)	full	II, D	– 1.1			V
MAXIMUM CLOCK FREQUENCY		III	500	600		MHz
ANALOG INPUT						
Voltage range	full	V		± 1		V
Input capacitance		IV		8		pF
Input resistance		V		350		kΩ
Analog bandwidth (Note 3)		V		550		MHz
REFERENCE INPUT						
Differential reference voltage	full	II, D		2	2.1	V
Reference ladder resistance	full	II, D	90	150	210	Ω
POWER REQUIREMENTS						
Positive supply voltage		I, D	2	3	5.25	V
	full	II	2	3	5.25	V
Positive supply current		I, D		22	29	mA
(AR = 3 V)	full	II			30	mA
Negative supply voltage		I, D	– 5.7	– 5.2	– 4.7	V
	full	II	– 5.7	– 5.2	– 4.7	V
Negative supply current		I, D		270	330	mA
(V_{EE} = – 5.2 V)	full	II			350	mA
Nominal power dissipation (Note 4)		V		1.5		W
Reference ladder dissipation		V		30		mW
THERMAL RESISTANCE						
Junction-to-ambient (Note 5)		V		33		°C/W
Junction-to-case		V		1.2		°C/W
ACCURACY						
Integral nonlinearity (Note 6)		I, D		0.1	0.25	LSB
	full	II		0.15	0.5	LSB
Differential nonlinearity (Note 6)		I, D		0.15	0.25	LSB
	full	II		0.2	0.5	LSB
Monotonicity and no missing codes	full	IV	Guaranteed over specified temperature range			

SPECIFICATIONS (Continued)

Electrical operating characteristics

$AV_{EE} = DV_{EE} = -5.2$ V ; AR = 3 V ; $R_L = 100\,\Omega$ to -2 V ; $T_C = 25$°C (unless otherwise specified)

Parameter	Test level	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS					
Signal to noise ratio (SNR)					
F_S = 10 MHz F_{in} = 1.5 MHz	D	35.5	37		dB
F_S = 500 MHz F_{in} = 1 MHz	III	34.9	36.1		dB
F_S = 400 MHz F_{in} = 10 MHz	III	34.9	36.1		dB
F_S = 400 MHz F_{in} = 100 MHz	III	31.8	34		dB
F_S = 400 MHz F_{in} = 196 MHz	III	28.2	30		dB
Total harmonic distorsion (THD)					
F_S = 10 MHz F_{in} = 1.5 MHz	D	40	60		dB
F_S = 500 MHz F_{in} = 1 MHz	III	42	44		dB
F_S = 400 MHz F_{in} = 10 MHz	III	42	48		dB
F_S = 400 MHz F_{in} = 100 MHz	III	33	36		dB
F_S = 400 MHz F_{in} = 196 MHz	III	31	36		dB
Effective number of bits					
F_S = 10 MHz F_{in} = 1.5 MHz	D	5.6	5.9		Bits
F_S = 500 MHz F_{in} = 1 MHz	III	5.5	5.7		Bits
F_S = 400 MHz F_{in} = 10 MHz	III	5.5	5.7		Bits
F_S = 400 MHz F_{in} = 100 MHz	III	5.0	5.4		Bits
F_S = 400 MHz F_{in} = 196 MHz	III	4.4	4.7		Bits

Note 1 : With I_{OUT} = 2 mA.

Note 2 : With I_{OUT} = 12 mA.

Note 3 : See definition of terms.

Note 4 : With AR = 3 V. $AV_{EE} = DV_{EE} = -5.2$ V.

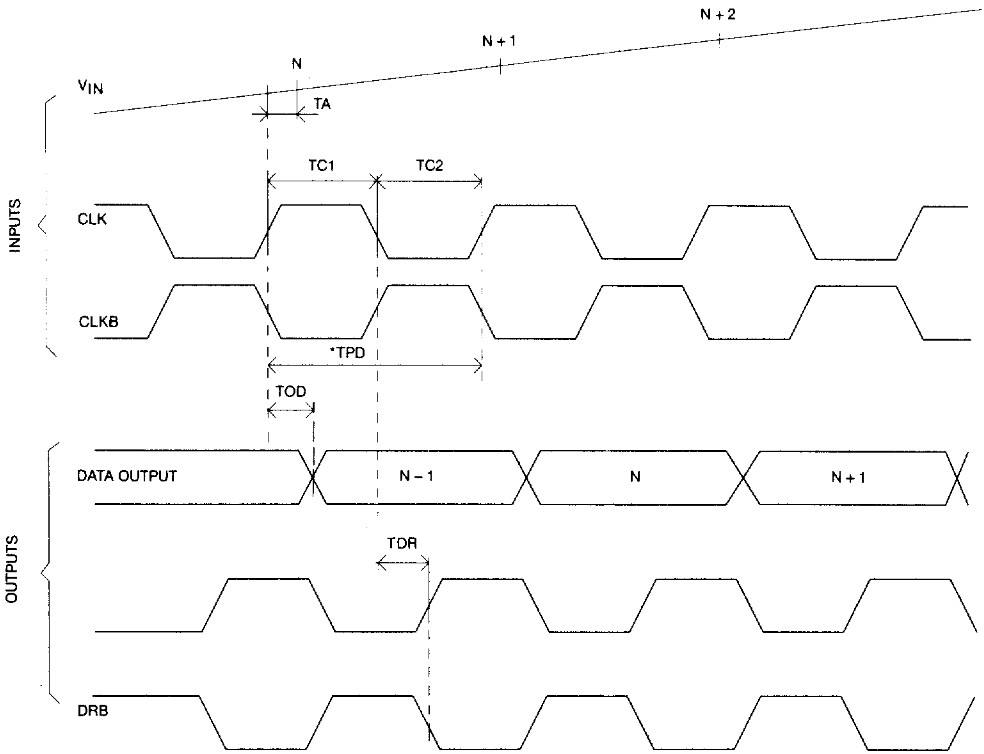
Note 5 : 33°C/W on glass epoxy board. 18°C/W on ceramic board.

Note 6 : Histogram based on sampling of 1.5 MHz sinusoïdal analog signal with and encode rate of 10 MHz.

EXPLANATION OF TEST LEVELS

Test level	
I	100 % production tested.
II	100 % production tested at +25°C, and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
D	100 % probe tested on wafer at T_{amb} = +25°C.

TIMING DIAGRAM



* TPD : Pipe line delay.

Figure 1

SWITCHING PERFORMANCES (Notes 1 and 2)

Parameter	Symbol	Typ.	Unit
Minimum Clock pulse width (high)	TC1	0.8	ns
Minimum Clock pulse width (low)	TC2	1	ns
Aperture delay	TA	0.3	ns
Aperture uncertainty (Note 1)		3	ps
Output delay	TOD	2.7	ns
Data ready output delay	TDR	2.8	ns
Output rise time (Note 3)		1	ns
Output fall time (Note 3)		1	ns

Note 1 : See definitions of terms.

Note 2 : $AV_{EE} = DV_{EE} = -5.2$ V ; AR = 3 V ; $+V_{REF} = +1$ V ; $-V_{REF} = -1$ V.

Note 3 : Outputs terminated through 100 Ω to − 2 V. $C_{load} < 6$ pF. Clock command rise/fall time should be less than 1.5 ns in normal operating mode.

FUNCTIONAL BLOCK DIAGRAM

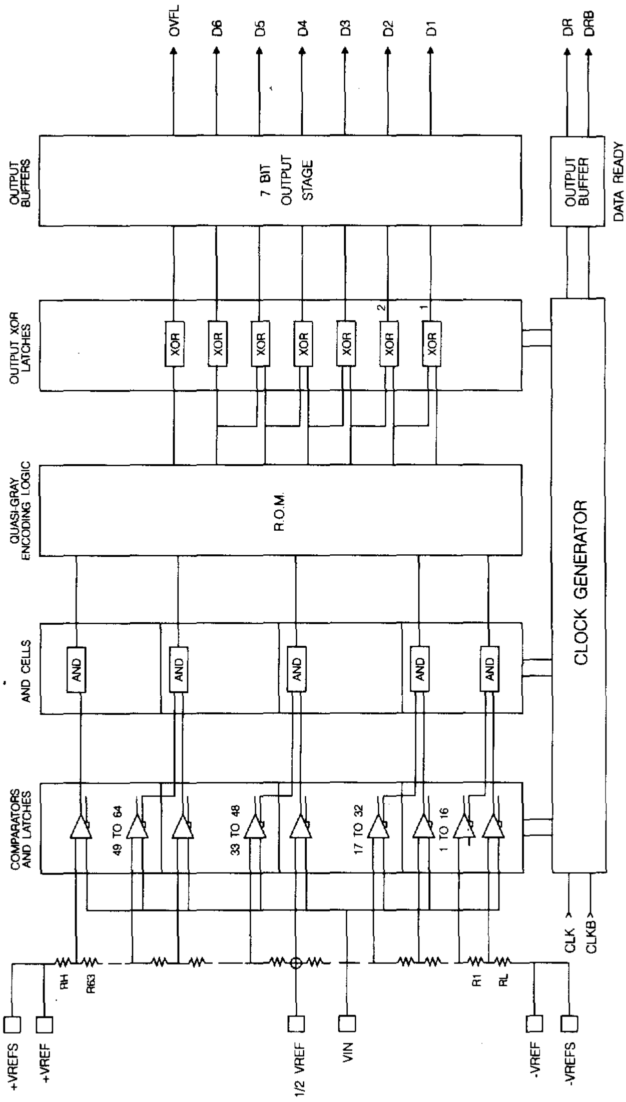


Figure 2

PIN DESCRIPTION

Pin	Name	Function
4, 5	AR	Positive supply voltage, (analog return)
37, 38	AV_{EE}	Negative supply voltage, analog section
61	CLK	Non inverted input of clock command (ECL)
63	CLKB	Inverted input of clock command (ECL)
29, 27, 26, 24, 22, 20	D1-D6	Digital data output (ECL)
10, 11, 33, 34	DV_{EE}	Negative supply voltage, digital section
31	DR	Data ready output signal (ECL)
40	DRB	Complementary data ready output signal (ECL)
8, 9, 15, 16, 35, 36, 56, 57, 67, 68	GND	Ground connections. Pins 8, 9, 15, 16, 35, 36, 56 and 57 are digital ground Pins 67 and 68 are analog ground
14	LSB_{INV}	LSBs invert, (D1 - D5) (see note 1)
13	MSB_{INV}	MSBs invert, (D6) (see note 2)
18	O_{VFL}	Overflow data output (ECL)
12	O_{VINH}	Overflow inhibit (ECL) (see note 3)
2	V_{IN}	Analog input, nominally between − 1 V and + 1 V
66	$-V_{REF}$	Negative reference voltage
65	$-V_{REFS}$	Negative reference voltage sense
60	$1/2\ V_{REF}$	Midpoint of reference resistor ladder
6	$+V_{REF}$	Positive voltage reference
7	$+V_{REFS}$	Positive reference voltage sense
1, 3, 17, 19, 21, 23, 25, 28, 30, 32, 39, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 58, 59, 62, 64	NC	Not connected

Seal ring of LCCC 68 package is internally connected to ground. Heat spreader of LCCC 68 is internally connected to V_{EE}, (device substrate).

Note 1 : When tied at V_{EE} (or floating), lower order (D1-D5) output bits are inverted. No inversion when grounded.

Note 2 : When tied at V_{EE} (or floating), MSB is inverted. No inversion when grounded.

Note 3 : When connected to ground, the overflow bit is inhibited and the nonreturn-to-zero feature is actived.

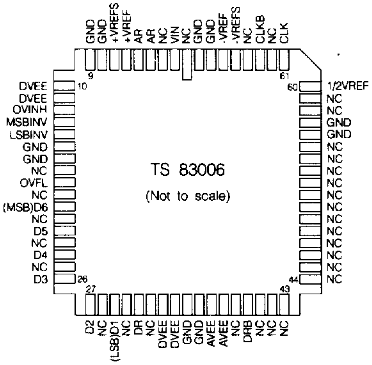


Figure 3

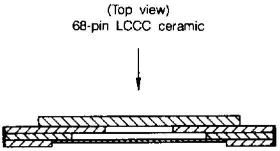


Figure 4

THEORY OF OPERATION

The block diagram (see page 6) shows a conventional flash converter structure having one comparator per state.
This architecture enables very high speed operation, without external sample and hold.

The analog input signal is fed to all comparators, and is compared to a set of 64 reference levels (6 bits + overflow), derived from a resistor ladder network.
Midpoint tap (1/2 V_{REF}) of the reference ladder is provided for linearity adjustment or transfer function modification.

When not used, a decoupling capacitor of 100 nF connected to AGND is recommended to minimize high frequency noise injection.

A set of 64 AND latches following the comparator array indicates the appropriate quantization level of the analog input signal.
An encoder stage and master-slave latches provide synchronized output data in binary code.

High speed output ECL buffers using active pulldown current sources, makes it possible to drive high capacitive loads (up to 6 pF) at maximum sampling rate without the need of external buffers.
A Data Ready circuit delivers differential output strobe signals, which track internal propagation delay, and facilitate in output data acquisition.

APPLICATIONS

User warning

The power supplies must be applied before all the other signals to prevent damage from occuring on the device.

Functional description

The TS 83006 operates with input analog signals varying between ± V_{REF} reference voltages, (Nominally $+V_{REF} = +1$ V, $-V_{REF} = -1$ V), applied across an internal resistor ladder.

Maximum differential Reference voltage is 2.1 V, so external reference generator circuit must limit the voltage to this value, to avoid permanent damage caused to the TS 83006 by excessive current densities.
The offset errors caused by input ± V_{REF} access resistances, can be cancelled using voltage sense lines (± V_{REFS} pins). (Maximum sense current : 500 μA).

The typical input capacitance of the TS 83006 is 8 pF, which can be driven directly by most 50 Ω signal sources.
Differential input ECL clock signals are recommended for the TS 83006, to reduce jitter and thus to improve output noise floor.
Fast clock transition times (< 500 ps, 300 ps recommended), are required when digitizing high-frequency input waveforms.

Clock generator with very low clock period jitter should also be used.

The differential Data Ready (DR, DRB) signals track the internal propagation delay of output data (typically 2.8 ns).
This enables easy external clock generation for output data acquisition over full temperature range.
Internal output ECL buffers were designed for driving heavy capacitive loads (up to 6 pF) at maximum Data rates.

Output Data format can be determined by two control pins :
LSB_{INV}, which allows the user to invert the five least significant bits.
MSB_{INV}, which allows the most significant bit to be inverted.

Selection among True/Inverted Binary, and True/Inverted Two's Complement output coding, is handled by proper setting of LSB_{INV}, MSB_{INV} control pins. (See TS 83006 Truth Table).

The OVINH (Overflow inhibit) control pin handles output RZ (Return to zero), or NRZ (Non Return to Zero) feature in overflow conditions.
When OVINH is connected to V_{EE} or allowed to float, and V_{IN} exceeds $+V_{REFS}$ sense voltage, overflow bit turns to ECL logic 1, and output bits to ECL logic 0.

For normal operation, (i.e. True Binary, Return to Zero), the LSB_{INV} and MSB_{INV} control pins are to be connected to Ground and OVINH tied at V_{EE} (or allowed to float).

Timing

Output Data change on rising edge of clock signal, (Comparators in latch mode), after Tod (typ = 2.7 ns) output propagation delay. (Pipeline delay is one clock cycle).
Output Data should be latched on rising edge of Data Ready signal (DR), corresponding to falling edge of Clock input command.

Application board layout and power supplies recommendations

Multilayer printed circuit board is recommended, because it enables compact implementation, and allows easy design of low impedance continuous Supply and Ground planes.

Digital input/output signal paths length should be matched and kept short, to avoid propagation delay mismatches, increased output bits times skew, and reflections.

So long as propagation delay along the line is shorter than digital signal rise or fall time, the reflection has little effect on the waveform.
However, if long interconnection lengths cannot be avoided, proper design of transmission line impedance with adapted ECL termination loads has to be observed.

It is important that separate supply planes be retained for Analog and Digital V_{EE}. Proper Supply decoupling by high resonant frequency chip capacitor near the device, and high quality tantalum capacitor at each power supply incoming, is especially recommended.

Packaging

The TS 83006 is packaged in a 68 LCCC chip carrier, with Tungsten-Copper heat spreader.
The top of the LCCC 68 Package (Heat spreader) is internally connected to V_{EE} (Device substrate).
A seal ring is internally connected to ground, which reduces internal coupling and thus improves output noise floor.
Sockets may be used for prototype evaluation, but should be avoided after-wards, because of possible limitations of TS 83006 dynamic performance.

TRUTH TABLE

Step	Input voltage	OV_{INH}	Binary		Two's complement	
			True	Inverted	True	Inverted
			MSB_{INV} (GND) LSB_{INV} (GND)	MSB_{INV} (V_{EE})* LSB_{INV} (V_{EE})*	MSB_{INV} (V_{EE})* LSB_{INV} (GND)	MSB_{INV} (GND) LSB_{INV} (V_{EE})*
00	− 1.000	x	000 000	111 111	100 000	011 111
01	− 0.968	x	000 001	111 110	100 001	011 110
—	—	x	—	—	—	—
—	—	x	—	—	—	—
—	—	x	—	—	—	—
31	− 0.031	x	011 111	100 000	111 111	000 000
32	− 0.000	x	100 000	011 111	000 000	111 111
33	+ 0.031	x	100 001	011 110	000 001	111 110
—	—	x	—	—	—	—
—	—	x	—	—	—	—
—	—	x	—	—	—	—
62	+ 0.938	x	111 110	000 001	011 110	100 001
63	+ 0.969	x	111 111	000 000	011 111	100 000
> 63	+ 1.000	«1»	(0) 111 111**	(0) 000 000**	(0) 011 111**	(0) 100 000**
		«0»	(1) 000 000***	(1) 111 111***	(1) 100 000***	(1) 011 111***

* V_{EE} or floating.
** OV_{INH} (overflow inhibit) = GND
*** OV_{INH} = V_{EE} (or floating). (Overflow bit is always zero except where noted in parentheses).

TYPICAL EVALUATION CIRCUIT

(True binary configuration. Return to zero feature).

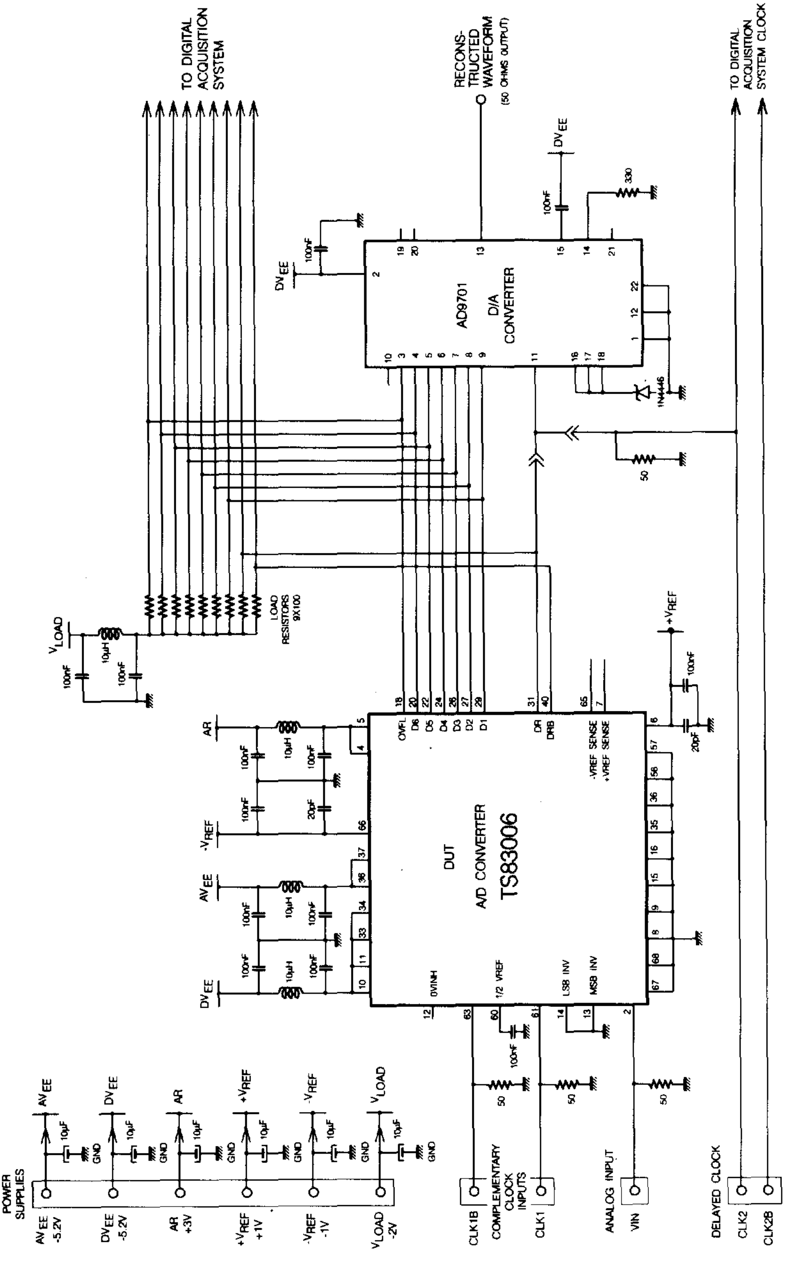


Figure 5

SCHEMATICS

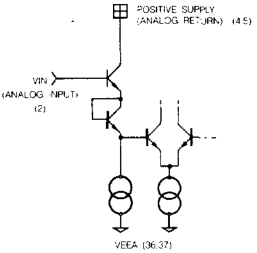


Figure 6 : Equivalent analog input.

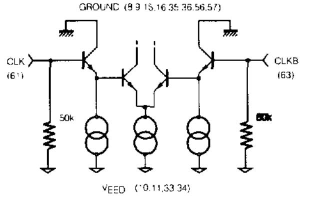


Figure 7 : CLK and CLKB equivalent inputs.

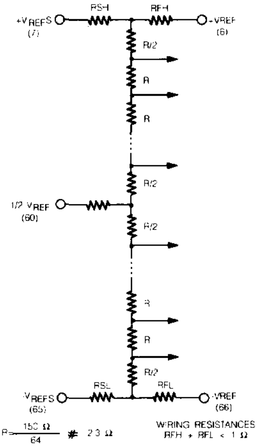


Figure 8 : Reference ladder.

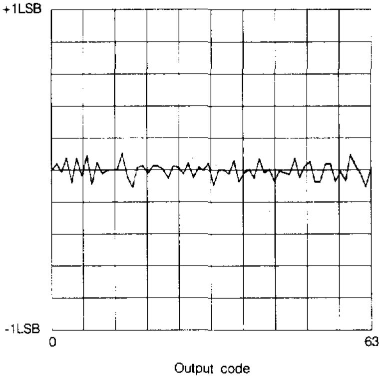


Figure 9 : Differential non linearity.

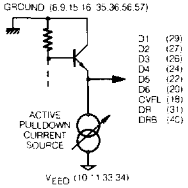


Figure 10 : Equivalent digital outputs.

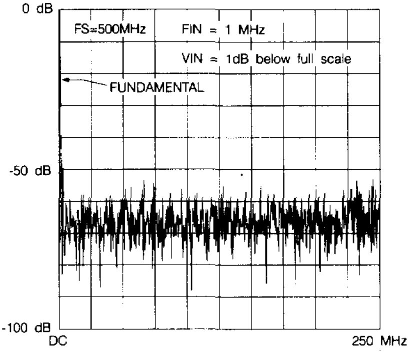


Figure 11 : FFT of TS 83006.

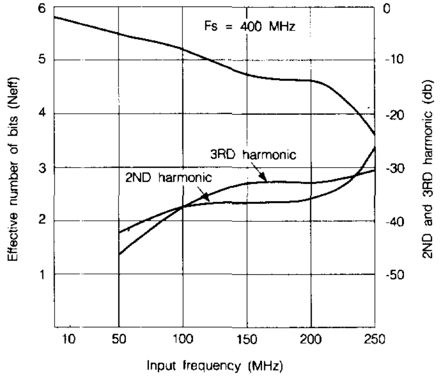


Figure 12 : Number of effective bits, 2nd and 3rd harmonics, versus input frequency.

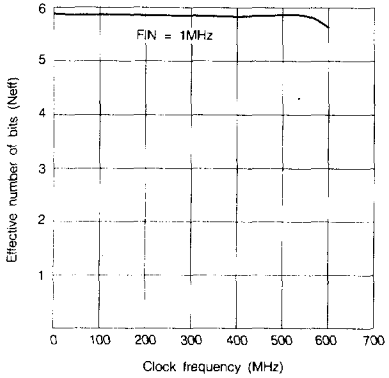


Figure 13 : Number of effective bits versus sampling rate.

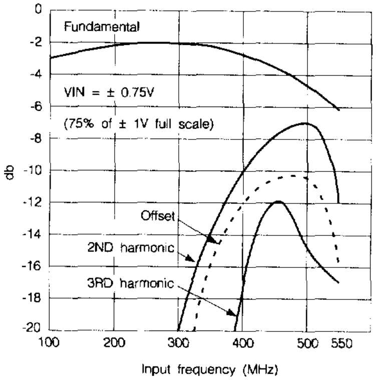


Figure 14 : Harmonics versus input frequency (large signal).

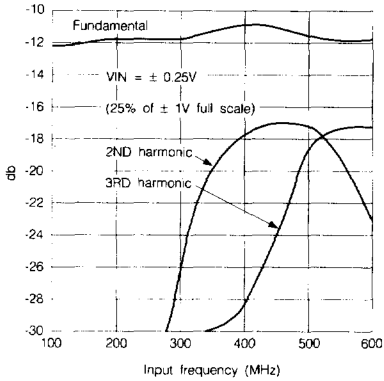


Figure 15 : Harmonics versus input frequency (small signal).

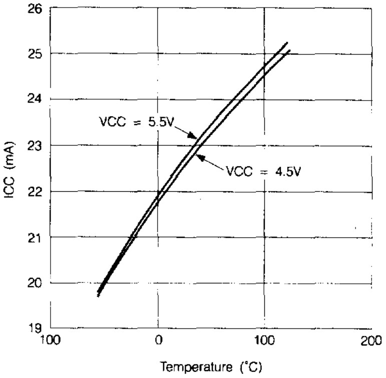


Figure 16 : I_{CC} versus temperature.

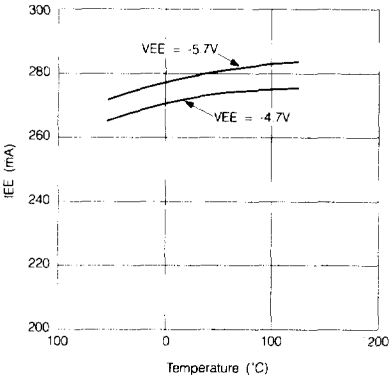


Figure 17 : I_{EE} versus temperature.

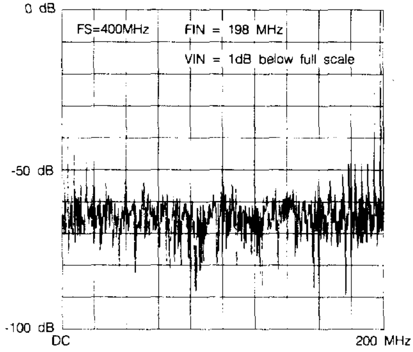


Figure 18 : FFT of TS 83006.

DEFINITION OF TERMS

Analog bandwidth

The analog input frequency at which the fundamental component in the reconstructed output has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis).

Signal to noise ratio (SNR)

The ratio of RMS signal amplitude to the RMS sum of all other spectral components, including significant harmonics except DC.

Total harmonic distorsion (THD)

The ratio of the five most significant harmonic components in the spectrum of the quantized representation, to the fundamental spectral component.

Differential non-linearity (DNL)

The differential non-linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all |DNL (i)|. DNL error specification of less than 1 LSB guarantees that there are no missing output codes, and that the transfer function is monotonic.

Integral non-linearity (INL)

The integral non-linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.

Aperture delay (TA)

The delay between the rising edge of CLK signal and the time at which V_{IN} is sampled.

Aperture uncertainty (JITTER)

The sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.

Pipe line delay (TPD)

The delay of one clock cycle, between two successive rising edges of CLK signal (50 % points).

Output delay (TOD)

The delay between the rising edge of CLK (50 % point) and the – 1.3 V point of a change in output data.

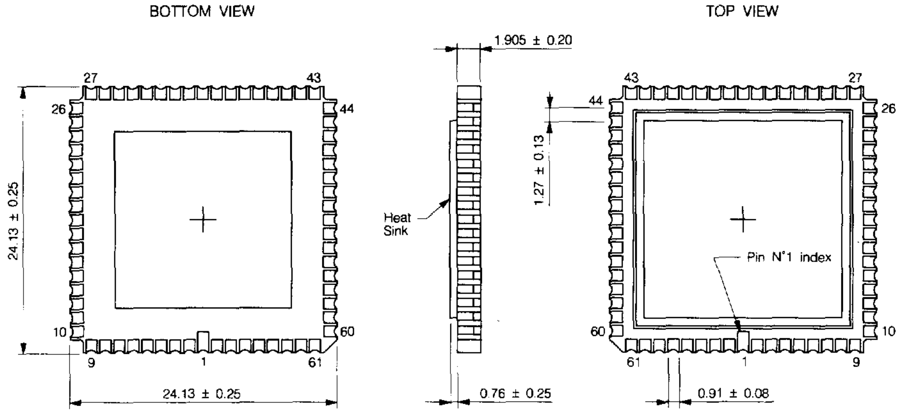
Data ready output delay (TDR)

The delay between the 50 % point of the falling edge of CLK and – 1.3 V point of the leading edge of the data ready pulse.

OUTLINE DIMENSIONS

LEADLESS CERAMIC CHIP CARRIER (LCCC) - SUFFIX E

Dimensions in mm



DIE MECHANICAL INFORMATION : JTS 83006

Pad layout : V444

Pad size : 0.120 × 0.120 mm

Die size : 3.300 × 2.200 mm

Die thickness : 380 μm

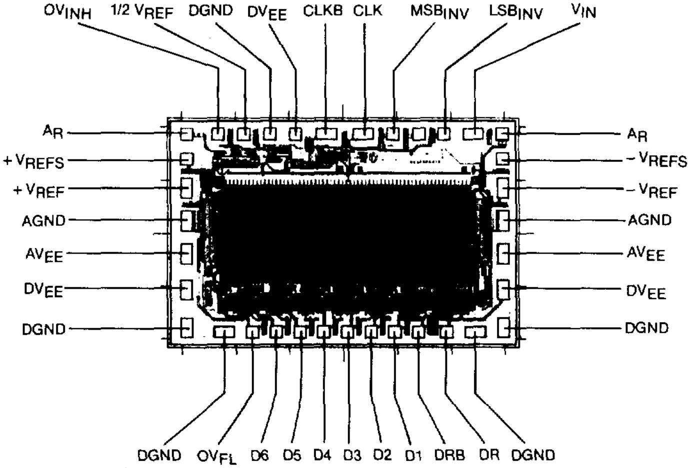
Metallization : Si (Back side)
Al-Si-Ti (Front side)

Passivation : Nitride

Revision : A

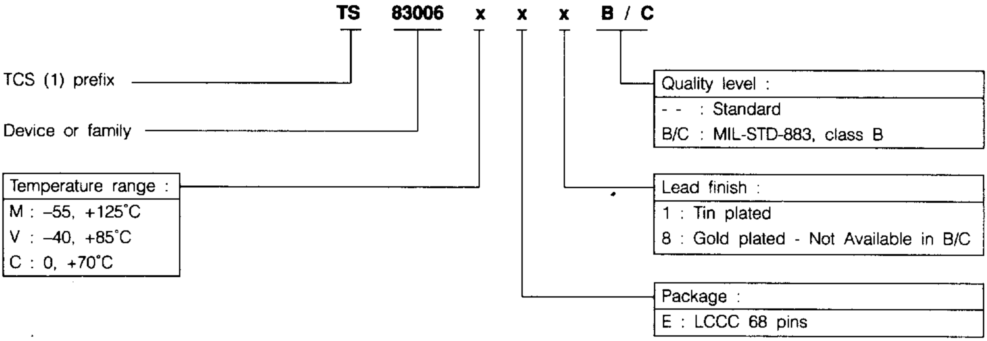
Qualification lot package : LCCC 68

Back side potential : AV_{EE}

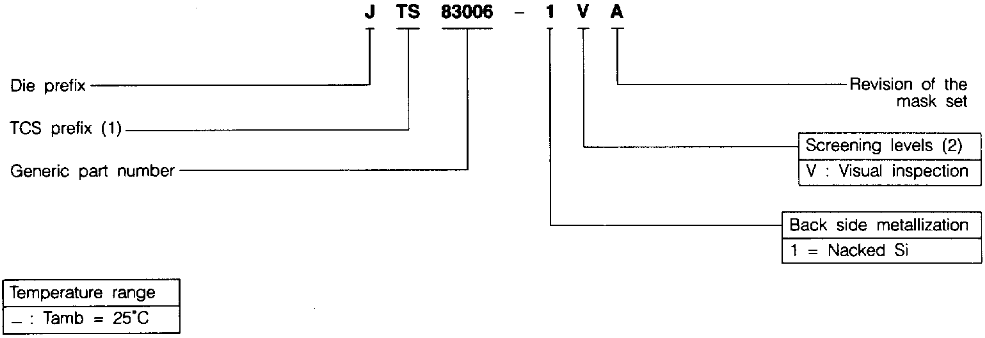


ORDERING INFORMATION

Packaged device



Die form



Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

Note 2 : For availability of the different available versions contact your TCS sales office.