CMOS Digital Integrated Circuit Silicon Monolithic

TZ1200 series

Application Processor Lite *ApP Lite*

Overview

The TZ1200 series is a family of processors based on the high performance 32-bit ARM® Cortex®-M4F RISC processor. The TZ1200 series incorporates 2.2 MB high-speed SRAM and various memory interfaces for external memory.

The TZ1200 series offers a variety of peripherals and functions such as an LCD controller, a 2D Graphics accelerator, a compress and decompress hardware engine for sensor data, eMMC/SDIO controllers, a crypt engine and audio interfaces in addition to USB device, UART, SPI and I2C. The TZ1200 series also incorporates Analog Front End with 24-bit ΔΣADC features. This interface allows the TZ1200 to connect many kinds of analog sensors such as photo diode, eletronode, gas sensor and so on without an external AFE circuit. This contributes to reduce the foot print and the cost of system.

Features

- CPU Core
  - ARM Cortex-M4F running at up to 120 MHz
  - Floating Point Unit (FPU)
  - Memory Protection Unit (MPU)
  - ARM® Thumb®-2 instruction set
- Memories
  - 2.2 MB embedded SRAM
- System Functions
  - Embedded voltage linear and switching regulators for single power supply operation
  - Power-on reset circuit
  - Brown-out detectors
  - Crystal oscillators**:** 12 MHz for main circuits and 32.768 kHz for RTC
  - High precision 12 MHz factory trimmed internal RC oscillator
- Memories Interfaces
  - SPI NOR flash interface
  - SPI NAND flash Interface
  - x2 eMMC/SDIO interfaces
  - External bus interface
- Data converter and Crypt engine
  - Compress and decompress hardware engine
  - Advanced Encryption Standard (AES) engine with 128/192/256-bit key length
  - Hash (SHA256) generation function
  - True random number generator
- Boot system
  - Support booting from SPI NOR or eMMC flash memory
  - Provide user program code protection with the crypt engine
- Graphics and Display
  - LCD display interface compatible with DBI-B, DBI-C and DSI
  - 2D graphics accelerater
- Audio Interfaces
  - Three I2S interfaces
  - One PDM interface
- USB Interface
  - USB 2.0 Device**:** 12 Mbps, 1 port 4 bidirectional endpoints
- Peripherals
  - 120 general purpose IOs (GPIO)
  - Four SPI masters for general purpose
  - Four UART interfaces
  - Two master and slave I2C interfaces support up to 1 Mbps
  - Two 8-channel DMA controllers
  - Watchdog timer
  - Two channels of 32-bit timer and counter
  - Eight channels of 16-bit advanced timer and counter with capture, compare or PWM mode
  - Real-time clock supports calender mode
- Analog Functionality
  - One 12-bit ADC with 16-channel inputs
  - One Analog Front End (24-bit Delta-Sigma ADC) with 4-channel inputs
  - One 12-bit DAC
  - Four LED current drivers
- Single Power Supply
  - Voltage range**:** 1.7 to 3.6 V
- Packages
  - P-UFBGA210-0808-0.4
  - Height 0.6 mm

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Preface

This document will be modified without further notice. Ensure that you refer to the latest version of the document when using the product. For information on the latest version, contact TOSHIBA technical support.

Conventions in this Document

- The numerical values are expressed as follows.
  Hexadecimal number**:** 0xABC
  Decimal number**:** 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary number**:** 0b111 - It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m**:**n].
  Example**:** S[3**:**0] shows four signal names S3, S2, S1, and S0 together.
- The characters surrounded by ***[]*** defines the register.
  Example**:** ***[ABCD]***, ***module.[ABCD].field***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example**:** ***[XYZ1]***, ***[XYZ2]***, and ***[XYZ3]*** to ***[XYZn]***
- The bit range of a register is written like as [m**:**n].
  Example**:** Bit[3**:**0] expresses the range of bits 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example**:** ***[ABCD].EFG*** = 0x01 (hexadecimal), ***[XYZn].VW*** = 1 (binary)
- Word and Byte represent the following bit length.
  Byte**:** 8 bits
  Half word**:** 16 bits
  Word**:** 32 bits
  Double word**:** 64 bits
- Properties of each bit in a register are expressed as follows.
  R**:** Read only
  W**:** Write only
  W1C**:** Write 1 Clear - The corresponding bit is cleared (=0) when "1" is written to this bit.
  W1S**:** Write 1 Set - The corresponding bit is set (=1) when "1" is written to this bit.
  R/W**:** Read and Write are possible.
  R/W0C**:** Read/Write 0 Clear
  R/W1C**:** Read/Write 1 Clear
  R/W1S**:** Read/Write 1 Set
  RS/WC**:** Read Set/Write Clear - Set after read operation, cleared after write operation.
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, don't use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value. In the cases that default is "—," follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "—," follow the definition of each register.

Abbreviation

OD	voltage mode Over Drive
MA	voltage Mode A
MB	voltage Mode B

1. Functional Summary

The TZ1200 series is a family of processors based on the high performance 32-bit Cortex-M4F RISC processor. The TZ1200 series incorporates 2.2 MB high-speed SRAM and various memory interfaces for external memories. The Cortex-M4F processor features of a floating point unit which supports ARM single precision data processing instructions and data types, and it also provides full set of DSP instructions, a memory protection unit and a flexible interrupt controller.

The TZ1200 series provides selection of the power supply voltage to fit its operating frequency. Optimized low power consumption in applications can be achieved by using its power saving modes.

The TZ1200 series has high-speed and low-power 2.2 MB of SRAM which is used to execute program codes, store data and is utilized for graphics acceleration. CPU can access to the main SRAM without wait state for read and write operations. SRAMs are divided into multiple power domains, and each SRAM domain can be retained in low power Retention mode.

The TZ1200 series also incorporates various external memory interfaces such as SPI NOR Flash, SPI NAND Flash and eMMC/SD. These interfaces enables to store large amount of sensing data to external memories or storages in combination with a hardware compression and decompression engine.

An Cryptographic engine and a random number generator are incorporated for a security function. The AES complies with FIPS (Federal Information Processing Standard) Publication 197, Advanced Encryption Standard. This provides encryption and decryption features with the minimum resource of the CPU. The Cryptographic engine also has SHA-256 hash generation engine. SHA-256 complies with FIPS 180-2 (Secure Hash Standard). The random number generator has passed the random number test of NIST SP800-22 (National Institute of Standards and Technology Special Publication 800-22), as well as a key generator for security features.

The TZ1200 series incorporates an LCD controller interface which is compliant to MIPI DBI type B, type C and DSI standards. External LCD controllers can be directly connected to one of these interfaces. 2D Graphics accelerator supports transformation and rotation with anti-aliasing as well as basic functions of BitBLT, alpha blending and raster operations.

The TZ1200 series incorporates audio interfaces providing a way to record or play back audio signal with external codec devices.

The TZ1200 series supports a variety of peripheral interfaces such as USB device, UART, SPI, and I2C.

The DMA controls data transmission between an SRAM and a peripheral such as the UART or between a part of the SRAM and another part of the SRAM. SRAM controller has another data transmission engine which enables the data transmission between two parts in the SRAM not over the data buses.

The TZ1200 series also incorporates various analog circuits such as high-resolution ΔΣADC with configurable AFE, a DAC with a sine wave generator and LED current drivers. These analog circuits provide measures of biomedical sensing in a health care applications. The configurable AFE consists of a configurable amplifier, a programmable gain amplifier and a rectifier. The configurable amplifier has two types of mode as instrumentation amplifier mode for voltage-output sensors or trans-impedance amplifier mode for current-output sensors. The ΔΣADC with configurable AFE allows the TZ1200 to be connected to a photo diode for pulse sensing directly without an external analog band-pass filter, a photoelectric sensor and a wide variety of sensors, such as a gas sensor. The DAC can generate sine wave able to be utilized in impedance measurement. LED current drivers enable direct driving of LEDs for pulse sensing. These functions contribute to reduce the foot print and the cost of the sensing system.

Product lineups

TZ1201XBG**:** with user program protection for prototyping and mass production

2. Features

2.1. CPU Core

- ARM Cortex-M4F processor
  - Instruction set Architecture: ARMv7E-M architecture
    - Single Precision floating point unit with IEEE 754 compliant
    - Supports SIMD and MAC DSP extension instructions
    - Thumb2 instruction set
  - Memory protection unit
  - Integrated bit manipulation instructions & bit banding
  - Operating Frequency: up to 96 MHz under normal condition (up to 120 MHz with Over Drive)
    - Debug function: ARM CoreSight component (v7 debug architecture)
      - Serial Wire Debug Interface (SWD)
      - Flash Patch and Breakpoint (FPB) unit for breakpoints and code patches
      - Data Watch point and Trace (DWT) unit for watch points, data tracing and system profiling
      - Instrumentation Trace Macrocell (ITM) unit for printf() style debugging
      - Embedded Trace Macrocell (ETM) unit for debugger to reconstruct program execution
      - Trace Port Interface Unit (TPIU) for bridge ETM and ITM to a data stream with SWO (Serial Write Output) or 4 trace data ports

2.2. Memories

- Main SRAM (SRAMCM)
  - Memory size: 1152 KB
  - Connected to Main bus
    - can work at maximum 96 MHz in normal mode (120 MHz in overdrive mode)
    - no wait state path for CPU code/data fetch
  - Support SRAM to SRAM data transmission without DMAC within SRAMCM
- Graphic SRAM (SRAMCG)
  - Memory size: 1024 KB connected to graphics sub-system bus
  - Connected to Graphics bus
    - can work at maximum 48 MHz in normal mode
  - Accessible from graphics sub-system with higher priority than other, etc. CPU.
- Work SRAM (SRAMCS)
  - Memory size: 64 KB
  - Connected to Sub bus
    - can work at maximum 48 MHz in normal mode

2.3. System Control

- Embedded linear and switching voltage regulators (1.3 V, 1.2 V, 1.1 V, or 0.9 V)
- Embedded LDO (0.9 V)
- Power-on Reset Circuit
- Brown-out Detectors
- High precision 12 MHz internal Silicon oscillator
- 12 MHz Crystal resonator
- 32 kHz Crystal oscillator / resonator for RTC function
- Analog PLL up to 120 MHz with reference clock 12 MHz
- Digital PLL up to 120 MHz with reference clock 32 kHz
- Power Management Unit (PMU)
  - Control internal clocks and reset signals
  - Manage various low power consumption modes.

2.4. External Memory and Storage Interfaces

- SPI Flash Memory Controller (SPIFC)
  - Supported devices: serial NOR and serial NAND flash memories
  - Support single and quad commands
  - Two functional modes:
    - Direct mode:
      An output buffer of a flash memory array is memory-mapped and accessible by the system.
    - Indirect mode:
      Programmable commands (instruction, address, dummy cycles and data phase)
      An interrupt is generated when an operation completes

- SPI NOR Flash Memory Controller (SPINOFC)
  - Supported device: serial NOR flash memory and serial NAND flash memories
    - Single and quad commands
    - Up to 48 MHz on the serial clock.
  - Security function:
    - Use program code protection
    - Read and decrypt an encrypted user program code simultaneously in Indirect mode
  - Boot function:
    - Support NOR flash memory
    - Read command: single read
    - Frequency of the serial clock: 12 MHz
    - Support 3-byte addressing
    - 32 KB pre-load function
    - Pre-load supports reading and decrypting an encrypted user program code simultaneously
  - Two functional modes:
    - Direct mode:
      An output buffer of the flash memory array is memory-mapped and accessible by the system.
    - Indirect mode:
      Programmable commands (instruction, address, dummy cycles and data phase)
      Supports DMA transmission between the SRAMCM
      An interrupt is generated when an operation completes

- eMMC/SD Card/SDIO host interfaces (EMMC)
  - Support eMMC Ver. 4.51, SD Ver. 3.0 standard
  - Two ports are configurable: up to 8-bit and 4-bit data width supported respectively
  - Data transmission rate: up to 48 MHz (48 MB/s at 8-bit mode)
  - Support Default Speed mode & High Speed mode (SD Card / SDIO)
  - Support Backward Compatibility mode and High Speed SDR mode (eMMC)
  - Internal DMA Controller
  - Boot function:
    - Support EMMC flash memory

- External Bus Interface (EBIF)
  - Support asynchronous and static memory interfaces as an external bus interface.
    - Data bus width: 16 bits or 8 bits.
    - Address bus width: 22 bits.
    - Number of chip-enable signals: 2.
    - Number of byte-enable signals: 2.
    - Other control signals: One output-enable, one write-enable and one address-valid signals.
  - Supported protocols: single read, single write and page read.

2.5. Data Converter and Security Function

- Compressor and Decompressor (TZCP)
  - Lossless data compression and decompression engine with built in DMAC
  - Supported data format: N bytes x M elements data array (N = 1 to 4, M = 1 to 8)
  - Target data characteristic: time-series data of various sensing devices
  - Performance: up to 24 MB/s

- Cryptographic Accelerator (CRA)
  - AES encryption and decryption
    - Compliant with FIPS 197 (Advanced Encryption Standard)
    - Supported 128, 192, 256-bit key length
    - Supported 3-block cipher modes of operation (ECB, CBC, CTR)
  - SHA-256 hash generation
    - Compliant with FIPS 180-2 (Secure Hash Standard)
  - Dedicated DMA engine
  - Performance: up to 30 MB/s (when CPU is running with 48 MHz)

- True Random Number Generator (RNG)
  - Generate 32-bit true random number
  - NIST SP800-22 (NIST special publication 800-22) passed

2.6. Graphics and Display

- LCD controller
  - Interface: MIPI DBI Type B (16/9/8 bits), Type C (option1/option3) or DSI (x2 lanes)
  - RGB-bit: RGB565, RGB666 or RGB888
  - Picture size: up to 480 × 320
  - Frame rate: up to 30 fps (480 × 320) or 60 fps (320 × 240)

- 2D Graphics Accelerator (GFX)

  The GFX for performing 2D graphics acceleration consists of the following graphics engines.
  - Bit bliting Engine: BitBLT, alpha blending, raster operation, gradient generation
  - Transformation Engine: high flexibility image transformation
  - Rotation Engine: scaling, rotation
  - Drawing Engine: anti-aliased line and triangle drawing
  - Frame Buffer Color Format:
    ARGB1555, RGB565 or ARGB8888 (DBIBC does conversion from Frame Buffer Format to DBI interface Color Format.)

2.7. Audio Interfaces

- I2S interfaces (I2S)
  - Three channels: Two for input or output (I2S0, I2S1), one for input only (I2S2)
  - Selectable master or slave
  - Format: I2S stereo, LR stereo, PCM monaural
  - Sampling frequency: 48 kHz, 44.1 kHz, 32 kHz, 24 kHz, 22.05 kHz, 16 kHz or 8 kHz
  - Internal PDM-I2S converter (I2S2 only)

- PDM interface (PDM)
  - Receive PDM format audio data
  - PDM to I2S data conversion and transfer data to I2S2 internally
  - Sampling frequency: 48 kHz, 24 kHz, 16 kHz or 8 kHz

2.8. Universal Serial Bus Interface

- USB device controller (USB)
  - Compliant with Universal Serial Bus Specification revision 2.0
  - Support Full Speed (12 Mbps)
  - One port, four endpoints
    Each endpoint 1‐3 is configurable as interrupt or bulk transfer mode
  - Internal DMA Controller

2.9. Peripherals

- GPIO
  - Up to 120 Pins
  - Configurable each pin as input or output separately
  - Interrupt generation capability from a transition or level condition
  - Programmable pull-up and pull-down function
  - Programmable drive current

- SPI Master (SPIM)
  - Four channels
  - SPIM0 and SPIM1 have three chip select signals. SPIM2 and SPIM3 have one chip select signal.
  - Serial Clock (SCLK) frequency**:** up to 12 MHz
  - Supported format**:** Motorola SPI, Texas Instruments SSP or National Semiconductor

- UART (UART)
  - Four channels
  - FIFO Depth
    - 16 of RX FIFO and 16 of TX FIFO
  - Programmable baud rate generator
    - Data rate**:** up to 1 Mbps (UART0,1,2), 3 Mbps (UART3)
    - Division of reference clock by (1 × 16) to (65535 × 16)
  - Support hardware flow controls**:** CTS and RTS
  - Fully-programmable serial interface characteristics
    - Data can be 5, 6, 7, or 8 bits
    - Even, odd, stick, or no-parity bit generation and detection
    - 1 or 2 stop bit generation

- I2C
  - Two channels
  - Transmission mode**:** Standard mode (100 kbps), Fast mode (400 kbps) or Fast mode plus (1 Mbps)
  - Master or slave I2C operation
  - 7-bit or 10-bit addressing
  - 7-bit combined format transfers
  - Bulk transfer mode
  - FIFO Depth
    - 6 of RX FIFO and 6 of TX FIFO

- DMA Controller (SDMAC)
  - 16 channels
    Each channel has source and destination pair
  - Programmable source and destination addresses
    - Addressing mode is selectable from increment, decrement or no change
    - Handshaking interfaces for source and destination peripherals
      SPI, UART, I2C, I2S, DACC, AFEZ, ADC12, ADVTMR

- Timer (TMR)
  - Two channels
  - 32-bit down counter
    - Count mode is selectable rom 32-bit or 16-bit
  - Operation Mode
    - One shot timer mode
    - Periodic timer mode
    - Free running timer mode
  - Pre-scale unit generating timer clock
    - (1x, 1/16 or 1/256)

- Advanced Timer (ADVTMR)
  - Eight channels
  - 16-bit down Counter
    - Count mode is selectable from 16-bit or 8-bit
    - Input capture function for each channel
    - Output compare function for each channel
  - Operation Mode
    - One shot timer mode
    - Periodic timer mode
    - Free running timer mode
  - Pre-scale unit generating timer clock (1×, 1/2, 1/4, 1/8, 1/32, 1/128, 1/512 or 1/1024)
  - Timing selection of input capture (Pulse, Rising edge, Falling edge or both edges)
  - PWM (Pulse Width Modulation) operation that uses output compares function

- Watch Dog Timer (WDT)
  - 32-bit Timer with interrupt and reset when timeout

- Real Time Clock (RTC)
  - Clock (hour, minute and second)
  - Calendar (month, week, date and leap year)
  - BCD format for clock and calendar data
  - Selectable output format from 12 (am/pm) or 24-hour display
  - Time adjustment + or -30 s
  - Alarm interrupt
  - Periodic interrupt
  - Two independent interval timer/counter

2.10. Analog Functionality

- 12-bit A/D Convertor (ADC12)
  - Successive approximation type
  - 12-bit resolution
  - Conversion time**:** 19 cycles at 1 to 16 MHz
  - Data Rate**:** Max. 667 ksps (Sequential conversion cycle is 24 cycles)
  - 16 channels of analog inputs switcher
  - Selectable conversion mode (Single/One-time scan or Cyclic scan)
  - Double buffer for each channel

- Analog Front End with 24-bit A/D converter (AFEZ)
  - Two independent Op-Amp for current excitation and/or voltage drive.
  - Four channels of differential analog inputs switcher
    - Internal Bias control for each channel
    - Current Bias control for each channel
  - Configurable AFE
    - Configurable amplifier
      - Current input mode (Trans-Impedance Amplifier)
      - Voltage input mode (Instrumentation Amplifier**:** 1× to 4×)
    - Programmable Gain Amplifier**:** 1× to 32×
    - Rectifier**:** Rectifies AC signal to DC signal
  - Delta-Sigma A/D converter
    - 24-bit resolution
    - Conversion time**:** selectable from 4132, 1060, 548 or 292 cycles
    - Data Rate**:** Max.13.6 ksps (Sequential conversion cycle is 294 cycles)
    - Selectable conversion mode (Single, One-time scan, Cyclic scan or advanced scan mode)
    - 16 of FIFO Depth for each channel

- Digital to Analog Converter (DACC)
  - 12-bit resolution
  - One channel of single-end analog output
  - Data Rate**:** up to 4 Msps
  - Two operation modes**:**
    - Programmable voltage output
    - Sine wave output (1 Hz to 500 kHz)

- LED Current Driver (LEDC)
  - Four current drive output pins
  - 8-bit resolution programmable current source driver up to 25 mA at each pin
  - Drive current can be doubled by using two drivers jointly.
  - Configurable current path using internal switch matrix. H-Bridge configuration can be selected.

3. Block Diagram

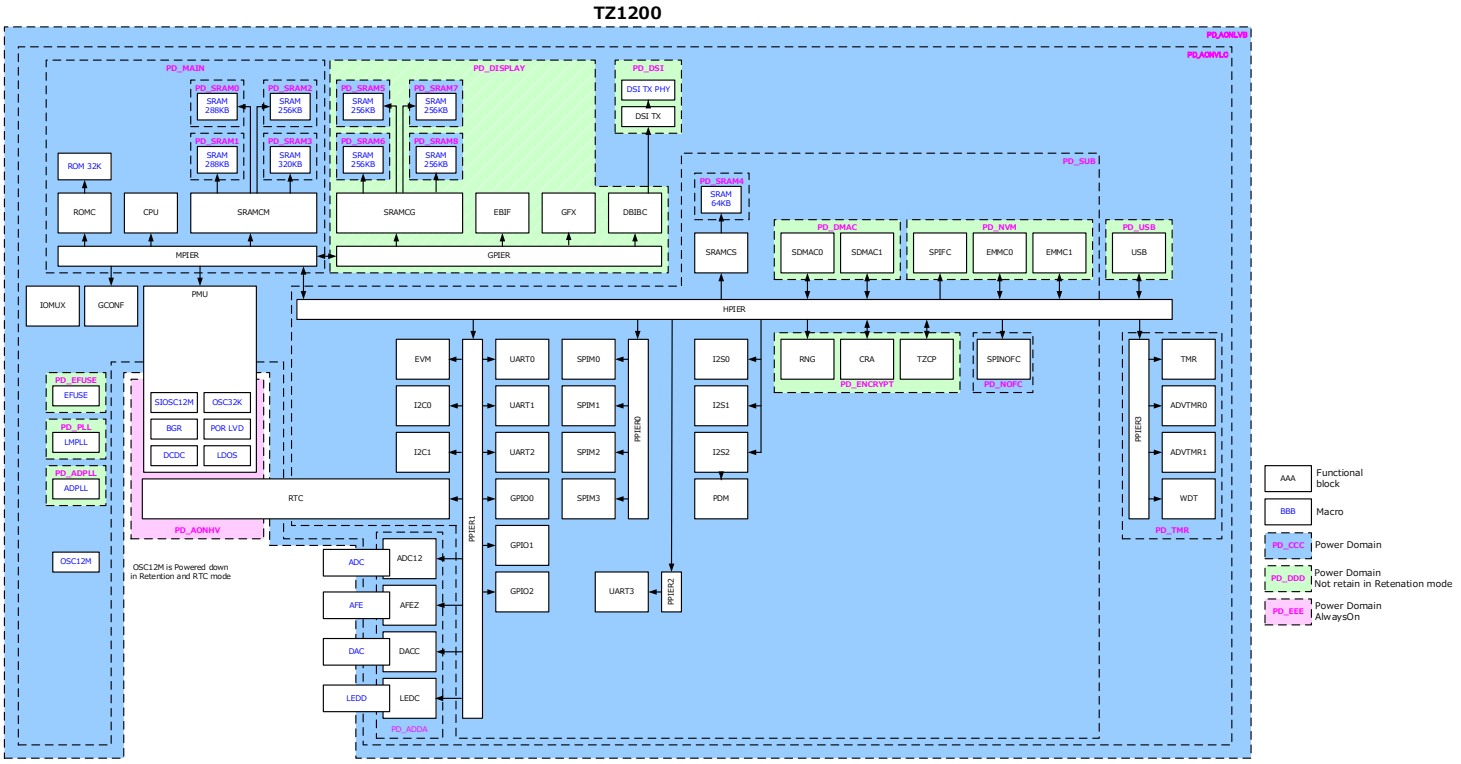


Figure 3-1 Block Diagram

4. Operation

4.1. Power Supply Overview

Figure 4-1 shows a simple example of power supply composition with the TZ1200 series.

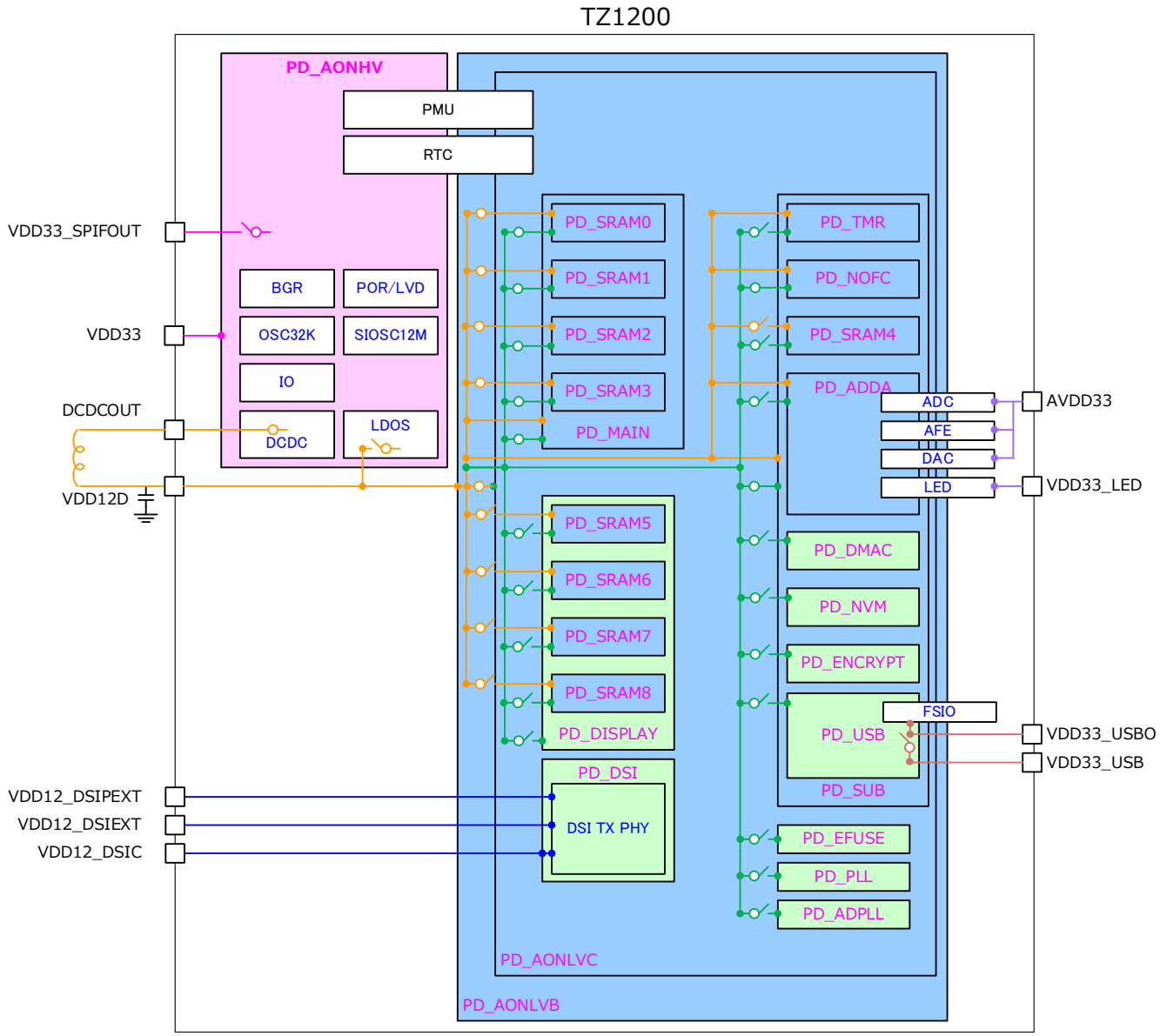


Figure 4-1 TZ1200 series Power Supply Overview (3.0 V < VDD33)

Embedded regulator (DCDC) and Embedded LDO (LDOS) supply power to internal logic blocks. PMU selects either DCDC or LDOS according to Power Mode. In case not using DSI display interface, only single power supply 3.3 V is required.

TZ1200 provides a power switch to control power supply for an external SPI flash memory in addition.

4.2. Clock and Reset Overview

The overview of the TZ1200 series clock and reset composition is shown in Figure 4-2.

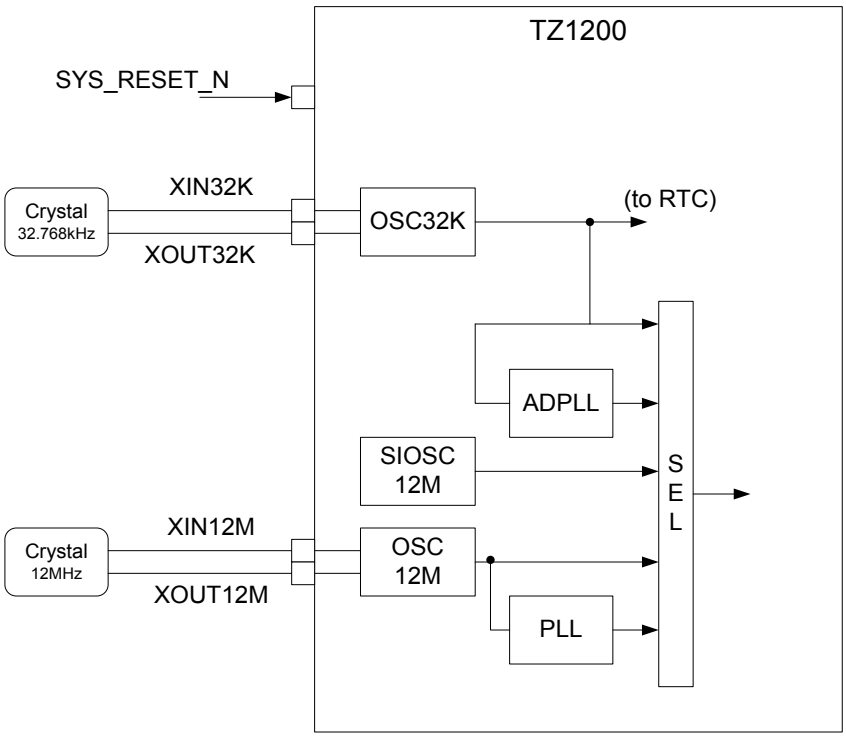


Figure 4-2 TZ1200 series Clock and Reset Overview

4.2.1. Clock Sources

One of the following five clocks can be the clock sources of internal systems.

- OSC32K
  - Clock oscillator with an external crystal oscillator / resonator.
  - Generates 32.768 kHz
- SIOSC12M
  - Clock generated by the embedded silicon oscillator.
  - Generates 12 MHz
- ADPLL
  - Clock output from a PLL whose reference clock is OSC32K.
  - Generates up to 120 MHz
- OSC12M
  - Clock oscillator with an external crystal resonator.
  - Generates 12 MHz
- PLL
  - Clock output from a PLL whose reference clock is OSC12M.
  - Reference clock necessary to be active when PLL is selected.
  - Generates 12, 24, 36, 48, 96 or 120 MHz

4.3. Power Management Summary

TZ1200 series supports multiple power configurations which allow a user application to achieve a required feature set with as low power consumption as possible. Power Management Unit (PMU) provides several modes to reduce power consumption.

- Power Mode to reduce power consumption by
  - stopping all or part of clocks
  - controlling power domain state (On, Off or Retention)
  - controlling Voltage Mode
- Voltage Mode to support voltage scaling and regulator selection.

Following diagram shows the combination of Power Mode and Voltage Mode.

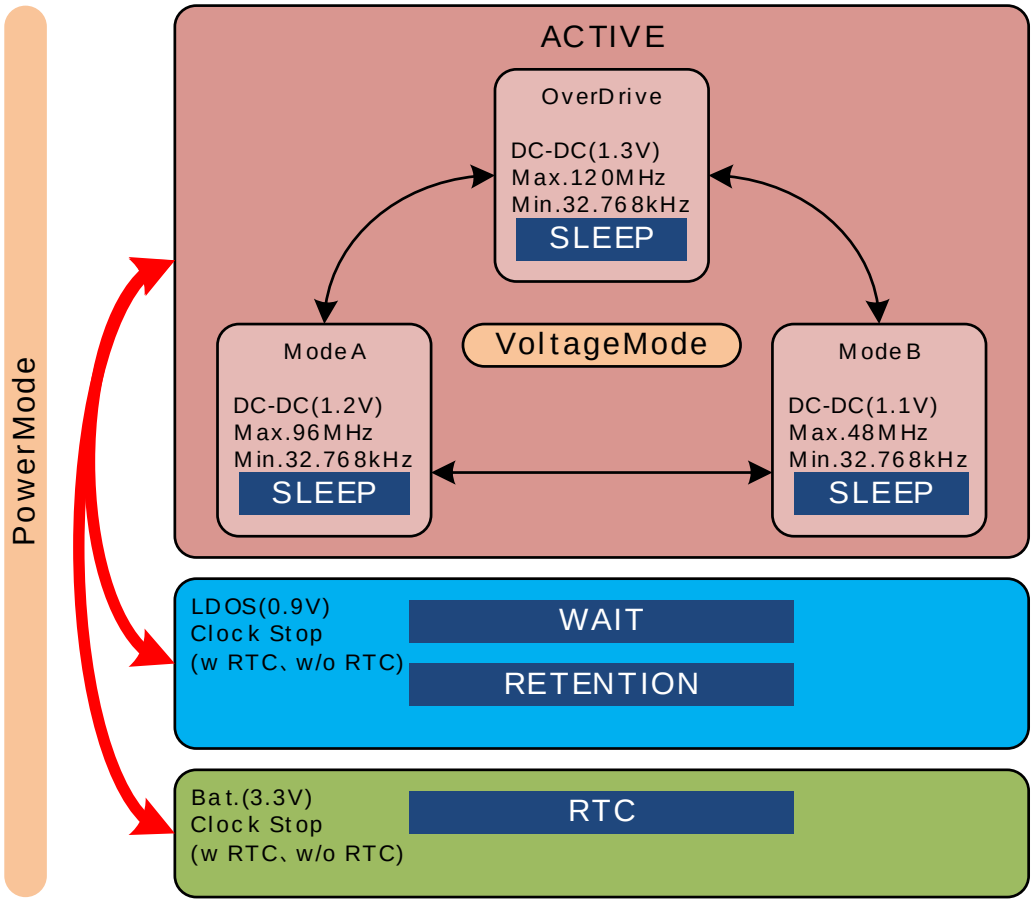


Figure 4-3 Power Mode and Voltage Scaling Overview

Table 4-1 MCU Power Mode and Voltage Mode overview

PowerMode	Description	Voltage Mode		CPU Clock	Bus and peripheral Clock	RTC Clock	Power Domain
ACTIVE	Active Mode	ModeA ModeB Overdrive	1.2 V 1.1 V 1.3 V	Run	Run	Run	All ON (*2)
SLEEP	CPU is stopped by WFI Peripherals are either stopped or running (selectable) Fastest wake up operation	ModeA ModeB Overdrive	1.2 V 1.1 V 1.3 V	Stop	Run / Stop (*1)	Run	All ON (*2)
WAIT	All clock sources except SIOSC12M are stopped. CPU is stopped by WFI Peripherals are either stopped or running (selectable) RTC running with the 32 kHz clock if enabled.	—	0.9 V	Stop	Run / Stop (*1)	Run / Stop	All ON (*2)
RETENTION	Lowest power configuration where the logic is retained except some domain	—	0.9 V	Stop	Stop	Run / Stop	RET or OFF (*3)(*4)
RTC	1.2 V domain is power off, 3.3 V domain kept powered with running 32 kHz clock.	—	—	Stop	Stop	Run / Stop	PAONHV: ON Other: OFF

*1: Run or Stop is configurable for each peripheral.
*2: Possible to shut off a part of power domain.
3: Possible to shut off all power domains except PAON domain. (RET means Retention)
*4: Domain PDMAC, PENCRYPT, PDISPLAY, PUSB, and PNVM are OFF, other domains are RET.

5. Pin Description

5.1. Pin Alignment (Top View)

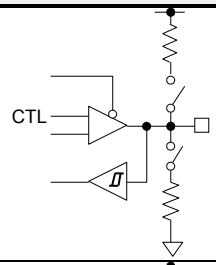
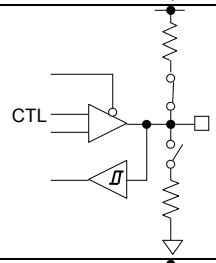
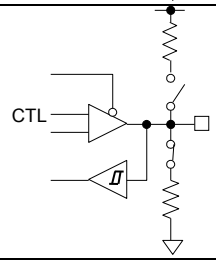
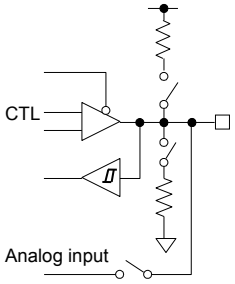
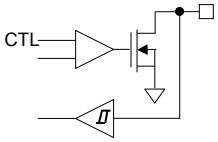
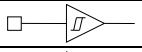
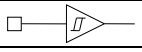
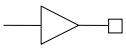
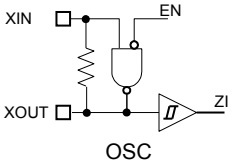
Lower	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	PD03	PD02	PD01	PD00	PB11	PB06	PB02	VDD33_SPIFOUT	PH02	PH07	PH12	PC06	PC03	PC01	VDD33_USBO	USB_DP	USB_DM
B	PD07	PD06	PD05	PD04	PB12	PB07	PB03	PH00	PH03	PH08	PH13	PC07	PC04	PC02	PC00	VSS33_USB	VDD33_USB
C	PD11	PD10	PD09	PD08	PB13	PB08	PB04	PH01	PH04	PH09	PH14	PH17	PC05	ILEDB0	ILEDB1	VDD33_LED	VDD33_LED
D	PD15	PD14	PD13	PD12	PB14	PB09	PB05	PB00	PH05	PH10	PH15	PH18	VPGM	ILEDA1	ILEDA0	VSS33_LED	VSS33_LED
E	PD19	PD18	PD17	PD16	PB15	PB10	VDD12D	PB01	PH06	PH11	PH16	VSSC	VDD33	ZAI1	ZAI0	DAOUT	AVSS33
F	VSSC	VSSC	VSSC	PD20	VDD33	VSSC								RLDO	ZAO	ZAI2	AVDD33
G	VDD12_DSIEXT	DSI_DP0	DSI_DN0											AO1P	RLDI2	RLDI1	AVDD33
H	VDD12_DSIPEXT	DSI_CP	DSI_CN		TOP View									AO1N	AO0P	AO0N	AVSS33
J	VDD12_DSIC	DSI_DP1	DSI_DN1											AVSS33	AI0N	AI0P	VREFL
K	VSSC	VSSC	VSSC											AVSS33	AI1N	AI1P	VREFH
L	PE03	PE02	PE01	PE00										AVSS33	AI2N	AI2P	AIN0
M	PE07	PE06	PE05	PE04										AVSS33	AI3N	AI3P	AIN1
N	PE12	PE11	PE10	PE09	PE08										VSSC	VSSC	VSSC
P	PF01	PF00	PE15	PE14	PE13	VDD33	VSSC	PA17	PA03	PA07						BOOTMODE1	BOOTMODE2
R	PF06	PF05	PF04	PF03	PF02	PA09	PA12	PA15	PA02	PA06	PG02	PA00	TEST	CLK32K_OUT	VSSC	BGR_OUT	BOOTMODE0
T	PF11	PF10	PF09	PF08	PF07	PA08	PA11	PA14	PA01	PA05	PG01	PA16	XOUT_12M	XIN_32K	SYS_RESET_N	POR_EN	VDD33
U	VSSC	PF16	PF15	PF14	PF13	PF12	PA10	PA13	PA18	PA04	PG00	PG03	XIN_12M	XOUT_32K	POR_OUT	DCDCOUT	VDD12D

Figure 5-1 Pin Alignment

5.2. IO pin description

IO pin attribute shows that the grouping of the pins classified by their structures and power type.

Table 5-1 IO pin Attribute

Attribute	Explanation	Structure
BDSPZ	Bi-directional buffer, 2, 4, 6 or 8 mA drive (at 3.3V), Schmitt trigger LVCMOS level input with programmable pull-up and pull-down resistors. Supply voltage of pull-up resistor is VDD33.	
BDSPU	Bi-directional buffer, 2, 4, 6 or 8 mA drive (at 3.3V), Schmitt trigger LVCMOS level input with programmable pull-up and pull-down resistors. (By default, pull-up resistor is ON) Supply voltage of pull-up resistor is VDD33.	
BDSPD	Bi-directional buffer, 2, 4, 6 or 8 mA drive (at 3.3V), Schmitt trigger LVCMOS level input with programmable pull-up and pull-down resistors. (By default, pull-down resistor is ON) Supply voltage of pull-up resistor is VDD33.	
BDSPAZ	Bi-directional buffer, 2, 4, 6 or 8 mA drive (at 3.3V), Schmitt trigger LVCMOS level input with programmable pull-up and pull-down resistors, and analog input functionality Supply voltage of pull-up resistor is VDD33.	
BDSOD	Bi-directional buffer, 4 mA drive, Open Drain output, Schmitt trigger, 5 V Tolerant LVCMOS level input	
IS	Schmitt Trigger LVCMOS Input Buffer	
IS5	Schmitt Trigger, 5 V Tolerant LVCMOS Input Buffer	
O2	Output Buffer, 2 mA Output	
OSC	Oscillator buffer	
USB-IO	Receiving and transporting for USB differential data	—
POWER	Digital power supply	—
GND	Digital GND	—

Attribute	Explanation	Structure
ANALOG	Analog signal	—
A-POWER	Analog power supply	—
A-GND	Analog GND	—
OTHER	Other than above	—

5.3. Pin Name and Signal Description

Table 5-2 TZ1200 series Pins

Ball No.	Pin name	Attribute	I/O	Explanation
T13	XOUT_12M	OSC	IO	Oscillator output for System clock (12 MHz)
U13	XIN_12M	OSC	In	Oscillator input for System clock (12 MHz)
U14	XOUT_32K	OSC	IO	Oscillator output for RTC clock (32 kHz) Also used as an optional external clock input.
T14	XIN_32K	OSC	In	Oscillator input for RTC clock (32 kHz)
R14	CLK32K_OUT	O2	Out	Clock supply (32 kHz)
T15	SYS_RESET_N	IS	In	System reset input
U15	POR_OUT	O2	Out	Power On Reset output
T16	POR_EN	IS	In	Pin for test, connect to VDD33 in application.
R17	BOOTMODE0	IS	In	Boot mode select 0
P16	BOOTMODE1	IS	In	Boot mode select 1
P17	BOOTMODE2	IS	In	Boot mode select 2
R12	PA00	IS5	In	Multiple function I/O (GPIO0_0, Wakeup)
T9	PA01	BDSPZ	IO	Multiple function I/O (GPIO0_1, Wakeup)
R9	PA02	BDSPZ	IO	Multiple function I/O (GPIO0_2, Wakeup)
P9	PA03	BDSPZ	IO	Multiple function I/O (GPIO0_3, Wakeup)
U10	PA04	BDSPZ	IO	Multiple function I/O (GPIO0_4, Wakeup)
T10	PA05	BDSPZ	IO	Multiple function I/O (GPIO0_5, Wakeup)
R10	PA06	BDSPZ	IO	Multiple function I/O (GPIO0_6, Wakeup)
P10	PA07	BDSPZ	IO	Multiple function I/O (GPIO0_7, Wakeup)
T6	PA08	BDSPZ	IO	Multiple function I/O (GPIO0_8, Wakeup)
R6	PA09	BDSPZ	IO	Multiple function I/O (GPIO0_9, Wakeup)
U7	PA10	BDSPZ	IO	Multiple function I/O (GPIO0_10, Wakeup)
T7	PA11	BDSPZ	IO	Multiple function I/O (GPIO0_11, Wakeup)
R7	PA12	BDSPAZ	IO	Multiple function I/O (GPIO0_12, AFEZ_SYNC0, PWM0 / CAPTURE0, DBG_TRACEDATA2, AIN2)
U8	PA13	BDSPAZ	IO	Multiple function I/O (GPIO0_13, AFEZ_SYNC1, PWM1 / CAPTURE1, DBG_TRACEDATA1, AIN3)

Ball No.	Pin name	Attribute	I/O	Explanation
T8	PA14	BDSPAZ	IO	Multiple function I/O (GPIO0_14, AFEZ_SYNC2, PWM2 / CAPTURE2, DBG_TRACEDATA0, AIN4)
R8	PA15	BDSPAZ	IO	Multiple function I/O (GPIO0_15, DBG_SWV, AFEZ_SYNC3, PWM3 / CAPTURE3, DBG_TRACECLK, AIN5)
T12	PA16	BDSOD	In/OD	Multiple function I/O (GPIO0_16)
P8	PA17	BDSPZ	IO	Multiple function I/O (GPIO0_17, I2C0_SCL)
U9	PA18	BDSPZ	IO	Multiple function I/O (GPIO0_18, I2C0_SDA)
D8	PB00	BDSPZ	IO	Multiple function I/O (GPIO1_0, SPIM0_CS0_N, UA1_RXD, I2S0_BCK)
E8	PB01	BDSPZ	IO	Multiple function I/O (GPIO1_1, SPIM0_CLK, UA1_TXD, I2S0_LRCK)
A7	PB02	BDSPAZ	IO	Multiple function I/O (GPIO1_2, SPIM0_MOSI, UA1_CTS_N, I2S0_DI, AIN6)
B7	PB03	BDSPAZ	IO	Multiple function I/O (GPIO1_3, SPIM0_MISO, UA1_RTS_N, I2S0_DO, AIN7)
C7	PB04	BDSPZ	IO	Multiple function I/O (GPIO1_4, SPIM2_CS_N, SPIM0_CS0_N, SPIM1_CS0_N)
D7	PB05	BDSPZ	IO	Multiple function I/O (GPIO1_5, SPIM2_CLK, SPIM0_CLK, SPIM1_CLK)
A6	PB06	BDSPZ	IO	Multiple function I/O (GPIO1_6, SPIM2_MOSI, SPIM0_MOSI, SPIM1_MOSI)
B6	PB07	BDSPZ	IO	Multiple function I/O (GPIO1_7, SPIM2_MISO, SPIM0_MISO, SPIM1_MISO)
C6	PB08	BDSPZ	IO	Multiple function I/O (GPIO1_8, SPIM1_CS0_N, UA3_RXD)
D6	PB09	BDSPZ	IO	Multiple function I/O (GPIO1_9, SPIM1_CLK, UA3_TXD)
E6	PB10	BDSPZ	IO	Multiple function I/O (GPIO1_10, SPIM1_MOSI, UA3_CTS_N)
A5	PB11	BDSPAZ	IO	Multiple function I/O (GPIO1_11, SPIM1_MISO, UA3_RTS_N, AIN8)
B5	PB12	BDSPAZ	IO	Multiple function I/O (GPIO1_12, SPIM0_CS1_N, SPIM0_CS1_N, SPIM1_CS1_N, AIN9)
C5	PB13	BDSPAZ	IO	Multiple function I/O (GPIO1_13, SPIM0_CS2_N, SPIM0_CS2_N, SPIM1_CS2_N, AIN10)
D5	PB14	BDSPZ	IO	Multiple function I/O (GPIO1_14, I2C1_SCL)
E5	PB15	BDSPZ	IO	Multiple function I/O (GPIO1_15, I2C1_SDA)
B15	PC00	BDSPZ	IO	Multiple function I/O (GPIO1_16, I2S1_BCK, AFEZ_SYNC0, PDM_CLK, PWM4 / CAPTURE4)

Ball No.	Pin name	Attribute	I/O	Explanation
A14	PC01	BDSPZ	IO	Multiple function I/O (GPIO1_17, I2S1_LRCK, AFEZ_SYNC1, PDM_LDI, PWM5 / CAPTURE5)
B14	PC02	BDSPZ	IO	Multiple function I/O (GPIO1_18, I2S1_DI, AFEZ_SYNC2, PDM_RDI, PWM6 / CAPTURE6)
A13	PC03	BDSPZ	IO	Multiple function I/O (GPIO1_19, I2S1_DO, AFEZ_SYNC3, PWM7 / CAPTURE7)
B13	PC04	BDSPZ	IO	Multiple function I/O (GPIO1_20, I2S2_BCK, PDM_CLK)
C13	PC05	BDSPZ	IO	Multiple function I/O (GPIO1_21, I2S2_LRCK, PDM_LDI)
A12	PC06	BDSPZ	IO	Multiple function I/O (GPIO1_22, I2S2_DI, PDM_RDI)
B12	PC07	BDSPAZ	IO	Multiple function I/O (GPIO1_23, I2S_MCLKI, I2S_MCLKO, SPIM1_CS1_N, AIN11)
A4	PD00	BDSPZ	IO	Multiple function I/O (GPIO2_0, DBIB_CSX / DBIC_CSX)
A3	PD01	BDSPZ	IO	Multiple function I/O (GPIO2_1, DBIB_TE, PWM0 / CAPTURE0)
A2	PD02	BDSPZ	IO	Multiple function I/O (GPIO2_2, DBIB_RDX, PWM1 / CAPTURE1)
A1	PD03	BDSPZ	IO	Multiple function I/O (GPIO2_3, DBIB_WRX / DBIC_SCL)
B4	PD04	BDSPZ	IO	Multiple function I/O (GPIO2_4, DBIB_DCX / DBIC_DCX)
B3	PD05	BDSPZ	IO	Multiple function I/O (GPIO2_5, DBIB_D0 / DBIC_SDO)
B2	PD06	BDSPZ	IO	Multiple function I/O (GPIO2_6, DBIB_D1 / DBIC_SDI)
B1	PD07	BDSPZ	IO	Multiple function I/O (GPIO2_7, DBIB_D2, PWM2 / CAPTURE2)
C4	PD08	BDSPZ	IO	Multiple function I/O (GPIO2_8, DBIB_D3, PWM3 / CAPTURE3)
C3	PD09	BDSPZ	IO	Multiple function I/O (GPIO2_9, DBIB_D4, PWM4 / CAPTURE4)
C2	PD10	BDSPZ	IO	Multiple function I/O (GPIO2_10, DBIB_D5, PWM5 / CAPTURE5)
C1	PD11	BDSPZ	IO	Multiple function I/O (GPIO2_11, DBIB_D6, PWM6 / CAPTURE6)
D4	PD12	BDSPZ	IO	Multiple function I/O (GPIO2_12, DBIB_D7, PWM7 / CAPTURE7)
D3	PD13	BDSPZ	IO	Multiple function I/O (GPIO2_13, DBIB_D8)
D2	PD14	BDSPZ	IO	Multiple function I/O (GPIO2_14, DBIB_D9)
D1	PD15	BDSPZ	IO	Multiple function I/O (GPIO2_15, DBIB_D10)
E4	PD16	BDSPZ	IO	Multiple function I/O (GPIO2_16, DBIB_D11)
E3	PD17	BDSPZ	IO	Multiple function I/O (GPIO2_17, DBIB_D12, UA2_RXD)
E2	PD18	BDSPZ	IO	Multiple function I/O (GPIO2_18, DBIB_D13, UA2_TXD)

Ball No.	Pin name	Attribute	I/O	Explanation
E1	PD19	BDSPZ	IO	Multiple function I/O (GPIO2_19, DBIB_D14, UA2_CTS_N)
F4	PD20	BDSPZ	IO	Multiple function I/O (GPIO2_20, DBIB_D15, UA2_RTS_N)
L4	PE00	BDSPZ	IO	Multiple function I/O (GPIO3_0, EB_ADR0 / EB_DAT0)
L3	PE01	BDSPZ	IO	Multiple function I/O (GPIO3_1, EB_ADR1 / EB_DAT1)
L2	PE02	BDSPZ	IO	Multiple function I/O (GPIO3_2, EB_ADR2 / EB_DAT2)
L1	PE03	BDSPZ	IO	Multiple function I/O (GPIO3_3, EB_ADR3 / EB_DAT3)
M4	PE04	BDSPZ	IO	Multiple function I/O (GPIO3_4, EB_ADR4 / EB_DAT4)
M3	PE05	BDSPZ	IO	Multiple function I/O (GPIO3_5, EB_ADR5 / EB_DAT5)
M2	PE06	BDSPZ	IO	Multiple function I/O (GPIO3_6, EB_ADR6 / EB_DAT6)
M1	PE07	BDSPZ	IO	Multiple function I/O (GPIO3_7, EB_ADR7 / EB_DAT7)
N5	PE08	BDSPZ	IO	Multiple function I/O (GPIO3_8, EB_ADR8 / EB_DAT8)
N4	PE09	BDSPZ	IO	Multiple function I/O (GPIO3_9, EB_ADR9 / EB_DAT9)
N3	PE10	BDSPZ	IO	Multiple function I/O (GPIO3_10, EB_ADR10 / EB_DAT10)
N2	PE11	BDSPZ	IO	Multiple function I/O (GPIO3_11, EB_ADR11 / EB_DAT11)
N1	PE12	BDSPZ	IO	Multiple function I/O (GPIO3_12, EB_ADR12 / EB_DAT12)
P5	PE13	BDSPZ	IO	Multiple function I/O (GPIO3_13, EB_ADR13 / EB_DAT13)
P4	PE14	BDSPZ	IO	Multiple function I/O (GPIO3_14, EB_ADR14 / EB_DAT14)
P3	PE15	BDSPZ	IO	Multiple function I/O (GPIO3_15, EB_ADR15 / EB_DAT15)
P2	PF00	BDSPZ	IO	Multiple function I/O (GPIO3_16, EB_ADR16)
P1	PF01	BDSPZ	IO	Multiple function I/O (GPIO3_17, EB_ADR17)
R5	PF02	BDSPZ	IO	Multiple function I/O (GPIO3_18, EB_ADR18)
R4	PF03	BDSPZ	IO	Multiple function I/O (GPIO3_19, EB_ADR19)
R3	PF04	BDSPZ	IO	Multiple function I/O (GPIO3_20, EB_ADR20)
R2	PF05	BDSPZ	IO	Multiple function I/O (GPIO3_21, EB_ADR21)
R1	PF06	BDSPZ	IO	Multiple function I/O (GPIO2_21, EB_AVD_N)
T5	PF07	BDSPZ	IO	Multiple function I/O (GPIO2_22, EB_WE_N)
T4	PF08	BDSPZ	IO	Multiple function I/O (GPIO2_23, EB_OE_N)

Ball No.	Pin name	Attribute	I/O	Explanation
T3	PF09	BDSPZ	IO	Multiple function I/O (GPIO2_24, EB_CE0_N)
T2	PF10	BDSPZ	IO	Multiple function I/O (GPIO2_25, EB_CE1_N)
T1	PF11	BDSPZ	IO	Multiple function I/O (GPIO2_26, EB_BE0_N)
U6	PF12	BDSPZ	IO	Multiple function I/O (GPIO2_27, EB_BE1_N)
U5	PF13	BDSPZ	IO	Multiple function I/O (GPIO2_28, EB_CLKO)
U4	PF14	BDSPZ	IO	Multiple function I/O (GPIO2_29, EB_CLKI)
U3	PF15	BDSPZ	IO	Multiple function I/O (GPIO2_30, EB_WAIT_N)
U2	PF16	BDSPZ	IO	Multiple function I/O (GPIO2_31, EB_CRE)
U11	PG00	BDSPD	IO	Multiple function I/O (GPIO3_22, DBG_SWCLK, UA0_CTS_N)
T11	PG01	BDSPU	IO	Multiple function I/O (GPIO3_23, DBG_SWDIO, UA0_RTS_N)
R11	PG02	BDSPZ	IO	Multiple function I/O (GPIO0_30, UA0_RXD)
U12	PG03	BDSPZ	IO	Multiple function I/O (GPIO0_31, UA0_TXD, DBG_TRACEDATA3)
B8	PH00	BDSPZ	IO	Multiple function I/O (GPIO1_24, SPINOFC_CS0_N, SPIFC_CS1_N)
C8	PH01	BDSPZ	IO	Multiple function I/O (GPIO1_25, SPINOFC_CLK, EM1_CLK, SPIFC_CLK, SPIM3_CLK)
A9	PH02	BDSPZ	IO	Multiple function I/O (GPIO1_26, SPINOFC_MOSI, EM1_DAT0, SPIFC_MOSI, SPIM3_MOSI)
B9	PH03	BDSPZ	IO	Multiple function I/O (GPIO1_27, SPINOFC_MISO, EM1_DAT1, SPIFC_MISO, SPIM3_MISO)
C9	PH04	BDSPZ	IO	Multiple function I/O (GPIO1_28, SPINOFC_IO2, EM1_DAT2, SPIFC_IO2)
D9	PH05	BDSPZ	IO	Multiple function I/O (GPIO1_29, SPINOFC_IO3, EM1_DAT3, SPIFC_IO3)
E9	PH06	BDSPZ	IO	Multiple function I/O (GPIO1_30, SPINOFC_CS2_N, EM1_CMD, SPIFC_CS0_N)
A10	PH07	BDSPZ	IO	Multiple function I/O (GPIO1_31, SPINOFC_CS1_N, EM1_CLKB, SPIFC_CS2_N, SPIM3_CS_N)
B10	PH08	BDSPZ	IO	Multiple function I/O (GPIO0_19, EM0_CLK, SPIFC_CS0_N)
C10	PH09	BDSPZ	IO	Multiple function I/O (GPIO0_20, EM0_CLKB, SPIFC_CLK)
D10	PH10	BDSPZ	IO	Multiple function I/O (GPIO0_21, EM0_CMD, SPIFC_MOSI)
E10	PH11	BDSPZ	IO	Multiple function I/O (GPIO0_22, EM0_DAT0, SPIFC_MISO)

Ball No.	Pin name	Attribute	I/O	Explanation
A11	PH12	BDSPZ	IO	Multiple function I/O (GPIO0_23, EM0_DAT1, SPIFC_IO2)
B11	PH13	BDSPZ	IO	Multiple function I/O (GPIO0_24, EM0_DAT2, SPIFC_IO3)
C11	PH14	BDSPZ	IO	Multiple function I/O (GPIO0_25, EM0_DAT3, SPIFC_CS1_N)
D11	PH15	BDSPAZ	IO	Multiple function I/O (GPIO0_26, EM0_DAT4, SPIM3_CS_N, UA2_CTS_N, SPIFC_CS2_N, AIN12)
E11	PH16	BDSPAZ	IO	Multiple function I/O (GPIO0_27, EM0_DAT5, SPIM3_CLK, UA2_RTS_N, AIN13)
C12	PH17	BDSPAZ	IO	Multiple function I/O (GPIO0_28, EM0_DAT6, SPIM3_MOSI, UA2_RXD, AIN14)
D12	PH18	BDSPAZ	IO	Multiple function I/O (GPIO0_29, EM0_DAT7, SPIM3_MISO, UA2_TXD, AIN15)
H2	DSI_CP	DPHY	Out	DSI positive differential output of clock lane
H3	DSI_CN	DPHY	Out	DSI negative differential output of clock lane
G2	DSI_DP0	DPHY	IO	DSI positive differential data input/output of data lane0
G3	DSI_DN0	DPHY	IO	DSI negative differential data input/output of data lane0
J2	DSI_DP1	DPHY	Out	DSI positive differential data output of data lane1
J3	DSI_DN1	DPHY	Out	DSI negative differential data output of data lane1
K17	VREFH	ANALOG	In	ADCC12/AFEZ/DACC Higher reference voltage
J17	VREFL	ANALOG	In	ADCC12/AFEZ/DACC Lower reference voltage
L17	AIN0	ANALOG	In	ADCC12 Analog input channel 0
M17	AIN1	ANALOG	In	ADCC12 Analog input channel 1
J16	AI0P	ANALOG	In	AFEZ Positive analog input channel 0
J15	AI0N	ANALOG	In	AFEZ Negative analog input channel 0
K16	AI1P	ANALOG	In	AFEZ Positive analog input channel 1
K15	AI1N	ANALOG	In	AFEZ Negative analog input channel 1
L16	AI2P	ANALOG	In	AFEZ Positive analog input channel 2
L15	AI2N	ANALOG	In	AFEZ Negative analog input channel 2
M16	AI3P	ANALOG	In	AFEZ Positive analog input channel 3
M15	AI3N	ANALOG	In	AFEZ Negative analog input channel 3
H15	AO0P	ANALOG	Out	AFEZ Positive analog output from PGA
H16	AO0N	ANALOG	Out	AFEZ Negative analog output from PGA
G14	AO1P	ANALOG	Out	AFEZ Positive analog output from Rectifier
H14	AO1N	ANALOG	Out	AFEZ Negative analog output from Rectifier
E15	ZAI0	ANALOG	In	AFEZ Excitation Amp analog input 0
E14	ZAI1	ANALOG	In	AFEZ Excitation Amp analog input 1
F16	ZAI2	ANALOG	In	AFEZ Excitation Amp analog input 2
F15	ZAO	ANALOG	Out	AFEZ Excitation Amp analog output
G16	RLDI1	ANALOG	In	AFEZ RLD Amp analog input 1
G15	RLDI2	ANALOG	In	AFEZ RLD Amp analog input 2
F14	RLDO	ANALOG	Out	AFEZ RLD Amp analog output
E16	DAOUT	ANALOG	Out	DACC DAC Voltage Output
D15	ILEDA0	ANALOG	Out	Current output of ChA0 (5 V Tolerant)
D14	ILEDA1	ANALOG	Out	Current output of ChA1 (5 V Tolerant)
C14	ILEDB0	ANALOG	Out	Current output of ChB0
C15	ILEDB1	ANALOG	Out	Current output of ChB1
A16	USB_DP	USB-IO	IO	USB port I/O data (DP)

Ball No.	Pin name	Attribute	I/O	Explanation
A17	USB_DM	USB-IO	IO	USB port I/O data (DM)
R13	TEST	IS	In	Pin for test, connect to VSSC in application.
D13	VPGM	OTHER	In	Pin for test, connect to VSSC in application.
R16	BGR_OUT	ANALOG	Out	BGR Monitor output
A8	VDD33_SPIFOUT	POWER	Out	VDD33 output for SPI NOR Flash
(*1)	VDD33	POWER	–	VDD input
U16	DCDCOUT	POWER	—	DCDC output
E7, U17	VDD12D	POWER	—	Digital 1.2 V input
H1	VDD12_DSIPEXT	POWER	—	PLL power supply for DPHY
G1	VDD12_DSIEXT	POWER	—	Receiver/transmitter power supply for DPHY
J1	VDD12_DSIC	POWER	—	Digital power supply for DPHY
B17	VDD33_USB	POWER	—	USB IO Power
A15	VDD33_USBO	POWER	Out	Power pin for the pull-up resistance of the USB device signal. It cannot be used as a power supply for other devices.
B16	VSS33_USB	GND	—	USB IO GND
C16, C17	VDD33_LED	POWER	—	LEDC Power Supply for LED driver and current reference
D16, D17	VSS33_LED	POWER	—	LEDC Ground for LED driver and current reference
(*2)	VSSC	GND	—	Ground
F17, G17	AVDD33	A-POWER	—	ADCC12/AFEZ/DACC Analog Power supply
(*3)	AVSS33	A-GND	—	ADCC12/AFEZ/DACC Analog Ground

*1: E13, F5, P6, T17

*2: E12, F1, F2, F3, F6, K1, K2, K3, N15, N16, N17, P7, R15, U1

*3: E17, H17, J14, K14, L14, M14

5.4. Setting Multiple function I/O

Some of pins have multiple functions. Register settings define a function of each pin. After booting up, pin functions are defined "FMODE" which is controlled by register in GCONF module.

The following table describes pin functions defined with each FMODE.

Table 5-3 Multiple function I/O

Pin Name	FUNCTION Name						
	FMODE0	FMODE1	FMODE2	FMODE3	FMODE4	FMODE5	FMODE6
PA00	No Function	GPIO0_0	—	—	—	—	—
PA01	No Function	GPIO0_1	—	—	—	—	—
PA02	No Function	GPIO0_2	—	—	—	—	—
PA03	No Function	GPIO0_3	—	—	—	—	—
PA04	No Function	GPIO0_4	—	—	—	—	—
PA05	No Function	GPIO0_5	—	—	—	—	—
PA06	No Function	GPIO0_6	—	—	—	—	—
PA07	No Function	GPIO0_7	—	—	—	—	—
PA08	No Function	GPIO0_8	—	—	—	—	—
PA09	No Function	GPIO0_9	—	—	—	—	—
PA10	No Function	GPIO0_10	—	—	—	—	—
PA11	No Function	GPIO0_11	—	—	—	—	—
PA12	No Function / AIN2	GPIO0_12	—	—	AFEZ_SYNC0	PWM0 / CAPTURE0	DBG_TRACEDATA2
PA13	No Function / AIN3	GPIO0_13	—	—	AFEZ_SYNC1	PWM1 / CAPTURE1	DBG_TRACEDATA1
PA14	No Function / AIN4	GPIO0_14	—	—	AFEZ_SYNC2	PWM2 / CAPTURE2	DBG_TRACEDATA0
PA15	No Function / AIN5	GPIO0_15	DBG_SWV	—	AFEZ_SYNC3	PWM3 / CAPTURE3	DBG_TRACECLK
PA16	No Function	GPIO0_16	—	—	—	—	—
PA17	No Function	GPIO0_17	I2C0_SCL	—	—	—	—
PA18	No Function	GPIO0_18	I2C0_SDA	—	—	—	—
PB00	No Function	GPIO1_0	SPIM0_CS0_N	UA1_RXD	I2S0_BCK	—	—
PB01	No Function	GPIO1_1	SPIM0_CLK	UA1_TXD	I2S0_LRCK	—	—
PB02	No Function / AIN6	GPIO1_2	SPIM0_MOSI	UA1_CTS_N	I2S0_DI	—	—
PB03	No Function / AIN7	GPIO1_3	SPIM0_MISO	UA1_RTS_N	I2S0_DO	—	—
PB04	No Function	GPIO1_4	SPIM2_CS_N	SPIM0_CS0_N	SPIM1_CS0_N	—	—
PB05	No Function	GPIO1_5	SPIM2_CLK	SPIM0_CLK	SPIM1_CLK	—	—
PB06	No Function	GPIO1_6	SPIM2_MOSI	SPIM0_MOSI	SPIM1_MOSI	—	—
PB07	No Function	GPIO1_7	SPIM2_MISO	SPIM0_MISO	SPIM1_MISO	—	—
PB08	No Function	GPIO1_8	SPIM1_CS0_N	UA3_RXD	—	—	—
PB09	No Function	GPIO1_9	SPIM1_CLK	UA3_TXD	—	—	—
PB10	No Function	GPIO1_10	SPIM1_MOSI	UA3_CTS_N	—	—	—
PB11	No Function / AIN8	GPIO1_11	SPIM1_MISO	UA3_RTS_N	—	—	—
PB12	No Function / AIN9	GPIO1_12	SPIM0_CS1_N	SPIM0_CS1_N	SPIM1_CS1_N	—	—
PB13	No Function / AIN10	GPIO1_13	SPIM0_CS2_N	SPIM0_CS2_N	SPIM1_CS2_N	—	—
PB14	No Function	GPIO1_14	I2C1_SCL	—	—	—	—
PB15	No Function	GPIO1_15	I2C1_SDA	—	—	—	—
PC00	No Function	GPIO1_16	I2S1_BCK	AFEZ_SYNC0	PDM_CLK	PWM4 / CAPTURE4	—
PC01	No Function	GPIO1_17	I2S1_LRCK	AFEZ_SYNC1	PDM_LDI	PWM5 / CAPTURE5	—
PC02	No Function	GPIO1_18	I2S1_DI	AFEZ_SYNC2	PDM_RDI	PWM6 / CAPTURE6	—
PC03	No Function	GPIO1_19	I2S1_DO	AFEZ_SYNC3	—	PWM7 / CAPTURE7	—
PC04	No Function	GPIO1_20	I2S2_BCK	PDM_CLK	—	—	—
PC05	No Function	GPIO1_21	I2S2_LRCK	PDM_LDI	—	—	—
PC06	No Function	GPIO1_22	I2S2_DI	PDM_RDI	—	—	—

Pin Name	FUNCTION Name						
	FMODE0	FMODE1	FMODE2	FMODE3	FMODE4	FMODE5	FMODE6
PC07	No Function / AIN11	GPIO1_23	I2S_MCLKI	I2S_MCLKO	—	SPIM1_CS1_N	—
PD00	No Function	GPIO2_0	DBIB_CSX / DBIC_CSX	—	—	—	—
PD01	No Function	GPIO2_1	DBIB_TE	PWM0 / CAPTURE0	—	—	—
PD02	No Function	GPIO2_2	DBIB_RDX	PWM1 / CAPTURE1	—	—	—
PD03	No Function	GPIO2_3	DBIB_WRX / DBIC_SCL	—	—	—	—
PD04	No Function	GPIO2_4	DBIB_DCX / DBIC_DCX	—	—	—	—
PD05	No Function	GPIO2_5	DBIB_D0 / DBIC_SDO	—	—	—	—
PD06	No Function	GPIO2_6	DBIB_D1 / DBIC_SDI	—	—	—	—
PD07	No Function	GPIO2_7	DBIB_D2	PWM2 / CAPTURE2	—	—	—
PD08	No Function	GPIO2_8	DBIB_D3	PWM3 / CAPTURE3	—	—	—
PD09	No Function	GPIO2_9	DBIB_D4	PWM4 / CAPTURE4	—	—	—
PD10	No Function	GPIO2_10	DBIB_D5	PWM5 / CAPTURE5	—	—	—
PD11	No Function	GPIO2_11	DBIB_D6	PWM6 / CAPTURE6	—	—	—
PD12	No Function	GPIO2_12	DBIB_D7	PWM7 / CAPTURE7	—	—	—
PD13	No Function	GPIO2_13	DBIB_D8	—	—	—	—
PD14	No Function	GPIO2_14	DBIB_D9	—	—	—	—
PD15	No Function	GPIO2_15	DBIB_D10	—	—	—	—
PD16	No Function	GPIO2_16	DBIB_D11	—	—	—	—
PD17	No Function	GPIO2_17	DBIB_D12	UA2_RXD	—	—	—
PD18	No Function	GPIO2_18	DBIB_D13	UA2_TXD	—	—	—
PD19	No Function	GPIO2_19	DBIB_D14	UA2_CTS_N	—	—	—
PD20	No Function	GPIO2_20	DBIB_D15	UA2_RTS_N	—	—	—
PE00	No Function	GPIO3_0	EB_ADR0 / EB_DAT0	—	—	—	—
PE01	No Function	GPIO3_1	EB_ADR1 / EB_DAT1	—	—	—	—
PE02	No Function	GPIO3_2	EB_ADR2 / EB_DAT2	—	—	—	—
PE03	No Function	GPIO3_3	EB_ADR3 / EB_DAT3	—	—	—	—
PE04	No Function	GPIO3_4	EB_ADR4 / EB_DAT4	—	—	—	—
PE05	No Function	GPIO3_5	EB_ADR5 / EB_DAT5	—	—	—	—
PE06	No Function	GPIO3_6	EB_ADR6 / EB_DAT6	—	—	—	—
PE07	No Function	GPIO3_7	EB_ADR7 / EB_DAT7	—	—	—	—
PE08	No Function	GPIO3_8	EB_ADR8 / EB_DAT8	—	—	—	—
PE09	No Function	GPIO3_9	EB_ADR9 / EB_DAT9	—	—	—	—
PE10	No Function	GPIO3_10	EB_ADR10 / EB_DAT10	—	—	—	—
PE11	No Function	GPIO3_11	EB_ADR11 / EB_DAT11	—	—	—	—
PE12	No Function	GPIO3_12	EB_ADR12 / EB_DAT12	—	—	—	—
PE13	No Function	GPIO3_13	EB_ADR13 / EB_DAT13	—	—	—	—

Pin Name	FUNCTION Name						
	FMODE0	FMODE1	FMODE2	FMODE3	FMODE4	FMODE5	FMODE6
PE14	No Function	GPIO3_14	EB_ADR14 / EB_DAT14	—	—	—	—
PE15	No Function	GPIO3_15	EB_ADR15 / EB_DAT15	—	—	—	—
PF00	No Function	GPIO3_16	EB_ADR16	—	—	—	—
PF01	No Function	GPIO3_17	EB_ADR17	—	—	—	—
PF02	No Function	GPIO3_18	EB_ADR18	—	—	—	—
PF03	No Function	GPIO3_19	EB_ADR19	—	—	—	—
PF04	No Function	GPIO3_20	EB_ADR20	—	—	—	—
PF05	No Function	GPIO3_21	EB_ADR21	—	—	—	—
PF06	No Function	GPIO2_21	EB_AVD_N	—	—	—	—
PF07	No Function	GPIO2_22	EB_WE_N	—	—	—	—
PF08	No Function	GPIO2_23	EB_OE_N	—	—	—	—
PF09	No Function	GPIO2_24	EB_CE0_N	—	—	—	—
PF10	No Function	GPIO2_25	EB_CE1_N	—	—	—	—
PF11	No Function	GPIO2_26	EB_BE0_N	—	—	—	—
PF12	No Function	GPIO2_27	EB_BE1_N	—	—	—	—
PF13	No Function	GPIO2_28	EB_CLKO	—	—	—	—
PF14	No Function	GPIO2_29	EB_CLKI	—	—	—	—
PF15	No Function	GPIO2_30	EB_WAIT_N	—	—	—	—
PF16	No Function	GPIO2_31	EB_CRE	—	—	—	—
PG00	No Function	GPIO3_22	DBG_SWCLK	UA0_CTS_N	—	—	—
PG01	No Function	GPIO3_23	DBG_SWDIO	UA0_RTS_N	—	—	—
PG02	No Function	GPIO0_30	—	UA0_RXD	—	—	—
PG03	No Function	GPIO0_31	—	UA0_TXD	—	—	DBG_TRACEDATA3
PH00	No Function	GPIO1_24	SPINOFC_CS0_N	—	SPIFC_CS1_N	—	—
PH01	No Function	GPIO1_25	SPINOFC_CLK	EM1_CLK	SPIFC_CLK	SPIM3_CLK	—
PH02	No Function	GPIO1_26	SPINOFC_MOSI	EM1_DAT0	SPIFC_MOSI	SPIM3_MOSI	—
PH03	No Function	GPIO1_27	SPINOFC_MISO	EM1_DAT1	SPIFC_MISO	SPIM3_MISO	—
PH04	No Function	GPIO1_28	SPINOFC_IO2	EM1_DAT2	SPIFC_IO2	—	—
PH05	No Function	GPIO1_29	SPINOFC_IO3	EM1_DAT3	SPIFC_IO3	—	—
PH06	No Function	GPIO1_30	SPINOFC_CS2_N	EM1_CMD	SPIFC_CS0_N	—	—
PH07	No Function	GPIO1_31	SPINOFC_CS1_N	EM1_CLKB	SPIFC_CS2_N	SPIM3_CS_N	—
PH08	No Function	GPIO0_19	EM0_CLK	—	—	SPIFC_CS0_N	—
PH09	No Function	GPIO0_20	EM0_CLKB	—	—	SPIFC_CLK	—
PH10	No Function	GPIO0_21	EM0_CMD	—	—	SPIFC_MOSI	—
PH11	No Function	GPIO0_22	EM0_DAT0	—	—	SPIFC_MISO	—
PH12	No Function	GPIO0_23	EM0_DAT1	—	—	SPIFC_IO2	—
PH13	No Function	GPIO0_24	EM0_DAT2	—	—	SPIFC_IO3	—
PH14	No Function	GPIO0_25	EM0_DAT3	—	—	SPIFC_CS1_N	—
PH15	No Function / AIN12	GPIO0_26	EM0_DAT4	SPIM3_CS_N	UA2_CTS_N	SPIFC_CS2_N	—
PH16	No Function / AIN13	GPIO0_27	EM0_DAT5	SPIM3_CLK	UA2_RTS_N	—	—
PH17	No Function / AIN14	GPIO0_28	EM0_DAT6	SPIM3_MOSI	UA2_RXD	—	—
PH18	No Function / AIN15	GPIO0_29	EM0_DAT7	SPIM3_MISO	UA2_TXD	—	—

Table 5-4 Function name

Function Name	I/O	Explanation
No Function	In	Not connected to any controller
No Function / AIN2–15	In	- Not connected to any controller (Digital Signal) - ADCC12 Analog input channel 2–15 (Analog Signal)
GPIO0_0	In	Programmable I/O: GPIO0 PIN0 (Can be used for USB VBUS detection, Wakeup, Input Only)
GPIO0_1–11	IO	Programmable I/O: GPIO0 PIN1–11 (Can be used for Wakeup)
GPIO0_12–15	IO	Programmable I/O: GPIO0 PIN12−15
GPIO0_16	In/OD	Open drain GPIO0 PIN16
GPIO0_17–31	IO	Programmable I/O: GPIO0 PIN17–31
GPIO1_0–31	IO	Programmable I/O: GPIO1 PIN0−31
GPIO2_0–31	IO	Programmable I/O: GPIO2 PIN0−31
GPIO3_0–16	IO	Programmable I/O: GPIO3 PIN0−16
GPIO3_17–23	IO	Programmable I/O: GPIO3 PIN17−23, Interrupt detection and notification are not available.
SPIMn_CS0_N	Out	SPIMn chip select 0 (n = 0–1)
SPIMn_CS1_N	Out	SPIMn chip select 1 (n = 0–1)
SPIMn_CS2_N	Out	SPIMn chip select 2 (n = 0–1)
SPIMn_CS_N	Out	SPIMn chip select (n = 2–3)
SPIMn_CLK	Out	SPIMn clock output (n = 0–3)
SPIMn_MOSI	Out	SPIMn serial data output (n = 0–3)
SPIMn_MISO	In	SPIMn serial data input (n = 0–3)
I2Cn_SDA	In/OD	I2Cn data (n = 0−1)
I2Cn_SCL	In/OD	I2Cn clock (n = 0−1)
UAn_RXD	In	UARTn serial data input (n = 0−3)
UAn_TXD	Out	UARTn serial data output (n = 0−3)
UAn_RTS_N	Out	UARTn RTS output (n = 0−3)
UAn_CTS_N	In	UARTn CTS input (n = 0−3)
SPINOFC_CS0_N	Out	SPINOFC chip select 0
SPINOFC_CS1_N	Out	SPINOFC chip select 1
SPINOFC_CS2_N	Out	SPINOFC chip select 2
SPINOFC_CLK	Out	SPINOFC clock output
SPINOFC_MOSI	IO	SPINOFC serial data output
SPINOFC_MISO	IO	SPINOFC serial data input
SPINOFC_IO2	IO	SPINOFC IO2
SPINOFC_IO3	IO	SPINOFC IO3
SPIFC_CS0_N	Out	SPIFC chip select 0
SPIFC_CS1_N	Out	SPIFC chip select 1
SPIFC_CS2_N	Out	SPIFC chip select 2
SPIFC_CLK	Out	SPIFC clock output
SPIFC_MOSI	IO	SPIFC serial data output
SPIFC_MISO	IO	SPIFC serial data input
SPIFC_IO2	IO	SPIFC IO2
SPIFC_IO3	IO	SPIFC IO3
AINn	In	ADCC12 Analog input n (n = 0−15)
AFEZ_SYNCn	Out	AFEZ Sampling timing sync output n (n = 0−3)

Function Name	I/O	Explanation
PWMn/CAPTUREn	In/Out	ADVTMR0 PWMm/CAPTUREm (n = 0−3, m = 0−3) ADVTMR1 PWMm/CAPTUREm (n = 4−7, m = 0−3)
I2Sn_BCK	IO	I2Sn audio serial clock (n = 0−2)
I2Sn_LRCK	IO	I2Sn audio L/R clock (n = 0−2)
I2Sn_DI	In	I2Sn audio serial data input (n = 0−2)
I2Sn_DO	Out	I2Sn audio serial data output (n = 0−1)
PDM_CLK	Out	PDM ADC clock output
PDM_LDI	In	PDM left data input
PDM_RDI	In	PDM right data input
I2S_MCLKI	In	I2S audio master clock input
I2S_MCLKO	Out	I2S audio master clock output
DBIB_CSX / DBIC_CSX	Out	DBIBC (DBI-B, DBI-C) chip select
DBIB_TE	In/Out	DBIBC (DBI-B) tearing effect input / V-sync output
DBIB_RDX	Out	DBIBC (DBI-B) read strobe
DBIB_WRX / DBIC_SCL	Out	DBIBC (DBI-B) write strobe, DBIBC (DBI-C) serial-clk
DBIB_DCX / DBIC_DCX	Out	DBIBC (DBI-B, DBI-C) data/command select
DBIB_D0 / DBIC_SDO	IO	DBIBC (DBI-B) parallel-data input, DBIBC (DBI-C) serial-data output/input
DBIB_D1 / DBIC_SDI	IO	DBIBC (DBI-B) parallel-data input, DBIBC (DBI-C) serial-data input
DBIB_D2−15	IO	DBIBC (DBI-B) parallel-data input
EB_ADRn/EB_DATn	IO	EBIF address/data (address-data multiplex, n = 0−15)
EB_ADR16-21	Out	EBIF address
EB_AVD_N	Out	EBIF address valid
EB_WE_N	Out	EBIF write enable
EB_OE_N	Out	EBIF output enable
EB_CE0_N	Out	EBIF chip enable 0
EB_CE1_N	Out	EBIF chip enable 1
EB_BE0_N	Out	EBIF byte enable 0
EB_BE1_N	Out	EBIF byte enable 1
EB_CLKO	Out	EBIF output clock
EB_CLKI	In	EBIF feedback input clock
EB_WAIT_N	In	EBIF wait
EB_CRE	Out	EBIF CellularRAM Configuration Register Access Enable
EMn_CLK	Out	EMMC clock output (n = 0–1)
EMn_CLKB	In	EMMC timing control clock (n = 0−1)
EMn_CMD	IO	EMMC command (n = 0−1)
EMn_DATm	IO	EMMC data (n = 0−1, m = 0−3 (n == 0) or 0−7 (n == 1))
DBG_SWCLK	In	SWD clock input
DBG_SWDIO	IO	SWD data in/out
DBG_SWV	Out	SWV trace data output
DBG_TRACECLK	Out	CPU trace clock
DBG_TRACEDATA0−3	Out	CPU trace data

6. Electrical Specification

All the characteristic data indicated in this section are results of data simulation. At this point, they are tentative value and might be changed after silicon validation/characterization.

All characteristics indicated in this section are applicable to the following conditions unless otherwise specified.

- VDD33 = 1.7 to 3.6 V
- AVDD33 = 1.7 to 3.6 V
- VDDC = 0.85 to 1.35 V
- Ta = -20 to 70°C

6.1. Absolute Maximum Ratings

Table 6-1 Absolute Maximum Ratings

Parameter	Symbol	Pin	Rating	Unit
Supply Voltage	VDDMAX	VDD33 VDD33_USB AVDD33 VDD33_LED	-0.3 to 3.9	V
		VDD12D	-0.3 to 1.6	V
		VDD12_DSIPEXT VDD12_DSIEXT VDD12_DSIC	-0.3 to 1.6	V
Supply Current	IMAX	VDD33	250	mA
		VDD33_USB	20	mA
		AVDD33	30	mA
		VDD12D	180	mA
		VDD12_DSI	100	mA
Input Voltage	VINMAX	5 V Tolerant pin (PA00, PA16, ILEDA0, ILEDA1)	-0.3 to VDD33+3.5 or -0.3 to 5.5 (*1)	V
		Other pins	-0.3 to VDD33 + 0.3 V or -0.3 to 3.9 (*1)	V
Input Current	IINMAX	LED current driver pins (ILEDA0,ILEDA1, ILEDB0, ILEDB1)	±50	mA
		Other pins	±10	mA
Storage Temperature	Tstg	—	-40 to 125	°C

*1: Smaller value is applied.

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these ratings would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause breakdown, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

6.2. Operating Conditions

6.2.1. Recommended Operating Conditions

Table 6-2 Recommended Operating Conditions

Parameter	Symbol	Pin	Condition	Min	Typ.	Max	Unit
Supply Voltage	VDD33	VDD33	—	1.7	3.3	3.6	V
	VDD33_USB	VDD33_USB	—	3.0	3.3	3.6	V
	AVDD33	AVDD33	—	1.7	3.3	3.6	V
	VDD33_LED	VDD33_LED	—	1.7	3.3	3.6	V
	VDD12	VDD12D (*1)	Voltage Mode Over Drive (*2)	—	1.3	—	V
			Voltage Mode A	—	1.2	—	
			Voltage Mode B	—	1.1	—	
	VDD12_DSI	VDD12_DSIPEXT VDD12_DSIEXT VDD12_DSIC	—	1.1	1.2	1.3	V
Input Clock Frequency	f_{OSCH}	XOUT_12M XIN_12M	—	—	12	—	MHz
	f_{OSCL}	XOUT_32k XIN_32k	—	—	32.768	—	kHz
Operating Temperature	Ta	—	—	-20	25	70	°C

*1: Should be connected to the regulator output pin (DCDCOUT) via an inductor.

*2: Constant Over Drive may shorten product life.

6.2.2. Internal Power Supply and Power Output

Table 6-3 Internal Power Supply and Power Output

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
MCU Internal Logic Power	VDDC	Voltage Mode Over Drive	—	1.3	—	V
		Voltage Mode A	—	1.2	—	V
		Voltage Mode B	—	1.1	—	V
		Voltage Mode D	—	0.9	—	V
Power Supply of VDD33_SPIFOUT	VDD33_SPIF	I_{OUT} = 0mA	—	VDD33	—	V
		I_{OUT} = 30mA	VDD33 – 0.04	—	—	V
External capacitance of VDD33_SPIFOUT	CL_SPIF	—	—	—	5.0	µF

6.3. Power Consumption

The current consumption value indicated in Table 6-5 and Table 6-6 are measured with the condition below:

- VDD33 = 3.3 V or 1.8V
- All ACTIVE State current consumptions are measured with CoreMark™ benchmark program.
- The program is loaded to SRAMCM, and CPU fetched the codes and data from SRAMCM during running the benchmark.
- Clocks and power domains for each power mode are specified in Table 6-4.
- Dynamic Clock Gating function implemented in PMU is enabled.
- In WAIT (CLKMODE = 1) mode, clock sources except SIOSC12M and OSC32K are disabled. In WAIT (CLKMODE = 0), RETENTION and RTC mode, all clock sources except OSC32K for RTC are disabled. In STOP mode, all clock sources including OSC32K clock are disabled.
- Values are based on characterization test.

Other specific conditions are described in the table.

Table 6-4 Conditions of Power Consumption for each Power Mode

Power Domain	Block	ACTIVE	SLEEP	WAIT CLKMODE = 1	WAIT CLKMODE = 0	RETENTION	RTC	STOP
PD_AONLVC	PMULVC	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
	GCONF	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_MAIN	CPU	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
	MPIER	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
	SRAMCM	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
	ROMC	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_SRAM0		ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_SRAM1		ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_SRAM2		ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_SRAM3		ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_SUB	HPIER	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
	PPIER1	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
	PPIER0/2	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
	SRAMCS	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
	RTCLV	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
	EVM	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	RET	OFF	OFF
	I2C0/1/2	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	RET	OFF	OFF
	UART0	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	RET	OFF	OFF
	UART1/2	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
	SPIM0/1/2/3	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF

Power Domain	Block	ACTIVE	SLEEP	WAIT CLKMODE = 1	WAIT CLKMODE = 0	RETENTION	RTC	STOP
	GPIO0/1/2/3	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
	I2S/PDM	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_SRAM4		ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_NOFC	SPINOFC	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_DMAC	DMAC0	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
	DMAC1	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
PD_ENCRYPT	CRA	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
	RNG	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
	TZCP	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
PD_USB	USB2D	OFF	OFF	OFF	OFF	OFF	OFF	OFF
PD_NVM	SPIFC	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
	EMMC/SDIO	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
PD_DISPLAY	GPIER	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
	GFX	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
	DBIBC	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
	EBIF	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
	SRAMCG	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
PD_DSI	DSI	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	OFF	OFF	OFF
PD_SRAM5		ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_SRAM6		ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_SRAM7		ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_SRAM8		ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
PD_TMR	PPIER3	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	ON / CLK=OFF	RET	OFF	OFF
	TMR	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	RET	OFF	OFF
	ADVTMR	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	RET	OFF	OFF
	WDT	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	RET	OFF	OFF
PD_ADDA	ADCC12	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	RET	OFF	OFF
	AFEZ	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	RET	OFF	OFF
	DACC	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	RET	OFF	OFF
	LEDC	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF	RET	OFF	OFF
PD_EFUSE	EFUSE	OFF	OFF	OFF	OFF	OFF	OFF	OFF
PD_PLL	PLL	ON / CLK=ON	ON / CLK=ON	OFF	OFF	OFF	OFF	OFF
PD_ADPLL	ADPLL	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Power Domain	Block	ACTIVE	SLEEP	WAIT CLKMODE = 1	WAIT CLKMODE = 0	RETENTION	RTC	STOP
PD_ANOHV	RTCHV	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=ON	ON / CLK=OFF
	PMUHV	ON	ON	ON	ON	ON	ON	ON

Table 6-5 Current Consumption for each Power Mode (VDD33=3.3 V)

Power Mode	Voltage Mode	Conditions	Typ.	Max		Unit
			Ta=25°C	Ta=25°C	Ta=45°C	
ACTIVE	A	96 MHz (Clock Source: PLL, OSC12M used), VDD12D 1.2 V	6.7	—	—	mA
	B	48 MHz (Clock Source: PLL, OSC12M used), VDD12D 1.1 V	3.3	—	—	mA
	Over Drive	120 MHz (Clock Source: PLL, OSC12M used), VDD12D 1.3 V	9.6	—	—	mA
SLEEP	A	96 MHz is gated (Clock Source: PLL, OSC12M used), VDD12D 1.2 V	2.8	—	—	mA
	B	48 MHz is gated (Clock Source: PLL, OSC12M used), VDD12D 1.1 V	1.8	—	—	mA
	Over Drive	120 MHz is gated (Clock Source: PLL, OSC12M used), VDD12D 1.3 V	3.8	—	—	mA
WAIT (CLKMODE = 1)	D	12 MHz is gated (Clock Source: SIOSC12M, PLL and OSC12M disabled), LDOS 0.9 V	560	—	—	µA
WAIT (CLKMODE = 0)	D	LDOS 0.9 V	113	459	807	µA
RETENTION	D	LDOS 0.9 V	26.2	74.3	119	µA
RTC (*1)	D	LDOS 0.9 V	4.2	5.8	9.1	µA
STOP	D	LDOS 0.9 V	2.5	4.2	7.5	µA

*1: The value includes 32 kHz crystal (RIVER TFX-03 32.768 kHz).

Table 6-6 Current Consumption for each Power Mode (VDD33=1.8 V)

Power Mode	Voltage Mode	Conditions	Typ.	Max		Unit
			Ta=25°C	Ta=25°C	Ta=45°C	
ACTIVE	A	96 MHz (Clock Source: PLL, OSC12M used), VDD12D 1.2 V	11.1	—	—	mA
	B	48 MHz (Clock Source: PLL, OSC12M used), VDD12D 1.1 V	5.4	—	—	mA
	Over Drive	120 MHz (Clock Source: PLL, OSC12M used), VDD12D 1.3 V	15.8	—	—	mA
SLEEP	A	96 MHz is gated (Clock Source: PLL, OSC12M used), VDD12D 1.2 V	4.5	—	—	mA
	B	48 MHz is gated (Clock Source: PLL, OSC12M used), VDD12D 1.1 V	2.7	—	—	mA
	Over Drive	120 MHz is gated (Clock Source: PLL, OSC12M used), VDD12D 1.3 V	6.4	—	—	mA
WAIT (CLKMODE = 1)	D	12 MHz is gated (Clock Source: SIOSC12M, PLL and OSC12M disabled), LDOS 0.9 V	552	—	—	µA
WAIT (CLKMODE = 0)	D	LDOS 0.9 V	112	456	802	µA
RETENTION	D	LDOS 0.9 V	24.8	71.9	114.5	µA
RTC (*1)	D	LDOS 0.9 V	2.7	3.5	5.3	µA
STOP	D	LDOS 0.9 V	1.9	2.7	4.5	µA

*1: The value includes 32 kHz crystal (RIVER TFX-03 32.768 kHz).

6.4. DC Characteristics

Table 6-7 to Table 6-11 shows DC characteristics of IO pins. Regarding correspondence between each pin and IO cell type, please see signal list described in Section 5.

6.4.1. Schmitt Level Input / Multi-Drive Output / Programmable Pull-Up/Down IO pins

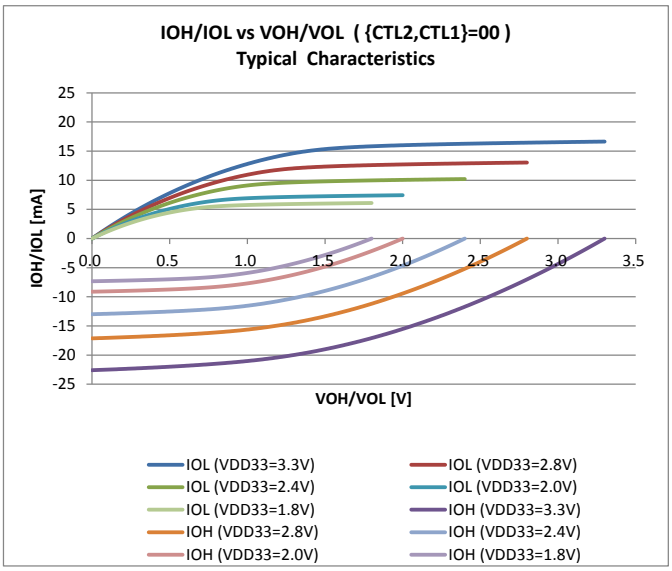
Table 6-7 Schmitt Level Input / Multi-Drive Output / Programmable Pull-Up/Down IO characteristics

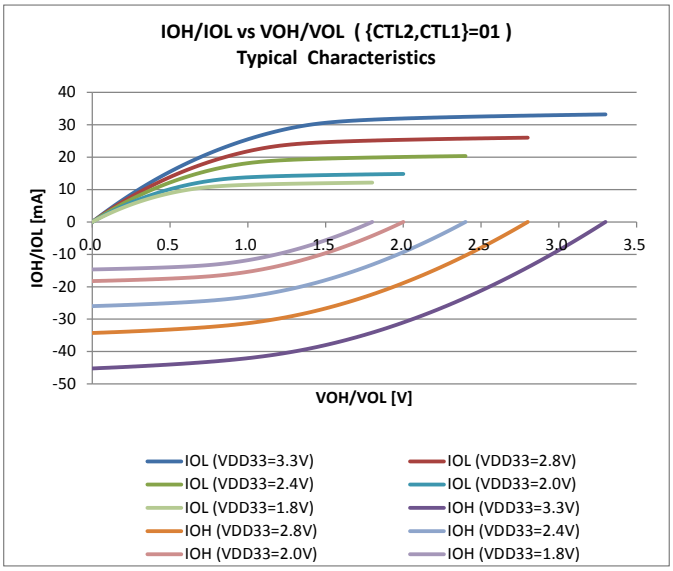
Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Low-level input current	IIL	VIN = VSS	Pull-up Disable	-10	—	10	μA
		VIN = VSS	Pull-up Enable (PUD = 0b1, ENPUD = 0b0) (*1)	-260	—	-40	μA
High-level input current	IIH	VIN = VDD33	Pull-down Disable	-10	—	10	μA
		VIN = VDD33	Pull-down Enable (PUD=0b0, ENPUD = 0b0) (*1)	40	—	260	μA
Low-level input voltage	VIL	—	—	—	—	VDD33 × 0.3	V
High-level input voltage	VIH	—	—	VDD33 × 0.7	—	—	V
Low-level output voltage	VOL	VDD33 = 2.8 to 3.6 V	{CTL2,CTL1} = 0b00 (*1) IOL = 2 mA	—	—	0.4	V
			{CTL2,CTL1} = 0b01 (*1) IOL = 4 mA	—	—	0.4	V
			{CTL2,CTL1} = 0b10 (*1) IOL = 6 mA	—	—	0.4	V
			{CTL2,CTL1} = 0b11 (*1) IOL = 8 mA	—	—	0.4	V
		VDD33 = 2.0 to 2.8 V	{CTL2,CTL1} = 0b00 (*1) IOL = 1.5 mA	—	—	0.4	V
			{CTL2,CTL1} = 0b01 (*1) IOL = 3 mA	—	—	0.4	V
			{CTL2,CTL1} = 0b10 (*1) IOL = 4.5 mA	—	—	0.4	V
			{CTL2,CTL1} = 0b11 (*1) IOL = 6 mA	—	—	0.4	V
		VDD33 = 1.7 to 2.0 V	{CTL2,CTL1} = 0b00 (*1) IOL = 1.5 mA	—	—	VDD33 × 0.2	V
			{CTL2,CTL1} = 0b01 (*1) IOL = 3 mA	—	—	VDD33 × 0.2	V
			{CTL2,CTL1} = 0b10 (*1) IOL = 4.5 mA	—	—	VDD33 × 0.2	V
			{CTL2,CTL1} = 0b11 (*1) IOL = 6 mA	—	—	VDD33 × 0.2	V
High-level output voltage	VOH	VDD33 = 2.8 to 3.6 V	{CTL2,CTL1} = 0b00 (*1) IOH = -2 mA	VDD33 - 0.4	—	—	V
			{CTL2,CTL1} = 0b01 (*1) IOH = -4 mA	VDD33 - 0.4	—	—	V
			{CTL2,CTL1} = 0b10 (*1) IOH = -6 mA	VDD33 - 0.4	—	—	V
			{CTL2,CTL1} = 0b11 (*1) IOH = -8 mA	VDD33 - 0.4	—	—	V
		VDD33 = 2.0 to 2.8 V	{CTL2,CTL1} = 0b00 (*1) IOH = -1.5 mA	VDD33 - 0.4	—	—	V
			{CTL2,CTL1} = 0b01 (*1)	VDD33	—	—	V

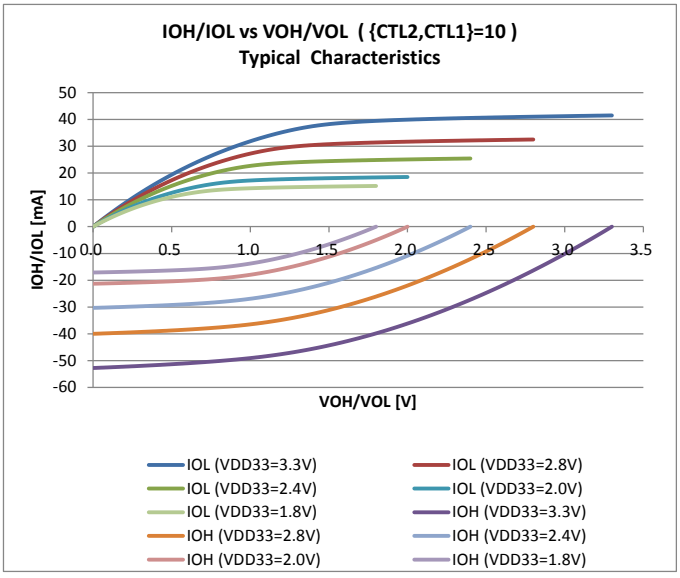
			IOH = -3 mA	- 0.4			
			{CTL2,CTL1} = 0b10 (*1) IOH = -4.5 mA	VDD33 - 0.4	—	—	V
			{CTL2,CTL1} = 0b11 (*1) IOH = -6 mA	VDD33 - 0.4	—	—	V
		VDD33 = 1.7 to 2.0 V	{CTL2,CTL1} = 0b00 (*1) IOH = -1.5 mA	VDD33 × 0.8	—	—	V
			{CTL2,CTL1} = 0b01 (*1) IOH = -3 mA	VDD33 × 0.8	—	—	V
			{CTL2,CTL1} = 0b10 (*1) IOH = -4.5 mA	VDD33 × 0.8	—	—	V
			{CTL2,CTL1} = 0b11 (*1) IOH = -6 mA	VDD33 × 0.8	—	—	V

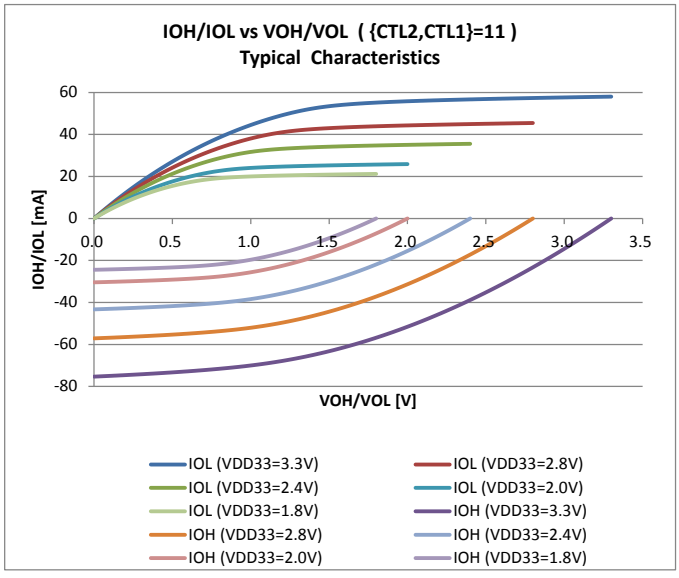
*1: PUD, ENPUD, CTL2 and CTL1 is a control register of GCONF block. Please see the GCONF section of the reference manual for detail.

Typical characteristics of output current (IOL/IOH) is shown on the figure below.









6.4.2. Schmitt Level Input / Open-Drain Output / 5 V tolerant IO pins

Table 6-8 Schmitt Level Input / Open-Drain Output / 5 V Tolerant IO

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Low-level input current	IIL	VIN = VSS	-10	—	10	μA
High-level input current	IIH	VIN = VDD33	-10	—	10	μA
Low-level input voltage	VIL	—	—	—	VDD33 × 0.3	V
High-level input voltage	VIH	—	VDD33 × 0.7	—	—	V
Low-level output voltage	VOL	VDD33 = 2.0 to 3.6 V	—	—	0.4	V
		VDD33 = 1.7 to 2.0 V	—	—	VDD33 × 0.2	V

6.4.3. Schmitt Level Input only pin

Table 6-9 Schmitt Level Input only pin characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Low-level input current	IIL	VIN = VSS	-10	—	10	μA
High-level input current	IIH	VIN = VDD33	-10	—	10	μA
Low-level input voltage	VIL	—	—	—	VDD33 × 0.3	V
High-level input voltage	VIH	—	VDD33 × 0.7	—	—	V

6.4.4. 5 V Tolerant Schmitt Level Input only pin

Table 6-10 5 V Tolerant Schmitt Level Input only pin characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Low-level input current	IIL	VIN = VSS	-10	—	10	μA
High-level input current	IIH	VIN = VDD33	-10	—	10	μA
Low-level input voltage	VIL	—	—	—	VDD33 × 0.3	V
High-level input voltage	VIH	—	VDD33 × 0.7	—	—	V

6.4.5. Output only pin

Table 6-11 Output only pin characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Low-level output voltage	VOL	VDDIO = 2.8 to 3.6 V, IOL = 2 mA	—	—	0.4	V
		VDDIO = 2.1 to 2.8 V, IOL = 1.5 mA	—	—	0.4	V
		VDDIO = 1.7 to 2.1 V, IOL = 1.5 mA	—	—	VDD33 × 0.2	V
High-level output voltage	VOH	VDDIO = 2.8 to 3.6 V, IOH = -2 mA	VDD33 - 0.4	—	—	V
		VDDIO = 2.1 to 2.8 V, IOH = -1.5 mA	VDD33 - 0.4	—	—	V
		VDDIO = 1.7 to 2.1 V, IOH = -1.5 mA	VDD33 × 0.8	—	—	V

6.5. Clock Source Characteristics

6.5.1. XOSC12M

Table 6-12 XOSC12M characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Oscillator Frequency	fO12M	—	—	12	—	MHz
External Feedback Resistor (*1)(*2)	Rf	—	—	—	—	MΩ
Startup Time (*1)(*4)	tSTART	R1 = 1 kΩ, CL = 5 pF, MAIN_GM = Mode2 (*3)	—	—	1.5	ms

*1: The value is based on evaluation result obtained with typical external components parameter. The value of these parameters varies depending on the crystal resonator used. It is recommended to refer the datasheet of the crystal resonator that you are going to use.

*2: TZ1200 series has the internal feedback resistor. It need not have external feedback resistor on board.

*3: MAIN_GM is one of the fields of the control register ***[OVERRIDE_EFUSE_OSC12M_TRIMMING]*** in Power Management Unit (PMU). Please see the PMU section of the reference manual for detail. Changing these bits results in changing of the startup time.

*4: The value is the evaluation data with the crystal (RIVER FCX-05 12.000 MHz) on Toshiba's evaluation board. Refer to the TZ1200 series System Design Guide for the other crystal value.

6.5.2. XOSC32K

6.5.2.1. Crystal Resonator

Table 6-13 XOSC32K characteristics (crystal resonator)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Oscillator Frequency	fO32K	—	—	32.768	—	kHz
External Feedback Resistor (*1)(*2)	Rf	—	—	—	—	MΩ
Startup Time (*1)(*4)	tSTART	CL = 3 pF, TRIMIN = Mode0 (*3)	—	—	150	ms
Frequency stabilization after Boost disable.	tSTBL	—	—	—	2	ms

*1: The value is based on evaluation result obtained with typical external components parameter. The value of these parameters varies depending on the crystal resonator used. It is recommended to refer the datasheet of the crystal resonator that you are going to use.

*2: TZ1200 series has the internal feedback resistor. It need not have external feedback resistor on board.

*3: TRIMIN is one of the fields of the control register ***[OVERRIDE_EFUSE_OSC32K_TRIMMING]*** in Power Management Unit (PMU). Please see the PMU section of the reference manual for detail. Changing these bits results in changing of the startup time

*4: The value is the evaluation data with the crystal (RIVER TFX-03 32.768 kHz) on Toshiba's evaluation board.

6.5.2.2. Crystal Oscillator

Table 6-14 XOSC32K characteristics (crystal oscillator)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
External Clock Frequency	fO32K	—	—	32.768	—	kHz
Low-level input current	IIL	VIN = VSS	-10	—	10	μA
High-level input current	IIH	VIN = VDD33	-10	—	10	μA
Low-level input voltage	VIL	—	—	—	VDD33 × 0.3	V
High-level input voltage	VIH	—	VDD33 × 0.7	—	—	V
Duty cycle	DU	—	35	—	65	%

6.5.3. SIOSC12M

Table 6-15 SIOSC12M characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Oscillator Frequency	fSO12M	Untrimmed	8	—	16	MHz
		Trimmed	11.7	12.0	12.3	MHz
Startup Time	tSTASO12M	—	—	1.3	3.9	μs

6.5.4. PLL

Table 6-16 PLL characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Output Clock Frequency	fCK	ND = 0b1001 (*1)	—	120	—	MHz
		ND = 0b0111 (*1)	—	96	—	MHz
		ND = 0b0011 (*1)	—	48	—	MHz
Reference Input Frequency	fFN	—	—	12	—	MHz
Lockup Time	tLU	TIMER_COUNT_BP = 0x0 (*2)	—	—	40	μs

*1: ND is one of the fields of the control register ***[CONFIG_PLL1]*** in Power Management Unit (PMU). Please see the PMU section of the reference manual for detail.

*2: TIMER_COUNT_BP are control resister ***[STARTUP_PLL]*** in Power Management Unit (PMU). Please see the PMU section of the reference manual for detail.

6.5.5. ADPLL

Table 6-17 ADPLL characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Output Clock Frequency	fCK	FCW = 0b0011100100 (*1) SELFREQR = 0b11000 (*1) SELFREQ = 0b0000 (*1) SELCP = 0b000 (*1)	—	119.573	—	MHz
		FCW = 0b0101101110 (*1) SELFREQR = 0b01000 (*1) SELFREQ = 0b0000 (*1) SELCP = 0b000 (*1)	—	95.944	—	MHz
		FCW = 0b0101101110 (*1) SELFREQR = 0b00000 (*1) SELFREQ = 0b0110 (*1) SELCP = 0b010 (*1)	—	47.972	—	MHz
Reference Input Frequency	fFN	—	—	32.768	—	kHz
Lockup Time	tLU	Normal Mode	—	—	8000	μs

*1: FCW, SELFREQR, SELFREQ, SELCP are control registers ***[CONFIG_ADPLL0]*** and ***[CONFIG_ADPLL1]*** in Power Management Unit (PMU).
Please see the PMU section of the reference manual for detail.

6.6. Analog Characteristics

6.6.1. POR

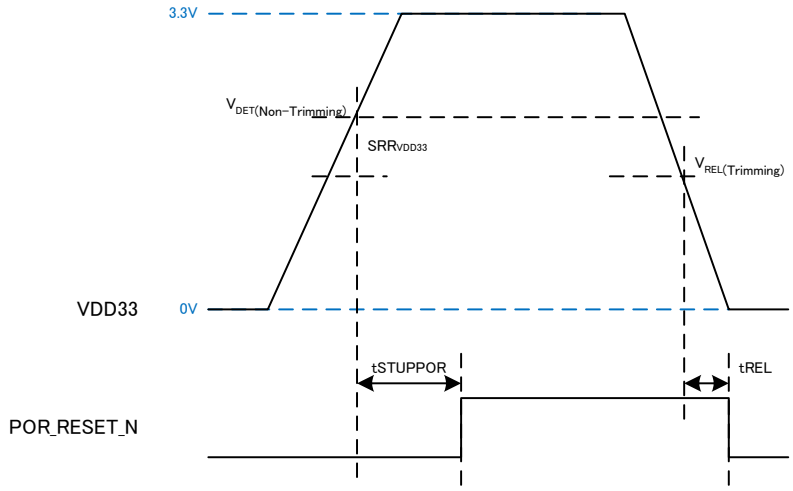


Figure 6-1 Reset Release by POR during power on

Table 6-18 POR characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Power supply Rising Slew Rate	SRRVDD33	VDD33 < 1.7 V	0.0018	—	0.18	V/μs
Power supply Falling Slew Rate	SRFVDD33	VDD33 < 1.7 V	-0.18	—	0	V/μs
Power-on Reset Voltage Rising Threshold	VDET	On VDD33 rising	1.18	—	1.64	V
Power-on Reset Voltage Falling Threshold	VREL	On VDD33 falling	1.49	1.54	1.59	V

POR is detected by VDET(Non-Trimming) during Non-trimming status. And then POR reset occurs after tSTUPPOR has passed. VDD33 voltage is VDET+SR_{VDD33}×tSTUPPOR. POR becomes Trimming status after CPU starts up. Therefore it may seems that VREL voltage is higher than VDET voltage.

Table 6-19 POR Timing Specification

Item	Min	Typ.	Max	Unit
tSTUPPOR	0.265	—	5	ms
tREL	—	—	1	ms

6.6.2. LVD

Table 6-20 LVD characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Power supply Rising Slew Rate	VSRR	VDD33 < 1.7 V	0.0018	—	0.18	V/μs
Power supply Falling Slew Rate	VSRF	VDD33 < 1.7 V	-0.18	—	0	V/μs
Brown-out Reset Voltage Threshold Setting Range	VBOR	On VDD33 falling (*1)	—	1.55 to 3.34	—	V
Brown-out Reset Voltage Threshold Accuracy	VBORA	(*2)	-50	—	+50	mV
		(*3)	-100	—	+100	mV
Hysteresis Voltage	VHYS	—	—	100	—	mV
Number of Steps for Voltage Threshold changing	BORSTEP	—	—	64	—	Steps
Step size	VBORSTEP	VBOR ≤ 1.8 V	—	8	—	mV
		VBOR > 1.8 V	—	48	—	mV

*1: Brown-out Reset Detect Level can be changed by register setting after system reset release.
*2: MSB of [OVERRIDE_EFUSE_LVD_TRIMMING].LVD is L.
*3: MSB of [OVERRIDE_EFUSE_LVD_TRIMMING].LVD is H.

LVD detecting threshold is 1.80+/-0.05V when [OVERRIDE_EFUSE_LVD_TRIMMING].LVD is set to “0x1F”.
To change the threshold setting, please check “4.8.3.3. Setting Change Procedure” in PMU Reference Manual.

6.6.3. DCDC

Table 6-21 DCDC characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Output Voltage	VOUT	Voltage Mode OverDrive	—	1.3	—	V
		Voltage Mode A	—	1.2	—	V
		Voltage Mode B	—	1.1	—	V

6.6.4. LDOS

Table 6-22 LDOS characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Output Voltage	VOUT	Voltage Mode D	—	0.9	—	V
Load Current	ILOAD	Voltage Mode D	—	—	5	mA

6.6.5. 12-bit SAR A/D converter

Table 6-23 12-bit SAR ADC characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resolution	—	—	—	12	—	Bits
Core Clock Frequency	fCLK	—	—	—	16	MHz
Conversion Time (*1)	—	Cycles in Core Clock	—	—	17	Cycles
Top Reference Voltage	VREFH	—	—	—	AVDD33	V
Bottom Reference Voltage	VREFL	—	0	—	—	V
Analog Input Configuration	—	—	Single-ended Voltage			—
Analog Input Range	VIN	AIN0, AIN1	VREFL	—	VREFH	V
		AIN2 ~ AIN15	VSSC	—	(*3)	V
Driving Source Impedance	ZINS	for AC signal input	—	—	250	Ω
		for DC signal input (*4)	See the Figure 6-3			—
Integral Nonlinearity	INL	—	—	±2	±4.5	LSB
Differential Nonlinearity	DNL	—	—	±1	±3	LSB
Offset Error	OE	See the Figure 6-2	—	±1	±18	LSB
Gain Error	GE	See the Figure 6-2	—	±3	±6	LSB
Operating Current (*2)	IDD	fCLK = 4 MHz	—	0.38	—	mA
		fCLK = 16 MHz	—	0.52	—	mA
Standby Current (*2)	IDDS	—	—	0.1	—	μA

*1: Required clock cycle of ADC core. Setup cycles of control logic are not included.

*2: The current of AVDD33 power supply.

*3: AVDD33 or VDD33 whichever is lower.

*4: If the ADC input signal is DC or very low frequency, the specification of the maximum driving source impedance is relaxed by adding an external capacitor(0.1μF) at each ADC input terminal.

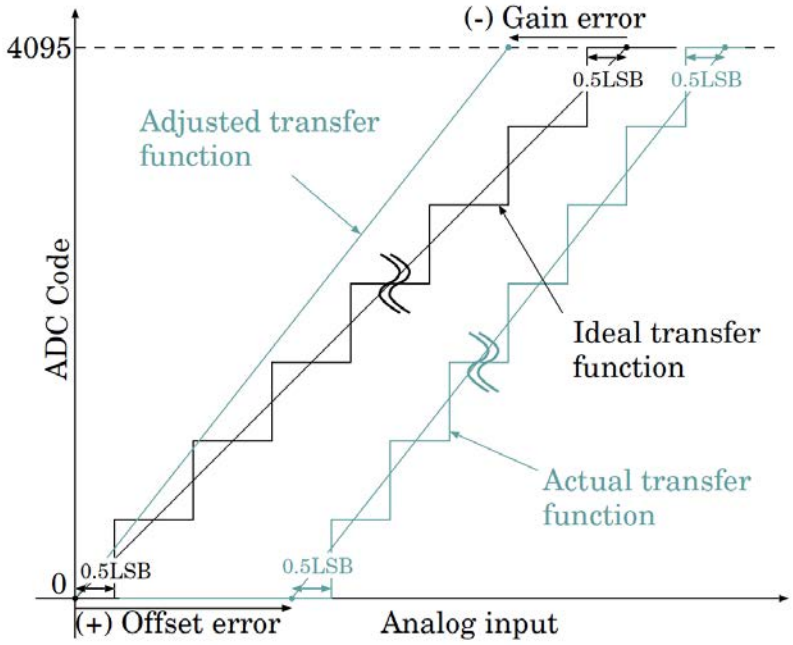
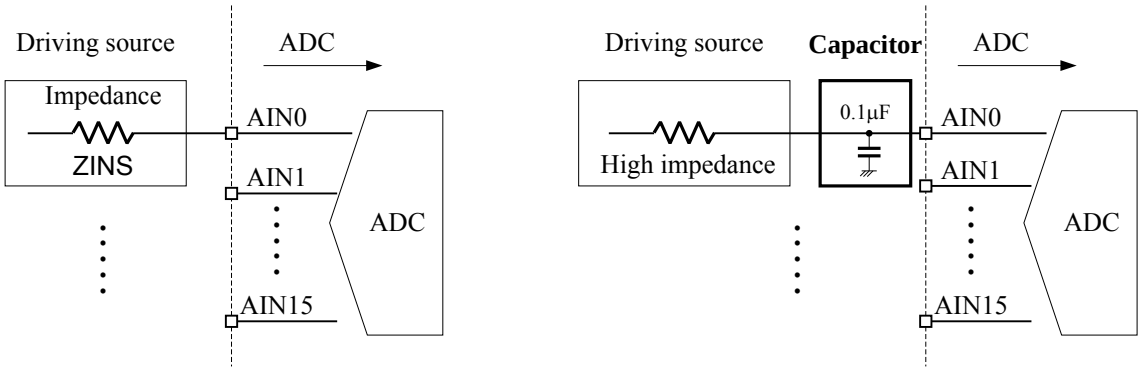


Figure 6-2 Specification Definition of Offset Error, Gain Error



AC signal input case
(Low impedance driving source)

DC signal input case
(High impedance driving source)

Figure 6-3 Configuration of Driving Source Impedance

6.6.6. Analog Front End

6.6.6.1. Configurable Amp, PGA, 24-bit ΔΣ A/D converter

Table 6-24 Analog Front End characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
General Specifications						
Resolution	—	—	—	24	—	Bits
Core Clock Frequency	fCLK	—	3.8	4	4.2	MHz
Conversion Time (*1) (Cycles in Core Clock)	—	CNT_MODE[1:0] (*2)	290, 546, 1058, 4130			Cycles
Gain Setting	GTOTAL	GAIN1 x GAIN2	x1, x2, x4, x8, x16, x32, x64, x128			V/V
Top Reference Voltage	VREFH	—	—	—	AVDD33	V
Bottom Reference Voltage	VREFL	—	0	—	—	V
Configurable Amplifier						
Voltage input-mode (Instrumentation Amplifier)						
Analog Input Configuration	—	CNT_MODE[8] = 0 (*2)	Differential Voltage			—
Analog Input Voltage Range	VIN	—	0.1 / GTOTAL	—	(AVDD33 - 0.1) / GTOTAL	V
Input Impedance	ZIN	—	20	35	—	MΩ
Configurable AMP Gain Setting	GAIN1	CNT_MODE[4:2] (*2)	x1, x2, x4			V / V
Common mode Rejection Ratio	CMRR	DC to 120 Hz	60	85	—	dB
Current input-mode (Trans Impedance Amplifier)						
Analog Input Configuration	—	CNT_MODE[8] = 1 (*2)	Differential Current			—
I/V Conversion Resistance	Rf	CNT_MODE[4:2] (*2)	10 k, 20k, 40k, 80k, 160k, 320k, 640k, 1M			Ω
I/V Conversion Resistance Tolerance	RfTOL	—	—	±20	—	%
Feedback Capacitance	Cf	CNT_MODE[7:5] (*2)	3, 6, 9, 12, 15, 18, 21, 24			pF
Feedback Capacitance Tolerance	CfTOL	—	—	±25	—	%
Maximum Input Current Range	IIN	—	±(VCM-0.1) / (Rf x GAIN2)	—	—	μA
Common mode Voltage	VCM	—	—	AVDD33/ 2	—	V
Programmable Gain Amplifier						
PGA Gain Setting	GAIN2	—	x1, x2, x4, x8, x16, x32			V / V
Gain Bandwidth (-3 dB)	GWgain	—	—	2 M	—	Hz
Operating Current	IDDPGA	—	—	0.5	—	mA
DC Performance						
Voltage input-mode (Instrumentation Amplifier)						
Output Noise	ONOISE_RMS	AIXP=AIXN=VCM (X=0,1,2,3)	See the Table 6-25 Output Noise characteristics (ONOISE_RMS)			—
Input-Referred Noise	INNOISE_RMS	AIXP=AIXN=VCM (X=0,1,2,3)	See the Table 6-26 Input-referred Noise characteristics (INNOISE_RMS)			—
Effective Number of Bits	ENOB_RMS	AIXP=AIXN=VCM (X=0,1,2,3)	See the Table 6-27 Input-referred ENOB characteristics (ENOB_RMS)			—

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Integral Nonlinearity	INL	AIXP – AIXN = VCM ± 0.2V GTOTAL=1	—	±75	±256	LSB
Offset Error	OE	AIXP=AIXN=VCM (X=0,1,2,3)	—	±10	±50	μV
Gain Error	GE	AIXP – AIXN = VCM ± 0.2V GTOTAL=1	—	±0.5	±1	%FS
Current input-mode (Trans Impedance Amplifier)						
Effective Number of Bits	ENOB_RMS	AIXP=AIXN=open Rf / Cf = 10kΩ / 24pF GAIN2=1, 4130-cycle	—	19.0	—	bits
Integral Nonlinearity	INL	IIN = ± 0.2V / 10kΩ Rf / Cf = 10kΩ / 24pF GAIN2 = 1, 4130-cycle	—	±75	—	LSB
Offset Error	OE	AIXP=AIXN=open Rf / Cf = 10kΩ / 24pF GAIN2=1, 4130-cycle	—	±10	—	μV
Gain Error (*3)	GE	IIN = ± 0.2V / 10kΩ Rf / Cf = 10kΩ / 24pF GAIN2 = 1, 4130-cycle	—	—	±20	%FS
Current Consumption						
Operating Current (*4)	IDD	Configurable AMP and 24-bit ΔΣ-ADC Active	—	1.1	—	mA
		Configurable AMP and PGA and 24-bit ΔΣ-ADC Active	—	1.6	—	mA
		Configurable AMP and PGA and Rectifier 24-bit ΔΣ-ADC Active	—	2.2	—	mA
Standby Current (*4)	IDDS	—	—	0.1	—	μA

*1: Required clock cycle of ADC core. Setup cycles of control logic are not included.

*2: CNT_MODE is a control register of ADC24 block. Please see the AFEZ section of the reference manual for detail.

*3: Gain Error includes variation in manufacturing processes.

*4: The current of AVDD33 power supply.

Table 6-25 Output Noise characteristics (ONOISE_RMS)

AIXP = AIXN = AVDD33/2 (X = 0, 1, 2, 3), AVDD33 = VREFH = 3.3 V, fCLK = 4 MHz, Ta = 25°C, no ac-noise on each power supply, unless otherwise noted.

Conversion frequency (time)	Configurable AMP Gain	x1	x2	x4						Unit
	PGA Gain	—	—	—	x2	x4	x8	x16	x32	
	Total Gain	**x1**	**x2**	**x4**	**x8**	**x16**	**x32**	**x64**	**x128**	
0.97ksps (4130 cycles)		11.75	11.69	12.99	15.76	25.68	45.59	88.30	176.9	μVrms
3.78ksps (1058 cycles)		24.77	24.36	27.81	33.97	52.31	97.02	183.1	372.6	
7.33ksps (546 cycles)		32.92	34.76	39.36	48.64	75.96	139.4	269.9	538.8	
13.8ksps (290 cycles)		45.94	44.91	60.14	62.51	102.3	161.8	299.5	615.7	

Table 6-26 Input-referred Noise characteristics (INNOISE_RMS)

AIXP = AIXN = AVDD33/2 (X = 0, 1, 2, 3), AVDD33 = VREFH = 3.3 V, fCLK = 4 MHz, Ta = 25°C, no ac-noise on each power supply, unless otherwise noted.

Conversion frequency (time)	Configurable AMP Gain	x1	x2	x4						Unit
	PGA Gain	—	—	—	x2	x4	x8	x16	x32	
	Total Gain	**x1**	**x2**	**x4**	**x8**	**x16**	**x32**	**x64**	**x128**	
0.97ksps (4130 cycles)		11.75	5.85	3.25	1.97	1.60	1.42	1.38	1.38	μVrms
3.78ksps (1058 cycles)		24.77	12.18	6.95	4.25	3.27	3.03	2.86	2.91	
7.33ksps (546 cycles)		32.92	17.38	9.84	6.08	4.75	4.36	4.22	4.21	
13.8ksps (290 cycles)		45.94	22.46	15.04	7.81	6.40	5.06	4.68	4.81	

Table 6-27 Input-referred ENOB characteristics (ENOB_RMS)

AIXP = AIXN = AVDD33/2 (X = 0, 1, 2, 3), AVDD33 = VREFH = 3.3 V, fCLK = 4 MHz, Ta = 25°C, no ac-noise on each power supply, unless otherwise noted.

Conversion Time	Configurable AMP Gain	x1	x2	x4						Unit
	PGA Gain	—	—	—	x2	x4	x8	x16	x32	
	Total Gain	**x1**	**x2**	**x4**	**x8**	**x16**	**x32**	**x64**	**x128**	
0.97ksps (4130 cycles)		19.1	20.0	20.8	21.7	22.0	22.1	22.2	22.2	Bits
3.78ksps (1058 cycles)		18.0	19.0	19.7	20.6	20.9	21.1	21.1	21.1	
7.33ksps (546 cycles)		17.6	18.4	19.2	20.1	20.4	20.5	20.6	20.6	
13.8ksps (290 cycles)		17.1	17.8	18.7	19.7	20.0	20.3	20.4	20.4	

Full-Scale Range = 2 * VREFH

INNOISE_RMS = ONOISE_RMS / Total Gain

ENOB_RMS = ln(Full-Scale Range / INNOISE_RMS) / ln(2)

6.6.6.2. OPAMPs

Table 6-28 Operational Amplifier characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
RLDAMP						
Input Range	VIN	—	0.1	—	AVDD33 - 0.1	V
Output Swing	FS	—	0.1	—	AVDD33 - 0.1	V
Input Resistor	R_{RLD}	SEL_RLDR[1:0] (*1)	0, 50k, 150k, 1M			Ω
Input Resistor Tolerance	R_{RLD}TOL	—	—	±20	—	%
Output Capacitance Load	CLOAD	—	—	—	1	nF
Output Resistance Load	RLOAD	—	1M	—	—	Ω
Offset Error	OE	—	—	—	±10	mV
Output Noise1	ON1	Noise bandwidth: 0.1 to 100 Hz	—	(10)	—	μV
Output Noise2	ON2	Noise Frequency: 1 kHz	—	(60)	—	nV / $\sqrt{\text{Hz}}$
Gain band width product	GBW	—	—	(2)	—	MHz
Total Harmonic Distortion	THD	FIN = 1 kHz, VIN = FS	—	(-72)	—	dBc
		FIN = 200 kHz, VIN = FS	—	(-50)	—	dBc
Operating Current	IDD	—	—	0.3	—	mA
ZAMP						
Input Range	VIN	—	0.1	—	AVDD33 -0.1	V
Output Swing	FS	—	0.1	—	AVDD33 -0.1	V
Internal Feedback Resistor	R_Z	CNT_MODE[13:12] (*3)	0, 18k, 36k, 1.375M			Ω
Internal Feedback Resistor Tolerance	R_ZTOL	—	—	±20	—	%
Offset Error	OE	—	—	—	±10	mV
Output Noise1	ON1	Noise bandwidth: 0.1 to 100 Hz	—	(10)	—	μV
Output Noise2	ON2	Noise Frequency: 1 kHz	—	(60)	—	nV / $\sqrt{\text{Hz}}$
Gain band width product	GBW	—	—	(2)	—	MHz
Total Harmonic Distortion	THD	FIN = 1 kHz, VIN = FS	—	(-72)	—	dBc
		FIN = 200 kHz, VIN = FS	—	(-50)	—	dBc
Operating Current	IDD	—	—	0.3	—	mA

*1: SEL_RLDR is a control register of AFEZ block. Please see the AFEZ section of the reference manual for detail.

*2: The characteristics shown in () is based on device characterization (Not production tested).

*3: Controlled by CNT_MODE[13:12] which is a control register of AFEZ block. Please see the AFEZ section of the reference manual for detail.

6.6.6.3. DC Impedance Measurement

The DC impedance measurement excited by DC current is structured by 12-bit DAC, ZAMP with internal resistor (Rz) , VCM generator, Configurable AMP, PGA, 24-bit ΔΣ A/D converter. The DC excitation current is generated by 12-bit DAC, ZAMP with internal Rz and VCM generator. When the current is applied to an object to be measured, DC voltage is generated between two terminals of the object depending on the impedance of the object. The voltage can be digitized by the 24-bit A/D converter and then the impedance of the object can be calculated from the measured voltage value and the excitation current value.

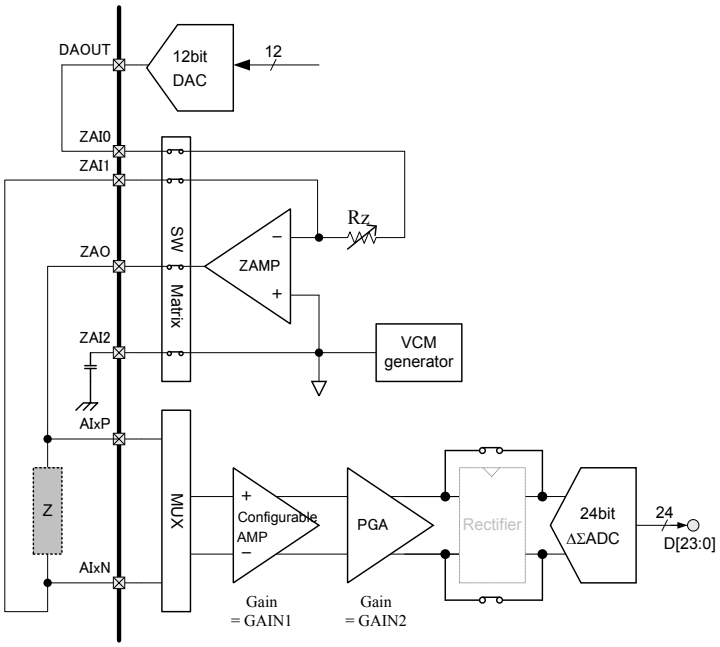


Figure 6-4 DC Impedance Measurement block diagram

Table 6-29 DC Impedance Measurement characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Impedance measurement range1 (CNT_MODE[13:12]=01 : Rz=18kΩ)						
Dynamic Range	RRANGE1	—	—	—	13k	Ω
Absolute Error (*1)	RAE1	—	—	—	±20	%
Integral Non-Linearity	RINL1	—	—	0.01	—	%FS
Repeatability Error (*2)	RRE1	Measured Z=510Ω GAIN1=x1, GAIN2=x1 ZAI0 = 0.96 * AVDD33	—	0.03	—	%rms
		Measured Z=10kΩ GAIN1= x1, GAIN2= x1 ZAI0 = 0.96 * AVDD33	—	0.01	—	%rms
Impedance measurement range2 (CNT_MODE[13:12]=11 : Rz=1.375MΩ)						
Dynamic Range	RRANGE2	—	—	—	1M	Ω
Absolute Error (*1)	RAE2	—	—	—	±20	%
Integral Non-Linearity	RINL2	—	—	0.02	—	%FS
Repeatability Error (*2) (*3)	RRE2	Measured Z=1MΩ GAIN1= x1, GAIN2= x1 ZAI0 = 0.96 * AVDD33	—	0.02	—	%rms

*1: Absolute Error includes variation in manufacturing processes and depends strongly on the resistance variation of internal resistor Rz to generate the excitation current.

*2: If the DC voltage to generate the DC excitation current is supplied into ZAI0 pin from the 12-bit DAC, the full scale voltage of the 12-bit DAC is 0.96*AVDD33.

*3: The Repeatability Error is defined by a standard deviation of 1000 measurement results.

6.6.6.4. AC Impedance Measurement

The AC impedance measurement excited by AC current is structured by DDS, 12-bit DAC, ZAMP with internal resistor (Rz) , VCM generator, Configurable AMP, PGA, Rectifier, 24-bit ΔΣ A/D converter. The AC excitation current is generated by DDS, 12-bit DAC, ZAMP with internal Rz and VCM generator. When the current is applied to an object to be measured, AC voltage swing is generated between two terminals of the object depending on the impedance of the object. After the peak voltage of the AC voltage is detected by the rectifier, the peak voltage can be digitized by 24-bit A/D converter and then the impedance of the object can be calculated from the measured voltage value and the excitation current amplitude value.

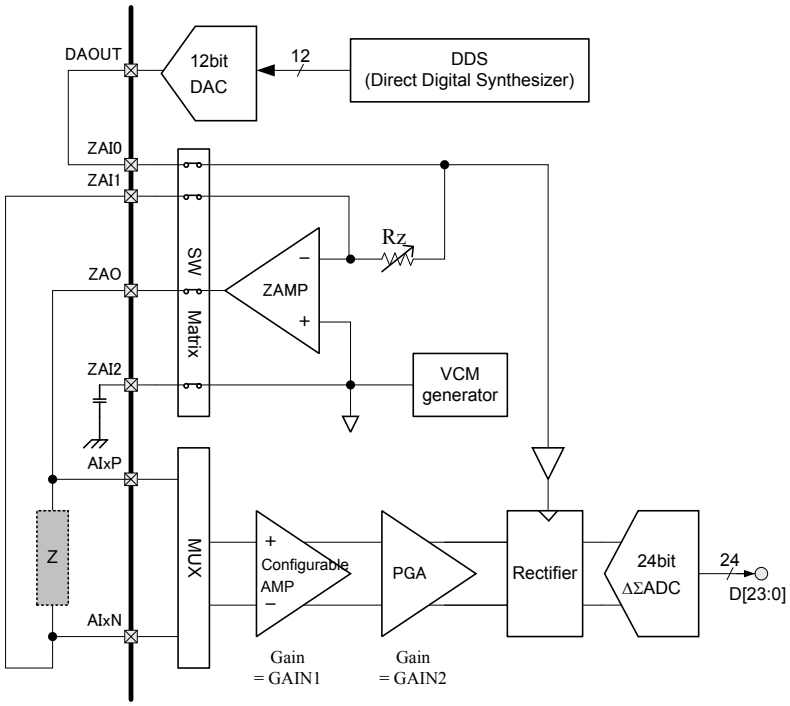


Figure 6-5 AC Impedance measurement block diagram

Table 6-30 AC Impedance Measurement characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Impedance measurement range1 (CNT_MODE[13:12]=01 : Rz=18kΩ)						
Excitation frequency range	FEXT	—	20	—	200k	Hz
Rectifier Differential Input Range (*1)	ZRIND	—	256	—	—	mV
Integral Non-Linearity	ZINL	FEXT=200kHz Including Rectifier, without ZAMP	—	0.4	—	%FS
Dynamic Range	ZRANGE1	20Hz < FEXT < 200kHz	—	—	13k	Ω
Absolute Error (*2)	ZAE1	—	—	—	±20	%
Repeatability Error (*3) (*4) (*5)	RRE1	Measured Z=510Ω, FEXT=5kHz GAIN1=x4, GAIN2=x8 Amplitude of ZAI0 = 0.92 * AVDD33	—	0.2	—	%rms
		Measured Z=510Ω, FEXT=50kHz GAIN1=x4, GAIN2=x8 Amplitude of ZAI0 = 0.92 * AVDD33	—	0.3	—	%rms
		Measured Z=510Ω, FEXT=200kHz	—	0.5	—	%rms

		GAIN1=x4, GAIN2=x8 Amplitude of ZAI0 = 0.92 * AVDD33				
Impedance measurement range2 (CNT_MODE[13:12]=11 : Rz=1.375MΩ)						
Excitation frequency range	FEXT	—	20	—	5k	Hz
Rectifier Differential Input Range (*1)	ZRIND	—	256	—	—	mV
Integral Non-Linearity	ZINL	FEXT=200kHz Including Rectifier, without ZAMP	—	0.4	—	%FS
Dynamic Range	ZRANGE2	20Hz < FEXT < 5kHz	—	—	1M	Ω
Absolute Error (*2)	ZAE2	—	—	—	±20	%
Repeatability Error (*3) (*4) (*5)	RRE2	Measured Z=1MΩ, FEXT=250Hz GAIN1=x1, GAIN2=x1 Amplitude of ZAI0 = 0.92 * AVDD33	—	0.1	—	%rms

*1: If the AC voltage swing which is generated between two terminals of the object is small, each voltage gain of Configuration AMP (GAIN1) and PGA (GAIN2) has to be set larger in order to satisfy the specification of the Rectifier Differential Input Range(more than 256mV) unless ADC output code has been clipped.

*2: Absolute Error includes variation in manufacturing processes and depends strongly on the resistance variation of internal resistor Rz to generate the excitation current.

*3: If the AC voltage to generate the AC excitation current is supplied into ZAI0 pin from the 12-bit DAC, the full scale voltage amplitude is 0.92*AVDD33.

*4: The Repeatability Error is defined by a standard deviation of 1000 data which is the average value of twice measurement results.

*5: Twice or more and even number of continuous A/D conversion an AC impedance measurement using the Rectifier is needed for accurate measurement, since the measurement results using the Rectifier are divided into 2 groups according to number of measurements.

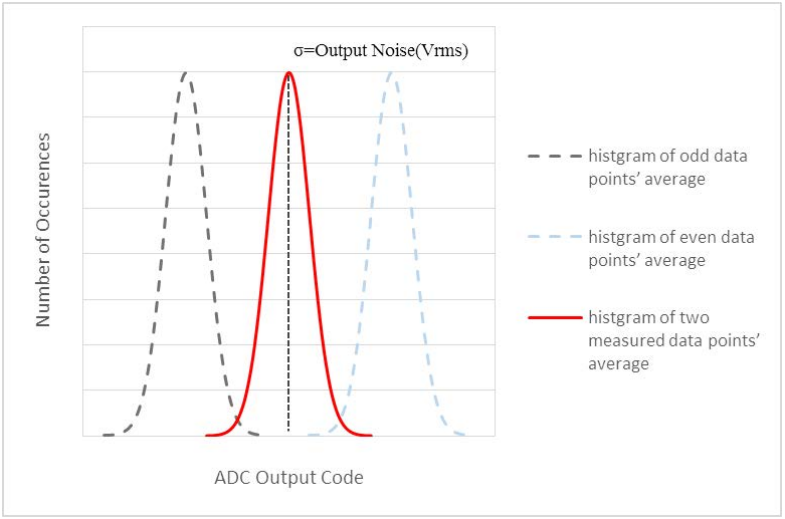


Figure 6-6 Histogram of AC Impedance measurement data

6.6.7. 12-bit D/A converter

Table 6-31 12-bit DAC characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resolution	—	—	—	12	—	Bits
Core Clock Frequency	fCLK	—	—	—	4	MHz
Top Reference Voltage	VREFH	—	—	—	AVDD33	V
Bottom Reference Voltage	VREFL	—	0	—	—	V
Minimum Analog Output Voltage	VMIN	VREFH = AVDD33, VREFL = AVSS33 = 0 V	—	VREFH*0.04	—	V
Maximum Analog Output Voltage	VMAX	VREFH = AVDD33, VREFL = AVSS33 = 0 V	—	VREFH*0.96	—	V
Common-Mode Voltage	VCM	VREFH = AVDD33, VREFL = AVSS33=0 V	—	VREFH*0.5	—	V
Load Capacitance	CLOAD	—	—	—	50	pF
Load Resistance	RLOAD	—	10	—	—	kΩ
Integral Non-Linearity	INL	—	—	±2	±5	LSB
Differential Non-Linearity	DNL	—	—	±0.5	±2.5	LSB
Settling Time (*1)	STLT	CLOAD = 50 pF, RLOAD = 10 kΩ	—	1	—	μs
Total Harmonic Distortion(*2)	THD	Output frequency = 1 kHz	—	-60	—	dBc
		Output frequency = 50 kHz	—	-50	—	dBc
		Output frequency = 100 kHz	—	-42	—	dBc
		Output frequency = 200 kHz	—	-35	—	dBc
Operating Current	IDD	No LOAD	—	0.34	—	mA
Standby Current	IDDS	No LOAD	—	0.1	—	μA

*1: The Settling time is defined by the time for a 12-bit input code transition between the lowest (0x000) and the highest (0xFFF) input codes when DAOUT reaches final value ±0.5LSB.

*2: The specification of Total Harmonic Distortion is defined under 4MHz core clock frequency.

6.6.8. LED current drive D/A converter

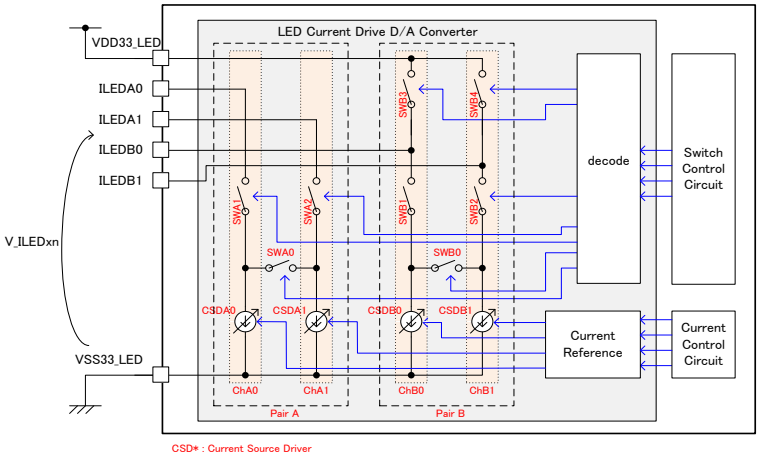


Figure 6-7 Block diagram of LED Current Drive D/A converter

Each channel consists of an output pin ILEDxn (x =A or B, n = 0 or 1), a current source driver (CSDxn), and a vertical switch between the output pin and the current source driver (SWx1/2), and a vertical switch between the output pin and VDD33_LED power (SWx3/4). ChA0 and ChA1 are connected through a bridge switch (SWA0) to configure a pair. ChB0 and ChB1, through a bridge switch (SWB0), too. The combination of ChA0 and ChA1 is called Pair-A, and the combination of ChB0 and ChB1, Pair-B. (Only Pair-B has SWB3 and SWB4 in this product.)

Table 6-32 LED current drive DAC characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resolution	—	—	—	8	—	Bits
Output Current Range	ILEDOUT	Full scale	—	25	—	mA
Output Current Absolute Error	IERROR	V_ILEDxn=1.0V (*1)	—	±15	—	%
Differential Non-Linearity	DNL	V_ILEDxn=1.0V (*1)	—	—	±0.5	LSB
Voltage headroom dependency	VDEPEND	See the Figure 6-8 Output current (Full scale) vs Voltage headroom (*1)				—
Temperature dependency	TDEPEND	See the Figure 6-9 Output current (Full scale) vs Temperature				—
Output current channel mismatch	CHMIS	V_ILEDxn=1.0V (*1)	—	—	±1	%
Operating Current	IDD	At output current = 0 mA	—	0.2	—	mA
Standby Current	IDDS	At output current = 0 mA	—	0.1	—	μA

*1: Voltage headroom (V_ILEDxn : x =A or B, n = 0 or 1) is defined by the difference between the output terminal (ILEDxn) voltage and VSS33_LED.

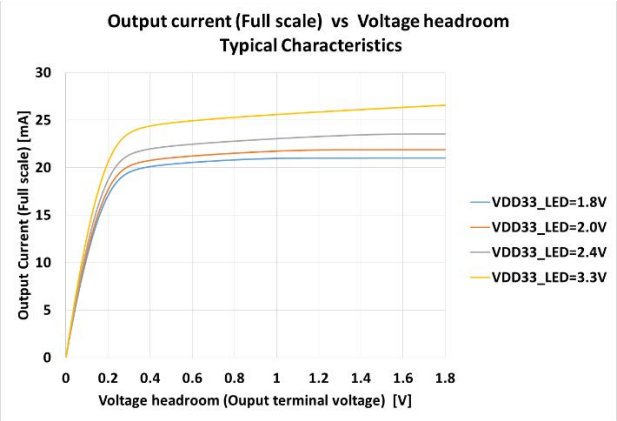


Figure 6-8 Output current (Full scale) vs Voltage headroom

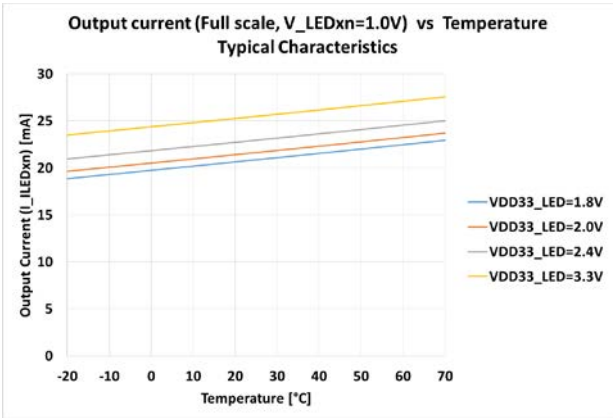


Figure 6-9 Output current (Full scale) vs Temperature

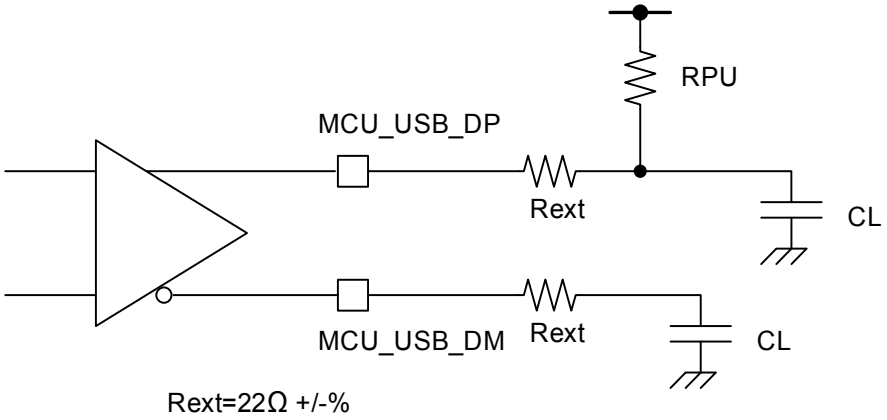
6.6.9. USB Full Speed IO

Table 6-33 USB FSIO characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Differential Drivers Cross Over Voltage	VCRS	—	1.3	—	2.0	V
Differential Input Sensitivity	VDI	—	200	—	—	mV
Differential Common Mode Range	VCM	—	0.8	—	2.5	V
Single Ended Receiver Input Range	VSER	—	0.8	—	2.0	V
Single Ended Receiver Hysteresis	VSHSYT	—	200	—	—	mV
Input Voltage Low	VIL	—	—	—	0.8	V
Input Voltage High	VIH	—	2.0	—	—	V
Output Voltage Low	VOL	—	0.0	—	0.3	V
Output Voltage High	VOH	—	2.8	—	VDD33_USB	V
Full Speed Driver Rise Time	TFR	Rext = 1.5 kΩ, CL = 50 pF (*1)	4	—	20	ns
Full Speed Driver Fall Time	TFF	Rext = 1.5 kΩ, CL = 50 pF (*1)	4	—	20	ns
Full Speed Operating Current (*2)	ICCFS	VDD33_USB = 3.3 V	—	8.5	—	mA
Suspended Supply Current (*2)	ICCS	VDD33_USB = 3.3 V	—	25	—	μA

*1: Figure below illustrates external loading for Full Speed Driver Rise/Fall time.

*2: The current of VDD33_USB power supply.



6.6.10. MIPI DPHY

Table 6-34 MIPI HSTX DC specifications

Symbol	Description	Condition	Min	Typ.	Max	Unit
HS mode						
VCMTX	HS transmit static common mode voltage	—	150	200	250	mV
|ΔVCMTX(1,0)|	VCMTX mismatch when output is Differential-1 or Differential-0	—	—	—	5	mV
|VOD|	HS transmit differential voltage	—	140	200	270	mV
|ΔVOD|	VOD mismatch when output is Differential-1 or Differential-0	—	—	—	10	mV
VOHHS	HS output high voltage	—	—	—	360	mV
ZOS	Single ended output impedance	—	40	50	62.5	Ω
ΔZOS	Single ended output impedance mismatch	—	—	—	10	%

Table 6-35 MIPI LPTX DC specifications

Symbol	Description	Condition	Min	Typ.	Max	Unit
VOH	Output high level	—	1.1	1.2	1.3	V
VOL	Output low level	—	-50	—	50	mV
ZOLP	Output impedance of LP transmitter	—	110	—	—	Ω

Table 6-36 MIPI LPRX DC Characteristics

Symbol	Description	Condition	Min	Typ.	Max	Unit
VIL	Input low threshold	Not in ULP st.	—	—	550	mV
VIL-UPS	Input low threshold in ULP state	—	—	—	300	mV
VIH	Output high threshold	—	880	—	—	mV
VHYST	Input hysteresis	—	25	—	—	mV

Table 6-37 MIPI HSTX AC specification

Symbol	Description	Condition	Min	Typ.	Max	Unit
ΔVCMTX (HF)	VCMTX variation above 450 MHz	RMS value	—	—	15	mV
ΔVCMTX (LF)	VCMTX variation between 50 and 450 MHz	Peak value	—	—	25	mV
tR and tF	20%–80% rise and fall time	—	—	—	0.3	UI
			150	—	—	ps

Table 6-38 MIPI LPTX AC specification

Symbol	Description	Condition	Min	Typ.	Max	Unit
TRLP/TFLP	15%-85% rise time and fall time	—	—	—	25	ns
TREOT	30%-85% rise time and fall time	—	—	—	35	ns
∂V/∂tSR	Slew rate	CLOAD = 0 pF	—	—	500	mV/ns
		CLOAD = 5 pF	—	—	300	mV/ns
		CLOAD = 20 pF	—	—	250	mV/ns
		CLOAD = 70 pF	—	—	150	mV/ns
		CLOAD = 0 to 70 pF, (Falling edge only)	30	—	—	mV/ns
		CLOAD = 0 to 70pF, (Rising edge only, output voltage 400 to 700 mV)	30	—	—	mV/ns
		CLOAD = 0 to 70pF, (Rising edge only, output voltage 700 to 930 mV, Vx is equal instantaneous output voltage minus 700 mV)	30-0.075 *Vx	—	—	mV/ns
CLOAD	Load capacitance	—	0	—	70	pF

Table 6-39 MIPI LPRX AC specification

Symbol	Description	Condition	Min	Typ.	Max	Unit
eSPIKE	Input pulse rejection	—	—	—	300	V*ps
TMIN-RX	Minimum pulse width response	—	20	—	—	ns
VINT	Peak interference amplitude	—	—	—	200	mV
fINT	Interference frequency	—	450	—	—	MHz

Table 6-40 MIPI PLL characteristics

Symbol	Description	Condition	Min	Typ.	Max	Unit
tLU	Lockup time	—	—	—	300	µs

6.7. AC Characteristics

6.7.1. RESET Input

Table 6-41 RESET Input Timing Requirement

Parameter	symbol	condition	Min	Typ.	Max	Unit
MCU_SYS_RESET_N assertion time	tRST	—	0.2	—	—	μs

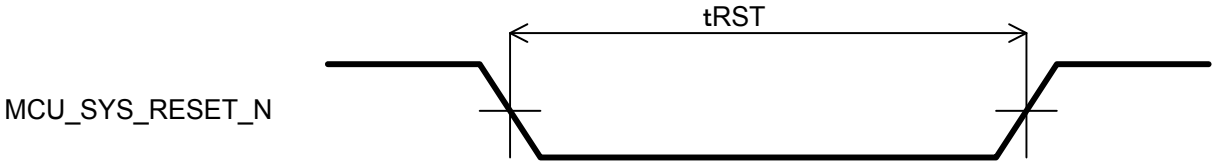


Figure 6-10 RESET Input Timing

6.7.2. GPIO Input

Table 6-42 GPIO Input Timing Requirement

Parameter	symbol	condition	Min	Typ.	Max	Unit
High level assertion time for wakeup (*1)	tHWU	—	0.2	—	—	μs
Low level assertion time for wakeup (*1)	tLWU	—	0.2	—	—	μs

*1: applied to GPIOm_n (m = 0–3, n = 0–31)

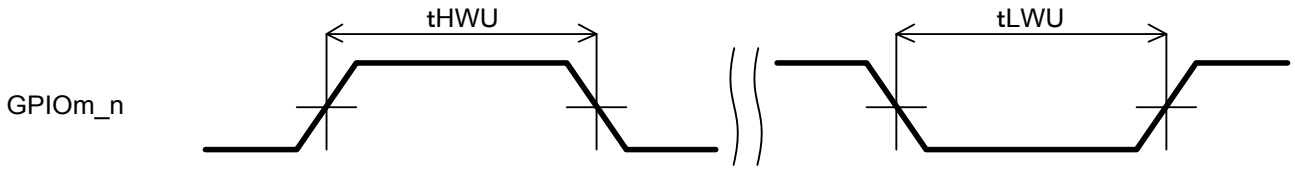


Figure 6-11 GPIO Input Timing

6.7.3. SPIM Interface

Table 6-43 SPI Interface Timing Requirement (1.65V <= VDD33 < 3.0V)

Parameter	symbol	condition	Min	Typ.	Max	Unit
SPI clock frequency	fSPCLK	Voltage Mode Overdrive	—	—	15	MHz
		Voltage Mode A, B	—	—	12	MHz
		Voltage Mode D	—	—	3	MHz
SPI input data setup time	tSPS	Voltage Mode Overdrive. {CTL2,CTL1} = 0b01, 0b10, 0b11. (*1) CL: Max 44pF (on SPIMn_CLK, n=0,1,2). CL: Max 27pF(on SPIM3_CLK).	4	—	—	ns
		Voltage Mode A, B. Same as Overdrive.	10	—	—	ns
		Voltage Mode D. Same as Overdrive.	135	—	—	ns
SPI input data hold time	tSPH	Voltage Mode Overdrive {CTL2,CTL1} = 0b01, 0b10, 0b11. (*1) CL: Min 9pF (on SPIMn_CLK, n=0,1,2,3).	34	—	—	ns
		Voltage Mode A, B. Same as Overdrive.	42	—	—	ns
		Voltage Mode D. Same as Overdrive.	167	—	—	ns
SPI output data delay time	tSPD	Voltage Mode Overdrive. {CTL2,CTL1} = 0b01, 0b10, 0b11 (*1). CL: Max 44pF, Min 9pF (on SPIMn_CLK, SPIMn_MOSI, n=0,1,2). CL: Max 27pF, Min 9pF (on SPIM3_CLK, SPIM3_MOSI). CL: Max 11pF, Min 9pF (on SPIMn_CS_N, n=0,1,2,3).	-10	—	17	ns
		Voltage Mode A, B. Same as Overdrive.	-18	—	26	ns
		Voltage Mode D Same as Overdrive.	-145	—	151	ns

*1: CTL2, CTL1 is a control register of GCONF block. Please see the GCONF section of the reference manual for detail.

Table 6-44 SPI Interface Timing Requirement (3.0V <= VDD33 < 3.6V)

Parameter	symbol	condition	Min	Typ.	Max	Unit
SPI clock frequency	fSPCLK	Voltage Mode Overdrive	—	—	15	MHz
		Voltage Mode A, B	—	—	12	MHz
		Voltage Mode D	—	—	3	MHz
SPI input data setup time	tSPS	Voltage Mode Overdrive. {CTL2,CTL1} = 0b01, 0b10, 0b11. (*1) CL: Max 44pF (on SPIMn_CLK, n=0,1,2). CL: Max 27pF(on	1	—	—	ns

		SPIM3_CLK).				
		Voltage Mode A, B. Same as Overdrive.	10	—	—	ns
		Voltage Mode D. Same as Overdrive.	135	—	—	ns
SPI input data hold time	tSPH	Voltage Mode Overdrive {CTL2,CTL1} = 0b01, 0b10, 0b11. (*1) CL: Min 9pF (on SPIMn_CLK, n=0,1,2,3).	34	—	—	ns
		Voltage Mode A, B. Same as Overdrive.	42	—	—	ns
		Voltage Mode D. Same as Overdrive.	167	—	—	ns
SPI output data delay time	tSPD	Voltage Mode Overdrive. {CTL2,CTL1} = 0b01, 0b10, 0b11 (*1). CL: Max 44pF, Min 9pF (on SPIMn_CLK, SPIMn_MOSI, n=0,1,2). CL: Max 27pF, Min 9pF (on SPIM3_CLK, SPIM3_MOSI). CL: Max 11pF, Min 9pF (on SPIMn_CS_N, n=0,1,2,3).	-10	—	17	ns
		Voltage Mode A, B. Same as Overdrive.	-18	—	26	ns
		Voltage Mode D Same as Overdrive.	-145	—	151	ns

*1: CTL2, CTL1 is a control register of GCONF block. Please see the GCONF section of the reference manual for detail.

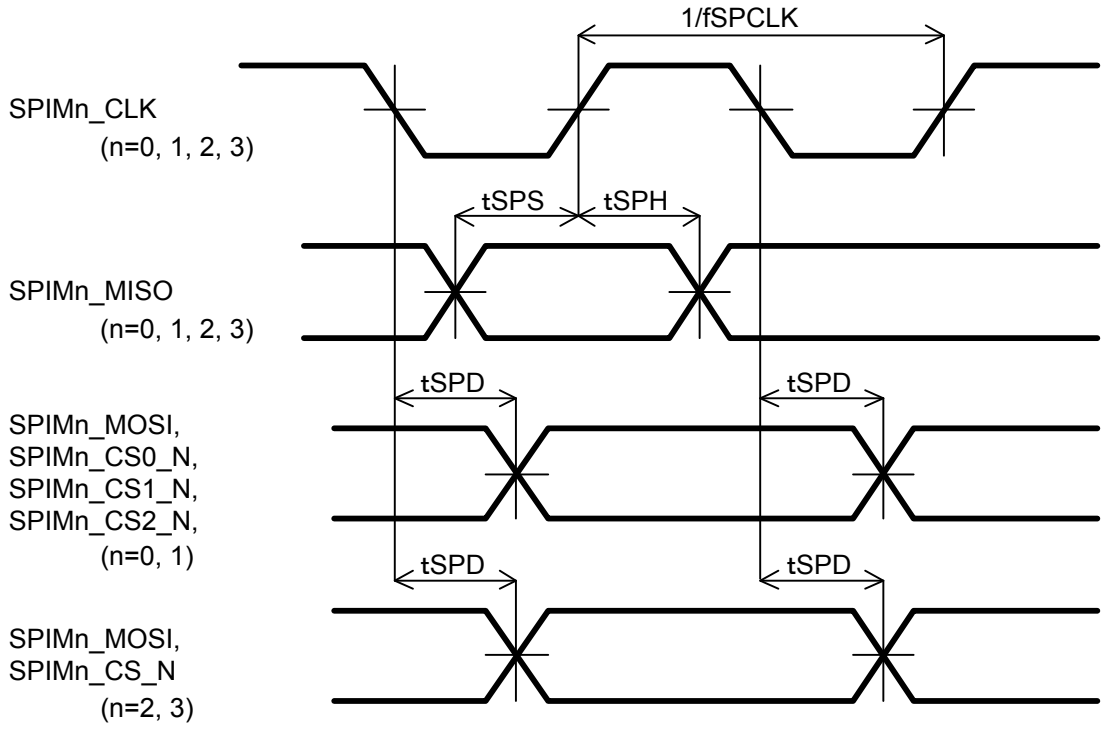


Figure 6-12 SPI Interface Timing

6.7.4. I2C Interface

- Standard Speed (100 kHz)

Table 6-45 I2C Interface Standard Speed (100 kHz) Timing Requirement

Parameter	symbol	condition	Min	Typ.	Max	Unit
I2C SCL clock frequency (*1)	fSCL	—	—	—	100	kHz
Low period of I2C SCL clock	fLOW	—	4.7	—	—	μs
High Period of I2C SCL clock	fHIGH	—	4.0	—	—	μs
Rise time of both SDA and SCL signals	tr	—	—	—	1000	ns
Fall time of both SDA and SCL signals	tf	—	—	—	300	ns
I2C Data setup time	tSU: DAT	—	250	—	—	ns
I2C Data Hold Time	tHD: DAT	—	0	—	—	μs
Set-up time for a repeated START condition	tSU: STA	—	4.7	—	—	μs
Hold time (repeated) START condition	tHD: STA	—	4.0	—	—	μs
Set-up time for STOP condition	tSU: STO	—	4.0	—	—	μs
capacitive load for each bus line	Cb	—	—	—	400	pF

- Fast Speed (400 kHz)

Table 6-46 I2C Interface Fast Speed (400 kHz) Timing Requirement

Parameter	symbol	condition	Min	Typ.	Max	Unit
I2C SCL clock frequency (*1)	fSCL	—	—	—	400	kHz
Low period of I2C SCL clock	fLOW	—	1.3	—	—	μs
High Period of I2C SCL clock	fHIGH	—	0.6	—	—	μs
Rise time of both SDA and SCL signals	tr	—	20	—	300	ns
Fall time of both SDA and SCL signals	tf	—	—	—	300	ns
I2C Data setup time	tSU: DAT	—	100	—	—	ns
I2C Data Hold Time	tHD: DAT	—	0	—	—	μs
Set-up time for a repeated START condition	tSU: STA	—	0.6	—	—	μs
Hold time (repeated) START condition	tHD: STA	—	0.6	—	—	μs
Set-up time for STOP condition	tSU: STO	—	0.6	—	—	μs
capacitive load for each bus line	Cb	—	—	—	400	pF

- Fast Mode Plus (1 MHz)

Table 6-47 I2C Interface Fast Mode Plus (1 MHz) Timing Requirement

Parameter	symbol	condition	Min	Typ.	Max	Unit
I2C SCL clock frequency (*1)	fSCL	—	—	—	1000	kHz
Low period of I2C SCL clock	fLOW	—	0.5	—	—	μs
High Period of I2C SCL clock	fHIGH	—	0.26	—	—	μs
Rise time of both SDA and SCL signals	tr	—	—	—	120	ns
Fall time of both SDA and SCL signals	tf	—	—	—	120	ns
I2C Data setup time	tSU: DAT	—	50	—	—	ns
I2C Data Hold Time	tHD: DAT	—	0	—	—	μs
Set-up time for a repeated START condition	tSU: STA	—	0.26	—	—	μs
Hold time (repeated) START condition	tHD: STA	—	0.26	—	—	μs
Set-up time for STOP condition	tSU: STO	—	0.26	—	—	μs

*1: Frequency of I2C serial clock (ic_clk) must be at least 4 MHz for Standard mode operation, at least 12 MHz for Fast mode operation, and at least 36 MHz for Fast Mode operation.

*2: Need proper setting of I2C control register. Please see the I2C section of the reference manual for detail.

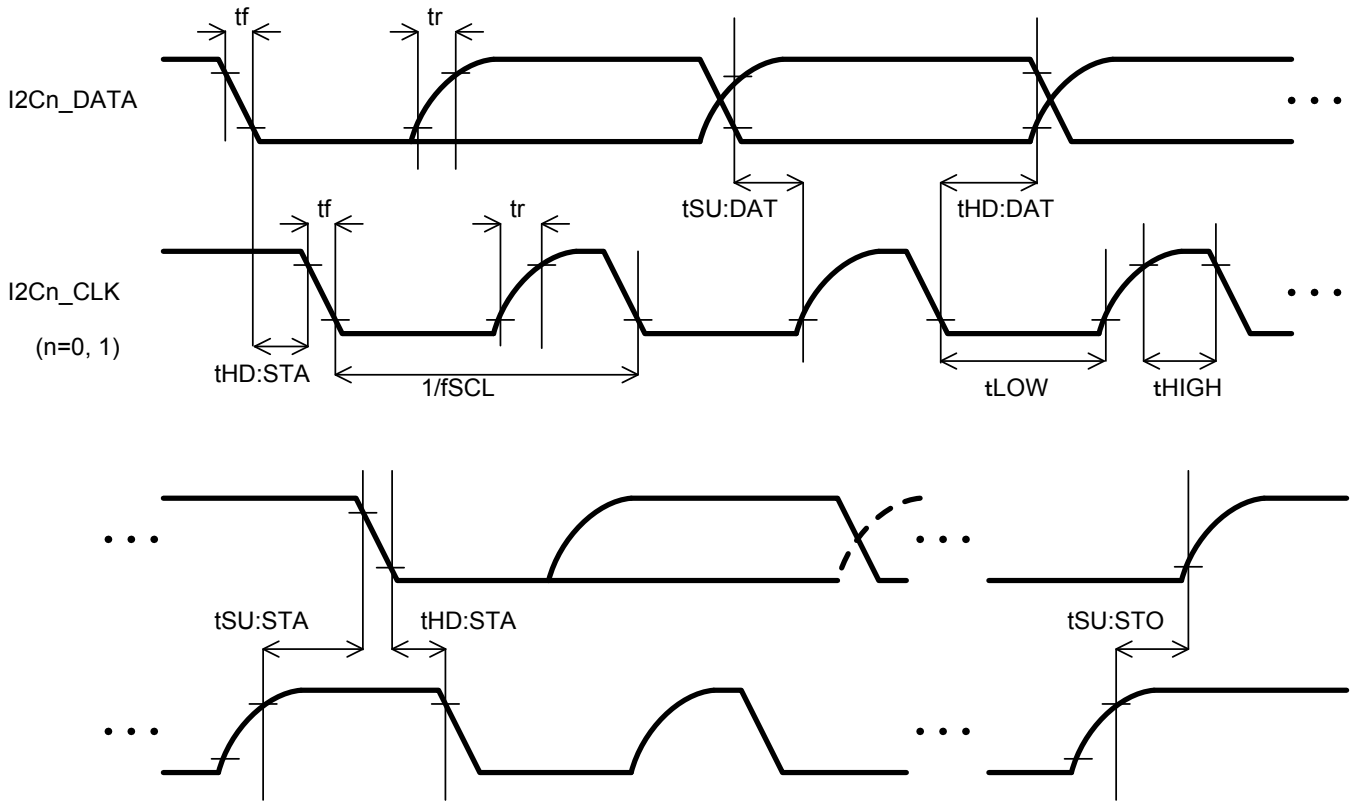


Figure 6-13 I2C Interface Timing

Most of the I2C timing requirements listed in above table needs appropriate setting of I2C control registers. Please see the I2C section of the reference manual for detail.

6.7.5. DEBUG Interface

- Serial Wire

Table 6-48 Serial Wire Interface Timing Requirement

Parameter	symbol	condition	Min	Typ.	Max	Unit
DBG_SWCLK clock period	tSWCK	—	100	—	—	ns
DEBUG input data setup time	tDBS	—	20	—	—	ns
DEBUG input data hold time	tDBH	—	15	—	—	ns
DEBUG output data delay time	tDBD	{CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	4	—	50	ns

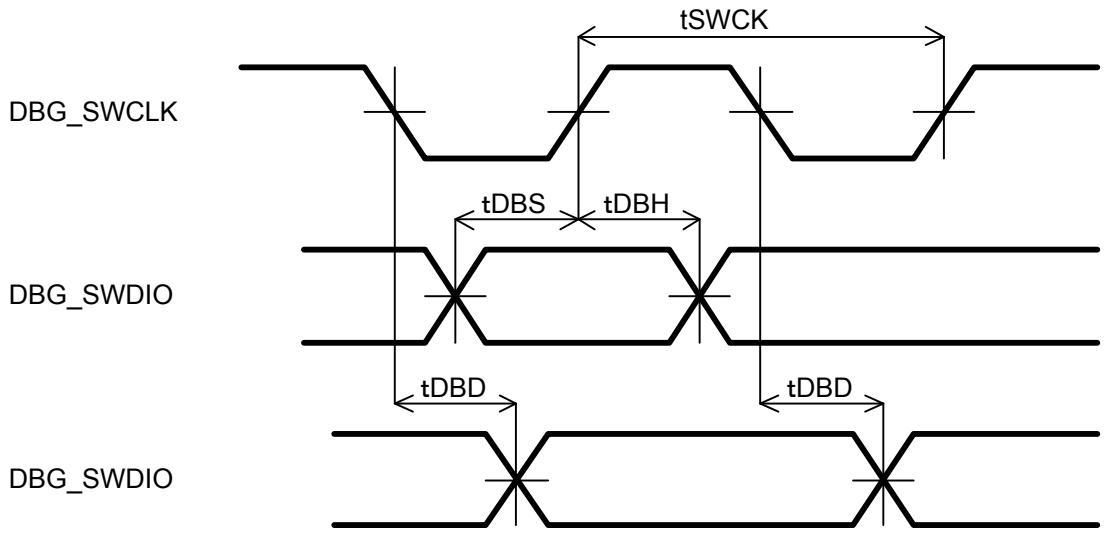


Figure 6-14 Serial Wire Interface Timing

- Trace

Table 6-49 Trace Interface Timing Requirement

Parameter	symbol	condition	Min	Typ.	Max	Unit
DBG_TRACECLK clock period	tTCLK	Voltage Mode Overdrive {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11 Voltage Mode A {CTL2,CTL1}: 0b01, 0b10, 0b11	83.3	—	—	ns
		Voltage Mode A {CTL2,CTL1}: 0b00 Voltage Mode B {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11	166.7	—	—	ns
TRACE data setup time of clock fall edge	tSETUPF	{CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	3	—	—	ns
TRACE data hold time of clock fall edge	tHOLDF	{CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	2	—	—	ns
TRACE data setup time of clock rise edge	tSETUPR	{CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	3	—	—	ns
TRACE data hold time of clock rise edge	tHOLDR	{CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	2	—	—	ns

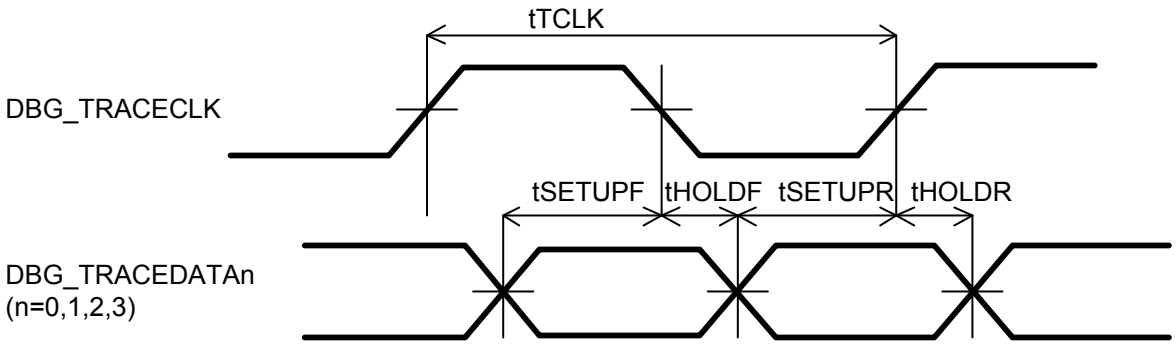


Figure 6-15 Trace Interface Timing

6.7.6. I2S Interface

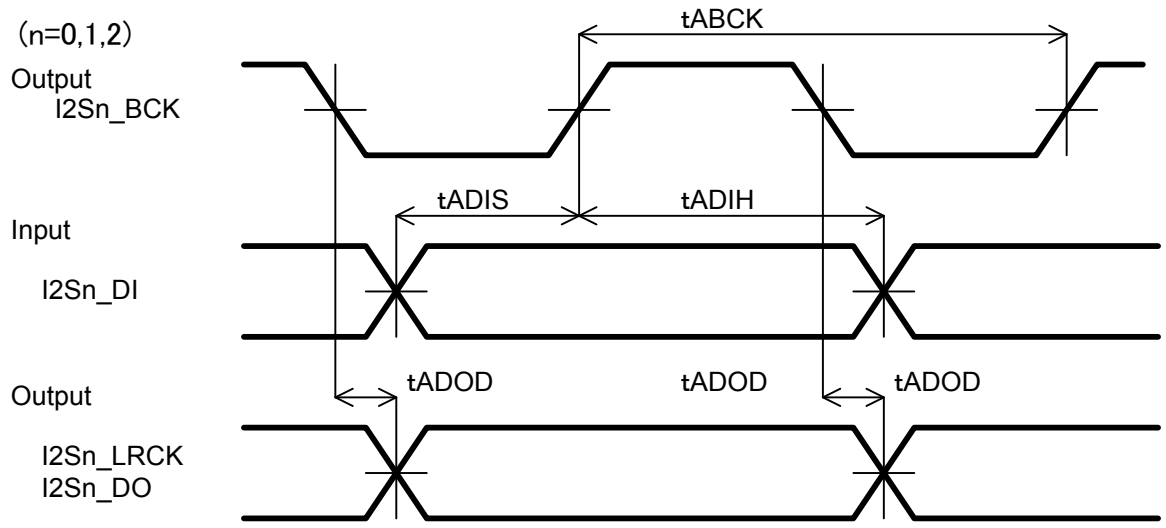
- Master Mode

Table 6-50 I2S Interface Timing Requirement (Master Mode)

Parameter	symbol	condition	Min	Typ.	Max	Unit
I2S Output Clock Period	tABCK	—	325 (*1)	—	—	ns
I2S Input Data Setup Time	tADIS	—	80	—	—	ns
I2S Input Data Hold Time	tADIH	—	80	—	—	ns
I2S Output Delay Time	tADOD	—	—	—	80	ns

*1: Max 3.072 MHz

Output Bit Clock (1)：Neg Edge Data Output、Pos Edge Input Data Sampleing



Output Bit Clock (2)：Pos Edge Data Output、Neg Edge Input Data Sampling

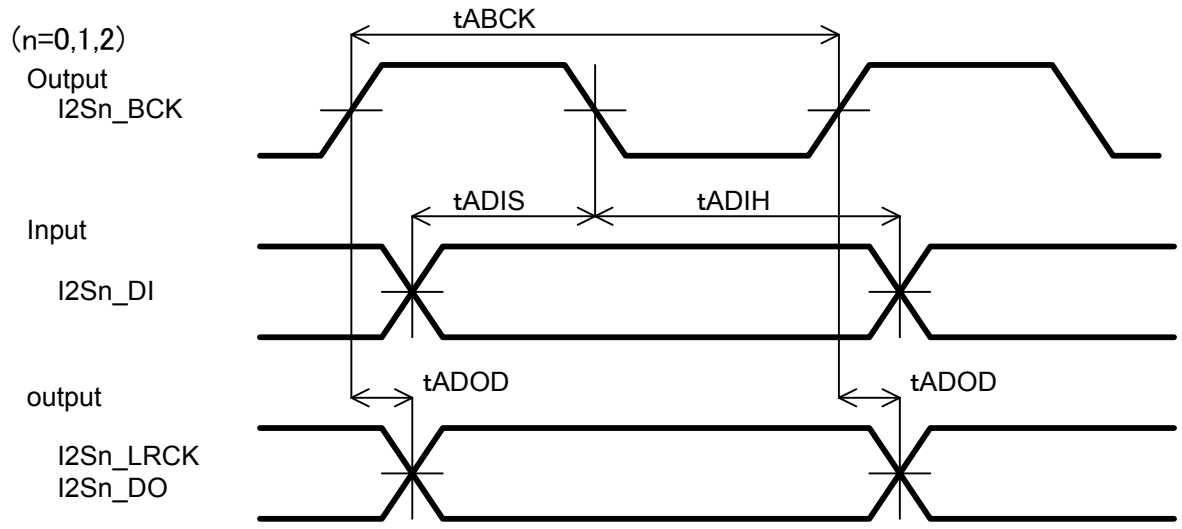


Figure 6-16 I2S Interface Timing (Master Mode)

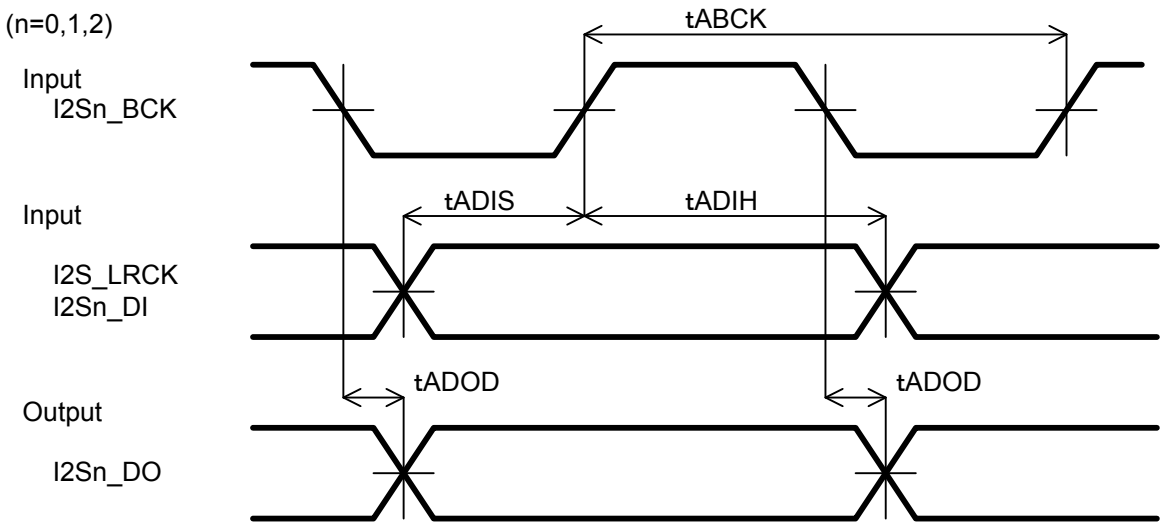
- Slave Mode

Table 6-51 I2S Interface Timing Requirement (Slave Mode)

Parameter	symbol	condition	Min	Typ.	Max	Unit
I2S Input Clock Period	tABCK	—	325 (*1)	—	—	ns
I2S Input Data Setup Time	tADIS	—	80	—	—	ns
I2S Input Data Hold Time	tADIH	—	80	—	—	ns
I2S Output Delay Time	tADOD	—	—	—	80	ns

*1: Max 3.072 MHz

Input Bit Clock (1): Neg Edge Data Output、Pos Edge Input Data Sampling



Input Bit Clock (2): Pos Edge Data Output, Neg Edge Input Data Sampling

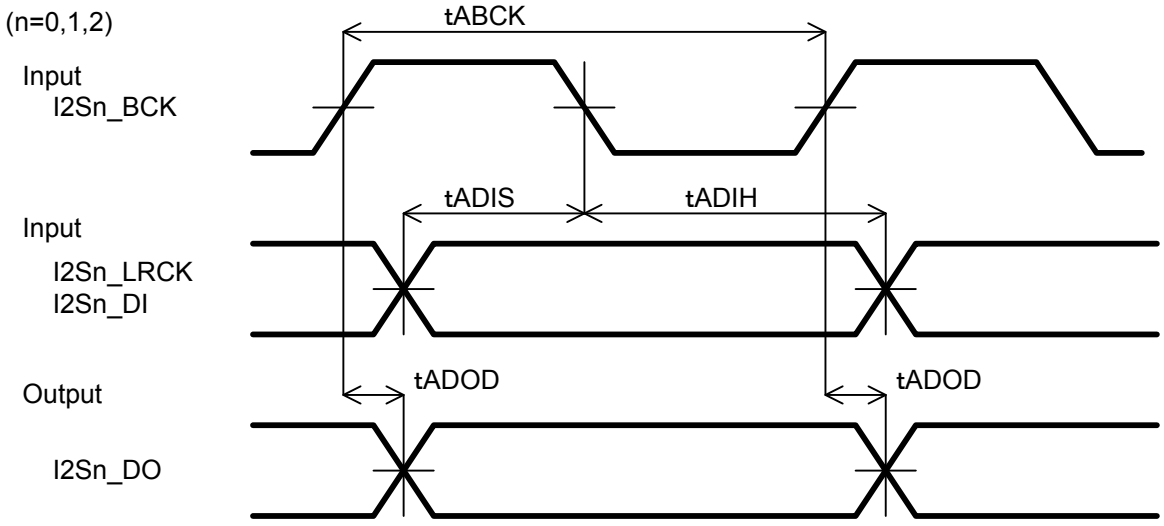


Figure 6-17 I2S Interface Timing (Slave Mode)

6.7.7. PDM Interface

Table 6-52 PDM Interface Timing Requirement

Parameter	symbol	condition	Min	Typ.	Max	Unit
PDM Output Clock Period	tPDMCK	—	163 (*1)	—	—	ns
PDM Input Data Setup Time	tPDMS	—	50	—	—	ns
PDM Input Data Hold Time	tPDMH	—	0	—	—	ns

*1: Max 6.144 MHz

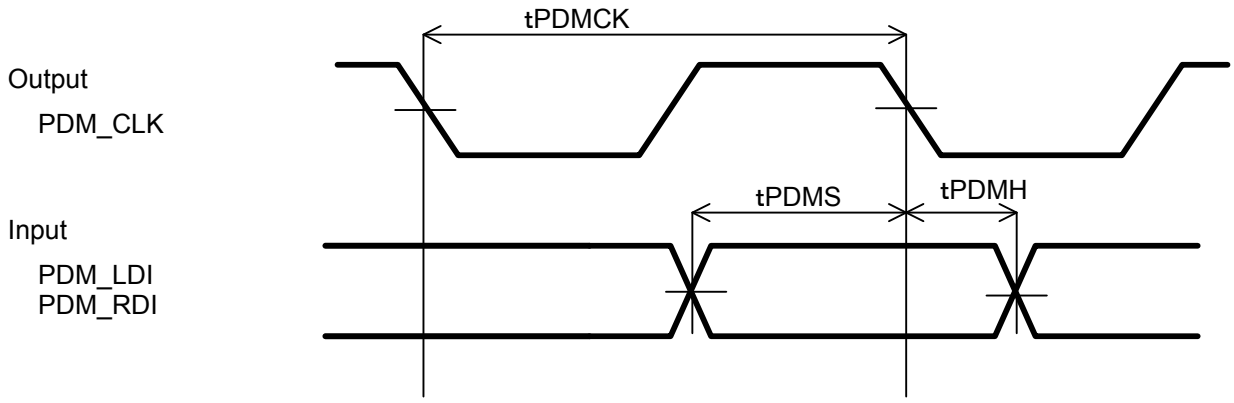


Figure 6-18 PDM Interface Timing

6.7.8. EBIF Interface

6.7.8.1. Asynchronous Mode

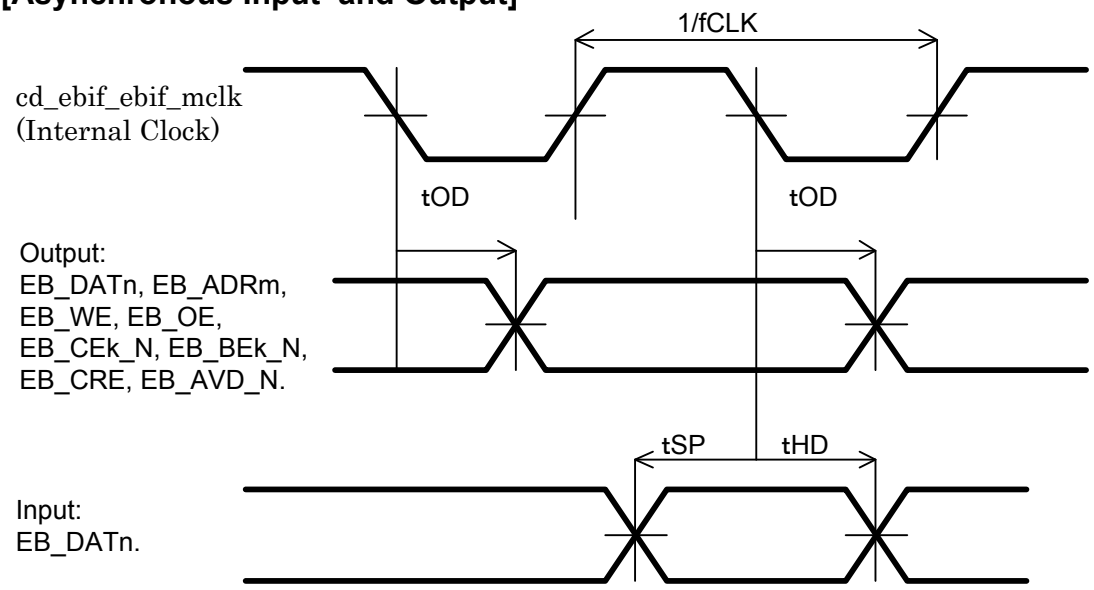
Table 6-53 EBIF Timing Requirements in Asynchronous Mode (fast frequency)

Parameter	symbol	condition	Min	Typ.	Max	Unit
Internal clock frequency	fCLK	—	48	—	60	MHz
Input data setup time	tSP	Input Slew: Max 2.0 ns.	20	—	—	ns
Input data hold time	tHD	Input Slew: Max 2.0 ns.	0.5	—	—	ns
Output data delay time	tOD	CL: Max 25 pF, min 2 pF. {CTL2,CTRL1}: 0b01, 0b10, 0b11.	0	—	20	ns

Table 6-54 EBIF Timing Requirements in Asynchronous Mode (slow frequency)

Parameter	symbol	condition	Min	Typ.	Max	Unit
Internal clock frequency	fCLK	—	3	—	30	MHz
Input data setup time	tSP	Input Slew: Max 2.0 ns.	20	—	—	ns
Input data hold time	tHD	Input Slew: Max 2.0 ns.	0.5	—	—	ns
Output data delay time	tOD	CL: Max 25 pF, min 2 pF. {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	0	—	20	ns

[Asynchronous Input and Output]



(n=0, 1, ⋯, 15. m=16, 17, ⋯, 21. k=0, 1.)

Figure 6-19 EBIF Timing Diagram in Asynchronous Mode

6.7.8.2. Synchronous Mode

Table 6-55 EBIF Timing Requirements in Synchronous Mode (fast frequency)

Parameter	symbol	condition	Min	Typ.	Max	Unit
Output clock frequency	fCLKO	CL: Max 25 pF, min 2 pF. {CTL2,CTL1}: 0b01, 0b10, 0b11.	48	—	60	MHz
Input clock frequency	fCLKI	Input Slew: Max 2.0 ns.	48	—	60	MHz
Clock skew from EB_CLKO to EB_CLKI (*1)	tCKSKW	CL: Max 25 pF, min 2 pF. {CTL2,CTL1}: 0b01, 0b10, 0b11. Input Slew: Max 2.0 ns.	0	—	1	ns
Input data setup time	tSP	Input Slew: Max 2.0 ns.	OD 6.2 MA 10.3 MB 10.3	—	—	ns
Input data hold time	tHD	Input Slew: Max 2.0 ns.	1.5	—	—	ns
Output data delay time	tOD	CL: Max 25 pF, min 2 pF. {CTL2,CTL1}: 0b01, 0b10, 0b11.	OD -5.83 MA -7.9 MB -7.9	—	OD 4.83 MA 6.9 MB 6.9	ns

*1: EB_CLKI is expected to be connected with EB_CLKO which is routed to the target device and then routed back to EB_CLKI. Refer to the document of the EBIF.

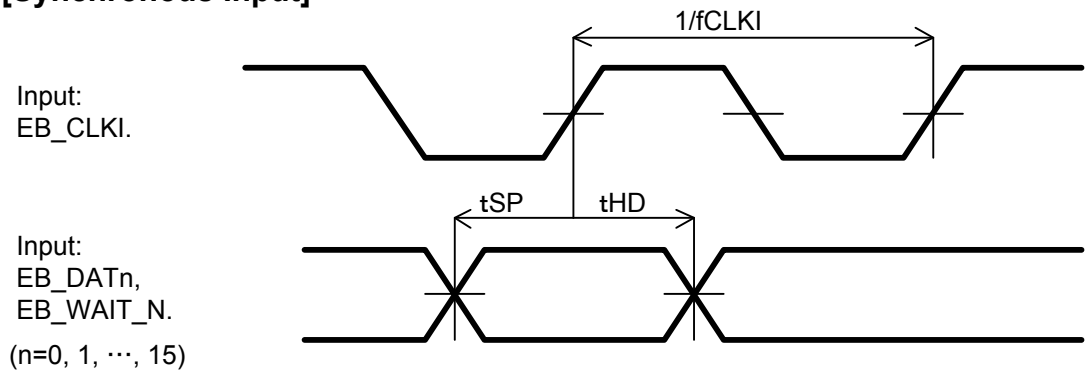
Table 6-56 EBIF Timing Requirements in Synchronous Mode (slow frequency)

Parameter	symbol	condition	Min	Typ.	Max	Unit
Output clock frequency	fCLKO	CL: Max 25 pF, min 2 pF. {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	3	—	30	MHz
Input clock frequency (*2)	fCLKI	Input Slew: Max 2.0 ns.	3	—	30	MHz
Clock skew from EB_CLKO to EB_CLKI (*1), (*2)	tCKSKW	CL: Max 25 pF, min 2 pF. {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11. Input Slew: Max. 2.0 ns.	0	—	2	ns
Input data setup time	tSP	Input Slew: Max 2.0 ns.	OD 22.84 MA 31.17 MB 31.17	—	—	ns
Input data hold time	tHD	Input Slew: Max 2.0 ns.	1.5	—	—	ns
Output data delay time	tOD	CL: Max 25 pF, min 2 pF. {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	OD -14.17 MA -18.33 MB -18.33	—	OD 13.17 MA 17.34 MB 17.34	ns

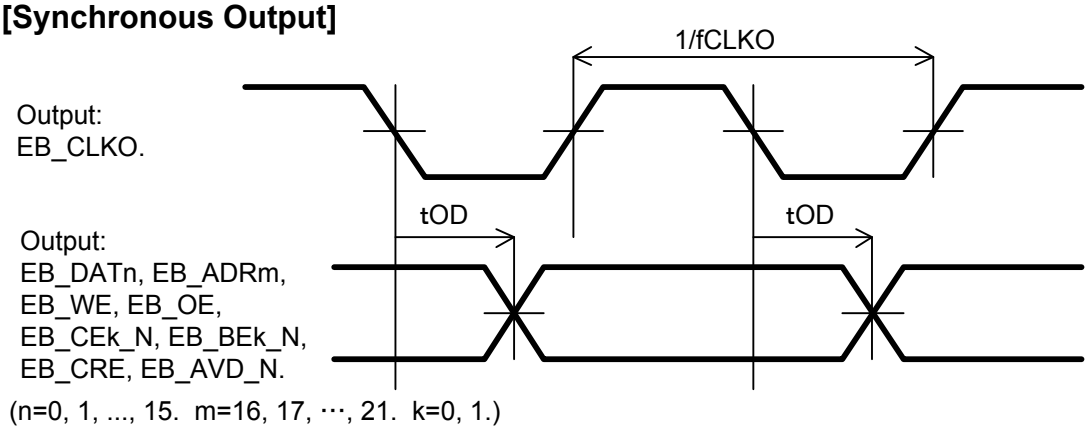
*1: EB_CLKI is expected to be connected with EB_CLKO which is routed to the target device and then routed back to EB_CLKI. Refer to the document of the EBIF.

*2: In the slow frequency case, the internal clock mode is available as a capture clock for inputs. This requirement is only needed in the case of using EB_CLKI.

[Synchronous Input]



[Synchronous Output]



[Clock Skew]

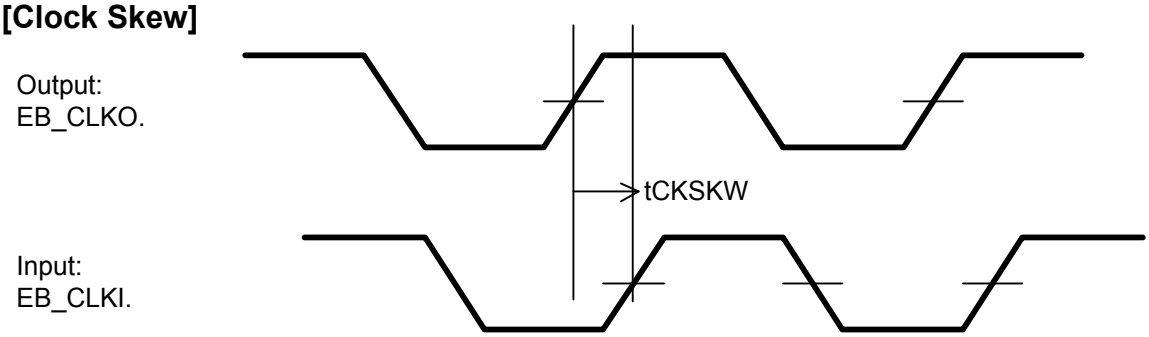


Figure 6-20 EBIF Timing Diagram in Synchronous Mode

6.7.8.3. Common Characteristics Asynchronous and Synchronous Mode

Table 6-57 EBIF Timing Requirements on Data Skew

Parameter	symbol	condition	Min	Typ.	Max	Unit
Data skew (*1), (*2)	tDTSKW	CL: Max 25 pF, min 2 pF. {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	0.2	—	—	ns

*1: From EB_DATn, EB_ADRm and EB_AVD_N to EB_WE_N (n = 0, 1, … , 15. m = 16, 17, … , 21.).

*2: This feature is valid if these data are changed at the same time.

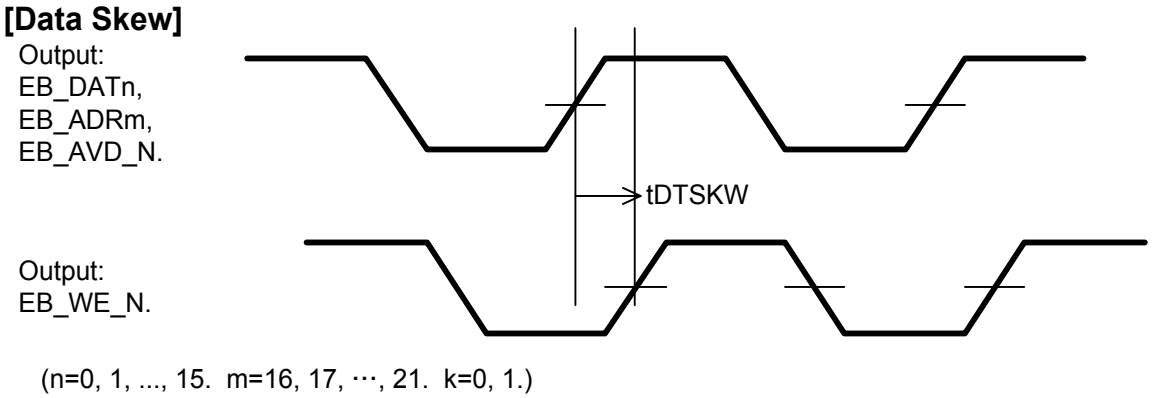


Figure 6-21 EBIF Timing Diagram on Data Skew

6.7.9. DBIBC Interface

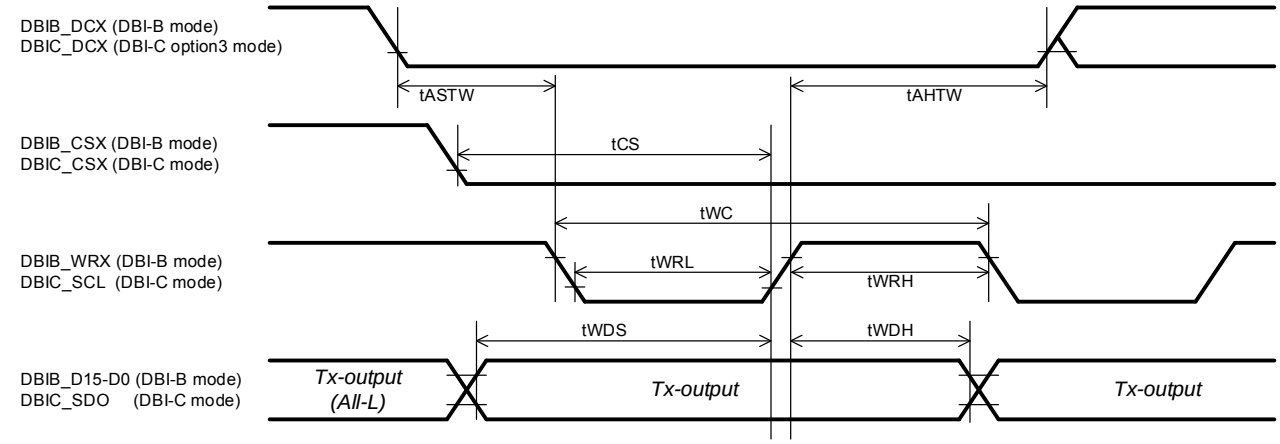
Table 6-58 DBIBC Interface Timing Requirement

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Address setup time (Write)	tASTW	—	tCK x cp - 7.0	—	—	ns
Address setup time (Read)	tASTR	—	tCK x read - 7.0	—	—	ns
Address hold time (Write)	tAHTW	—	tCK x divw2 - 6.0	—	—	ns
Address hold time (Read)	tAHTR	—	tCK x divr2 - 6.0	—	—	ns
Chip Select setup time	tCS	—	tCK x (csx + divw1) - 7.0	—	—	ns
Write cycle	tWC	—	—	tCK × divw	—	ns
Write Control pulse H duration	tWRH	—	tCK x divw2 - 1.1	tCK × divw2	tCK × divw2 + 1.5	ns
Write Control pulse L duration	tWRL	—	tCK x divw1 - 1.5	tCK × divw1	tCK × divw1 + 1.1	ns
Read cycle	tRC	—	—	tCK × divr	—	ns
Read Control pulse H duration	tRDH	—	tCK x divr2 - 0.3	tCK × divr2	tCK × divr2 + 2.4	ns
Read Control pulse L duration	tRDL	—	tCK x divr1 - 2.4	tCK × divr1	tCK × divr1 + 0.3	ns
Write data setup time	tWDS	—	tCK x divw1 - 7.0	—	—	ns
Write data hold time	tWDH	—	tCK x divw2 - 6.0	—	—	ns
Read data setup time	tRST	—	30.0	—	—	ns
Read data hold time	tRHT	—	0	—	—	ns
Write output disable time	tWOD	—	tCK x divw2 - 10.0	—	tCK × divw2 + 7.0	ns
Data input hold time	tDIH	—	tCK x divr2 - 10.0	—	—	ns

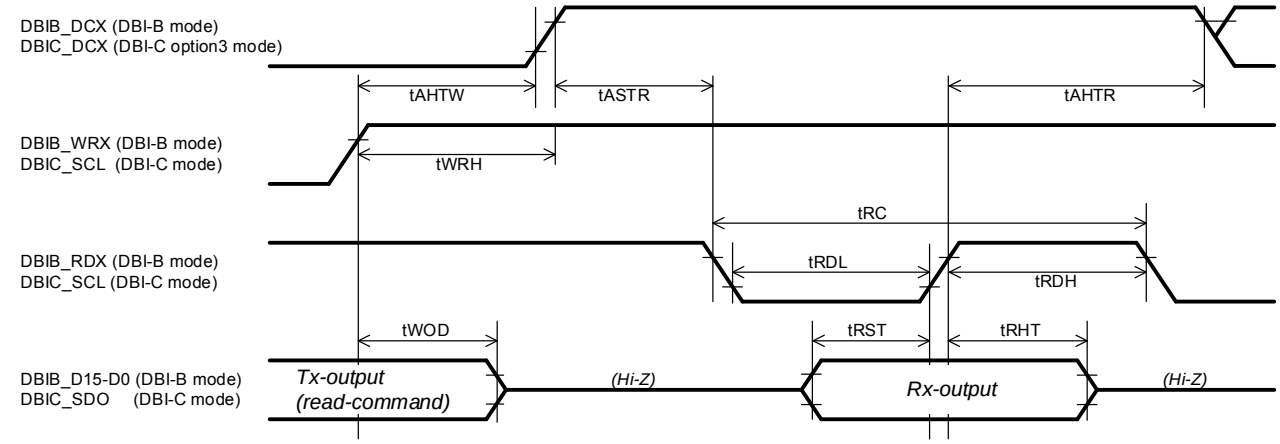
tCK: Output-Clk cycle (ns)
Voltage Mode A: 10.4 ns, Voltage Mode B: 20.8 ns, Voltage OverDrive: 8.3 ns
div: (Write)divw, (Read)divr
divw: *DBIBC.[DBIBC_OUT_CYCLE].outdivw*
divr: *DBIBC.[DBIBC_OUT_CYCLE].outdivr*
cp: *DBIBC.[DBIBC_OUT_CYCLE].ac_cmd_param*
read: *DBIBC.[DBIBC_OUT_CYCLE].ac_read_start*
csx: *DBIBC.[DBIBC_OUT_CYCLE].ac_csx_cp*
divw1: divw / 2
divw2: divw / 2 + divw%2
divr1: divr / 2
divr2: divr / 2 + divr%2

Please set the same value of the drive-strength to the using pins.

[Write]



[Write-Read]



[Read-Write]

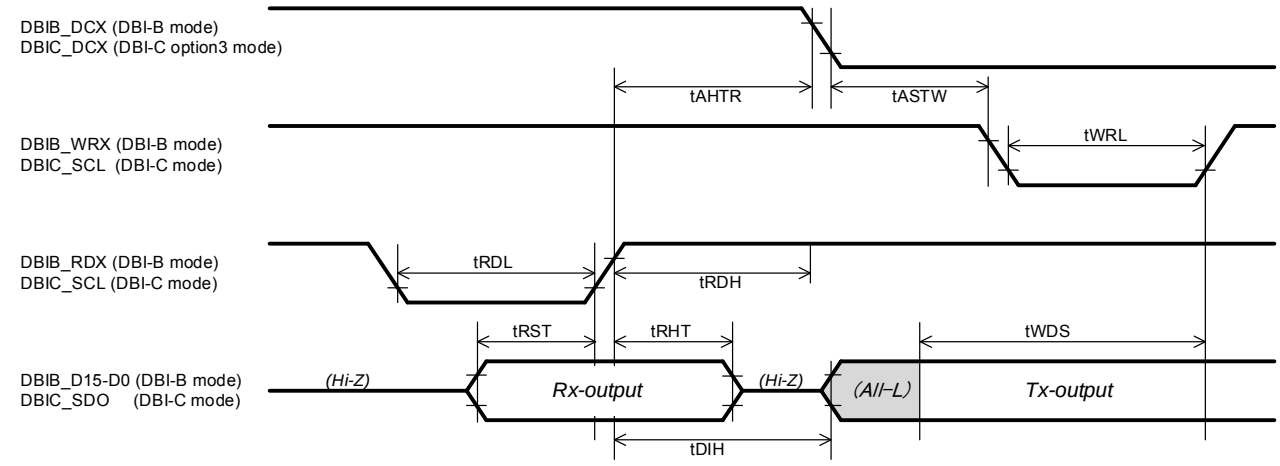


Figure 6-22 DBIBC Interface Timing

6.7.10. SPIFC Interface

Table 6-59 SPIFC Timing Requirements (fast frequency)

Parameter	symbol	condition	Min	Typ.	Max	Unit
Output clock frequency	fCLK	CL: Max 26 pF, min 1pF. {CTL2,CTL1}: OD 0b11, MA 0b01, 0b10, 0b11, MB 0b10, 0b11.	48	—	60	MHz
Input data setup time	tSP	Input Slew: Max 2.0 ns.	OD 7.17 MA 11.34 MB 11.34	—	—	ns
Input data hold time	tHD	Input Slew: Max 2.0 ns.	OD 1.0 MA 0.0 MB 0.0	—	—	ns
Output data delay time	tDTOD	CL: Max 26 pF, min 1pF. {CTL2,CTL1}: OD 0b11, MA 0b01, 0b10, 0b11, MB 0b10, 0b11.	OD -2.84 MA -4.92 MB -4.92	—	OD 2.84 MA 4.92 MB 4.92	ns
Output chip-select delay time	tCSOD	CL: Max 8 pF, min 1pF. {CTL2,CTL1}: OD 0b11, MA 0b01, 0b10, 0b11, MB 0b10, 0b11.	OD -2.84 MA -4.92 MB -4.92	—	OD 2.84 MA 4.92 MB 4.92	ns

Table 6-60 SPIFC Timing Requirements (slow frequency)

Parameter	symbol	condition	Min	Typ.	Max	Unit
Output clock frequency	fCLK	CL: Max 26 pF, min 1pF. {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	3	—	30	MHz
Input data setup time	tSP	Input Slew: Max 2.0 ns.	OD 23.84 MA 32.17 MB 32.17	—	—	ns
Input data hold time	tHD	Input Slew: Max 2.0 ns.	OD 0.0 MA 0.0 MB 0.0	—	—	ns
Output data delay time	tDTOD	CL: Max 26 pF, min 1pF. {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	OD -11.17 MA -15.34 MB -15.34	—	OD 11.17 MA 15.34 MB 15.34	ns
Output chip-select delay time	tCSOD	CL: Max 8 pF, min 1pF. {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	OD -11.17 MA -15.34 MB -15.34	—	OD 11.17 MA 15.34 MB 15.34	ns

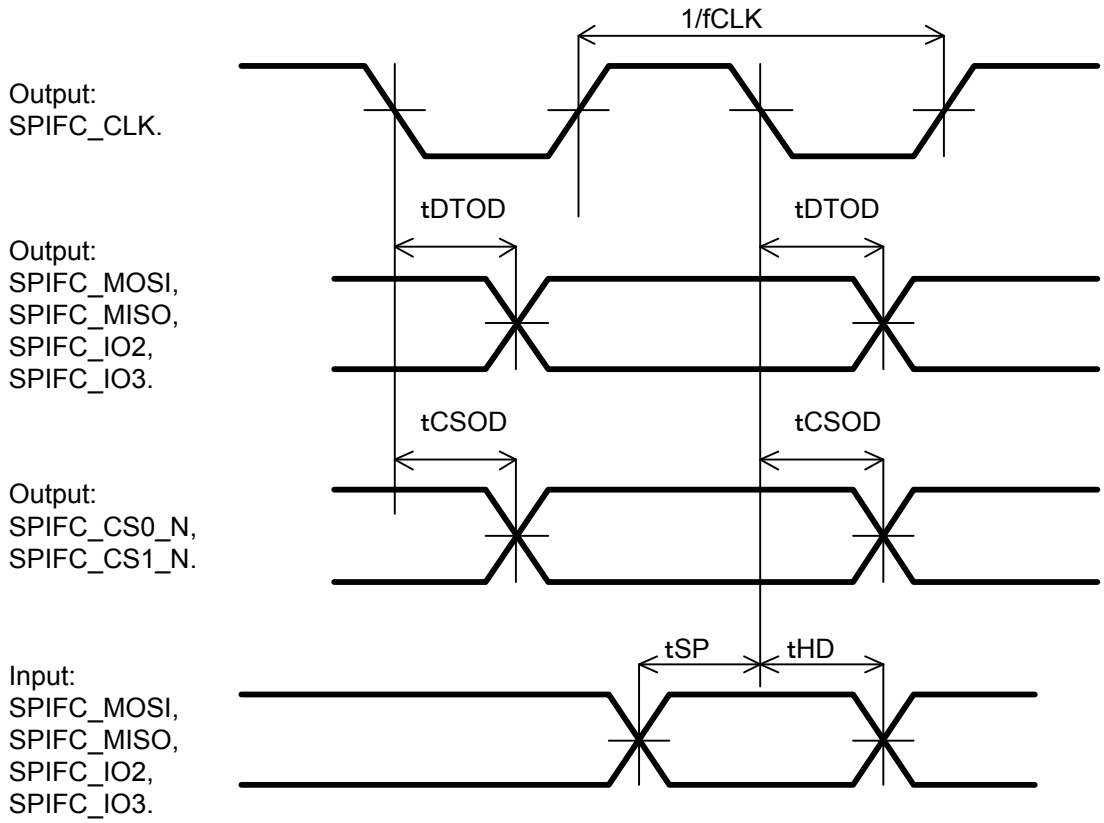


Figure 6-23 SPIFC Timing Diagram

6.7.11. SPINOFC Interface

Table 6-61 SPINOFC Timing Requirements (fast frequency)

Parameter	symbol	condition	Min	Typ.	Max	Unit
Output clock frequency	fCLK	CL: Max 26 pF, min 1pF. {CTL2,CTL1}: OD 0b11, MA 0b01, 0b10, 0b11, MB 0b10, 0b11.	48	—	60	MHz
Input data setup time	tSP	Input Slew: Max 2.0 ns.	OD 7.17 MA 11.34 MB 11.34	—	—	ns
Input data hold time	tHD	Input Slew: Max 2.0 ns.	OD 1.0 MA 0.0 MB 0.0	—	—	ns
Output data delay time	tDTOD	CL: Max 26 pF, min 1pF. {CTL2,CTL1}: OD 0b11, MA 0b01, 0b10, 0b11, MB 0b10, 0b11.	OD -2.84 MA -4.92 MB -4.92	—	OD 2.84 MA 4.92 MB 4.92	ns
Output chip-select delay time	tCSOD	CL: Max 8 pF, min 1pF. {CTL2,CTL1}: OD 0b11, MA 0b01, 0b10, 0b11, MB 0b10, 0b11.	OD -2.84 MA -4.92 MB -4.92	—	OD 2.84 MA 4.92 MB 4.92	ns

Table 6-62 SPINOFC Timing Requirements (slow frequency)

Parameter	symbol	condition	Min	Typ.	Max	Unit
Output clock frequency	fCLK	CL: Max 26 pF, min 1pF. {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	3	—	30	MHz
Input data setup time	tSP	Input Slew: Max 2.0 ns.	OD 23.84 MA 32.17 MB 32.17	—	—	ns
Input data hold time	tHD	Input Slew: Max 2.0 ns.	OD 0.0 MA 0.0 MB 0.0	—	—	ns
Output data delay time	tDTOD	CL: Max 26 pF, min 1pF. {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	OD -11.17 MA -15.34 MB -15.34	—	OD 11.17 MA 15.34 MB 15.34	ns
Output chip-select delay time	tCSOD	CL: Max 8 pF, min 1pF. {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	OD -11.17 MA -15.34 MB -15.34	—	OD 11.17 MA 15.34 MB 15.34	ns

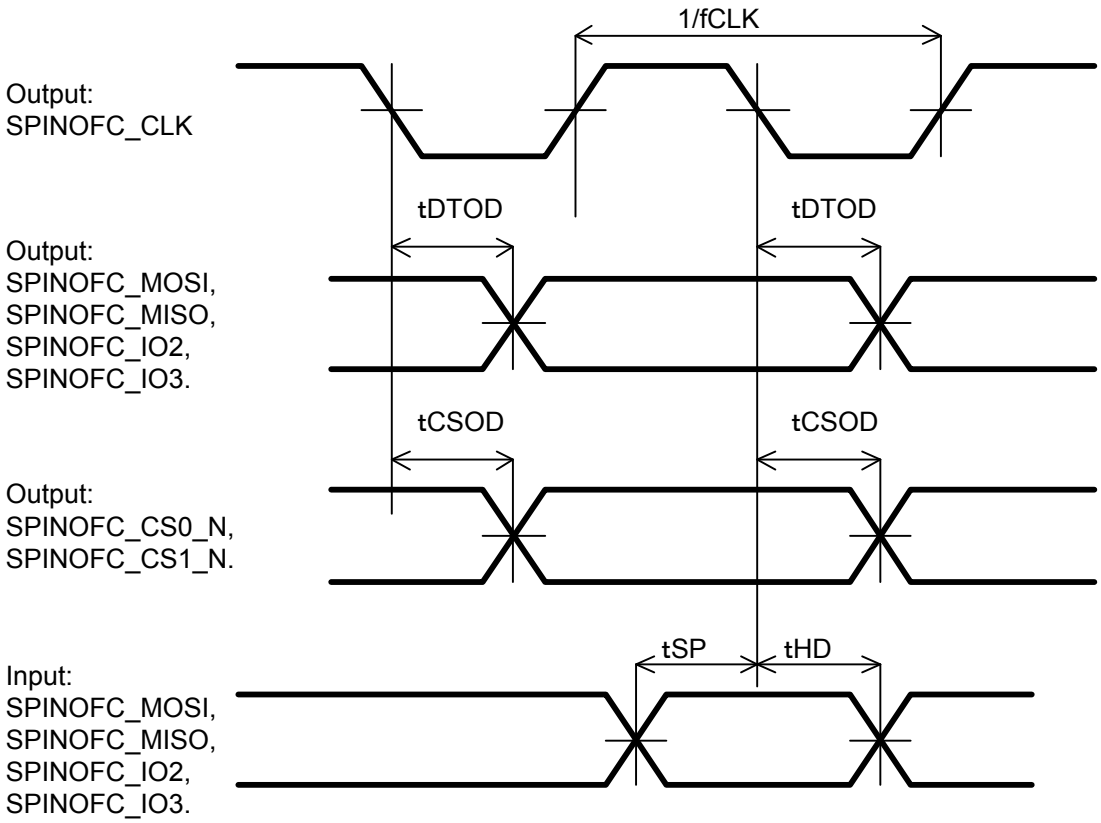


Figure 6-24 SPINOFC Timing Diagram

6.7.12. eMMC/SD Card/SDIO Interface

- Backward Compatibility (eMMC)/Default Speed (SD Card, SDIO)

Table 6-63 eMMC Interface Timing Requirements in Backward Compatibility Mode

Parameter	symbol	condition	Min	Typ.	Max	Unit
Clock frequency	fSDCK	Internal loopback clock mode {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	—	—	16	MHz
		External loopback clock mode (use EMn_CLKB pin) {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	—	—	24	MHz
CMD/DATA output delay time	tSDD	CL < 40pF {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	0	—	11	ns
CMD/DATA setup time	tSDS	—	5.5	—	—	ns
CMD/DATA hold time	tSDH	—	7.8	—	—	ns

Table 6-64 SD Card / SDIO Interface Timing Requirements in Default Speed Mode

Parameter	symbol	condition	Min	Typ.	Max	Unit
Clock frequency	fSDCK	Internal loopback clock mode {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	—	—	16	MHz
		External loopback clock mode (use EMn_CLKB pin) {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	—	—	24	MHz
CMD/DATA output delay time	tSDD	CL < 40pF {CTL2,CTL1}: 0b00, 0b01, 0b10, 0b11.	0	—	11	ns
CMD/DATA setup time	tSDS	—	5.5	—	—	ns
CMD/DATA hold time	tSDH	—	7.8	—	—	ns

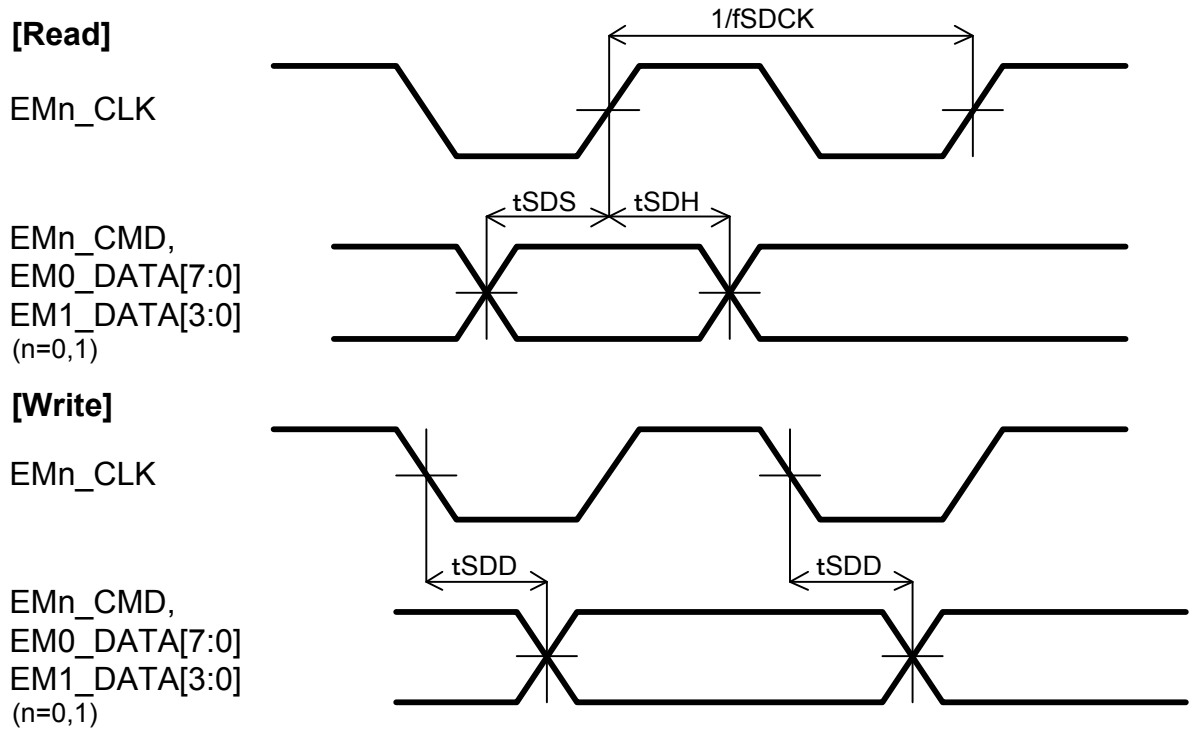


Figure 6-25 eMMC/SD Card/SDIO Interface Timing in Backward Compatibility (eMMC)/Default Speed (SD Card, SDIO) Mode

- High Speed SDR (eMMC)/High Speed (SD Card, SDIO)

Table 6-65 eMMC Interface Timing Requirements in High Speed SDR Mode

Parameter	symbol	condition	Min	Typ.	Max	Unit
Clock frequency	fSDCK	Internal loopback clock mode {CTL2,CTL1}: 0b01, 0b10, 0b11.	—	—	24	MHz
		Internal loopback clock mode {CTL2,CTL1}: 0b11.	—	—	32	MHz
		External loopback clock mode (use EMn_CLKB pin), {CTL2,CTL1}: 0b01, 0b10, 0b11.	—	—	48	MHz
CMD/DATA output delay time	tSDD	CL < 40pF {CTL2,CTL1}: 0b01, 0b10, 0b11.	3.5	—	13.5	ns
CMD/DATA setup time	tSDS	—	5.5	—	—	ns
CMD/DATA hold time	tSDH	—	2.0	—	—	ns

Table 6-66 SD Card / SDIO Interface Timing Requirements in High Speed Mode

Parameter	symbol	condition	Min	Typ.	Max	Unit
Clock frequency	fSDCK	Internal loopback clock mode {CTL2,CTL1}: 0b01, 0b10, 0b11.	—	—	24	MHz
		Internal loopback clock mode {CTL2,CTL1}: 0b11.	—	—	32	MHz
		External loopback clock mode (use EMn_CLKB pin) {CTL2,CTL1}: 0b01, 0b10, 0b11.	—	—	48	MHz
CMD/DATA output delay time	tSDD	CL < 40pF {CTL2,CTL1}: 0b01, 0b10, 0b11.	3.5	—	13.5	ns
CMD/DATA setup time	tSDS	—	5.5	—	—	ns
CMD/DATA hold time	tSDH	—	2.0	—	—	ns

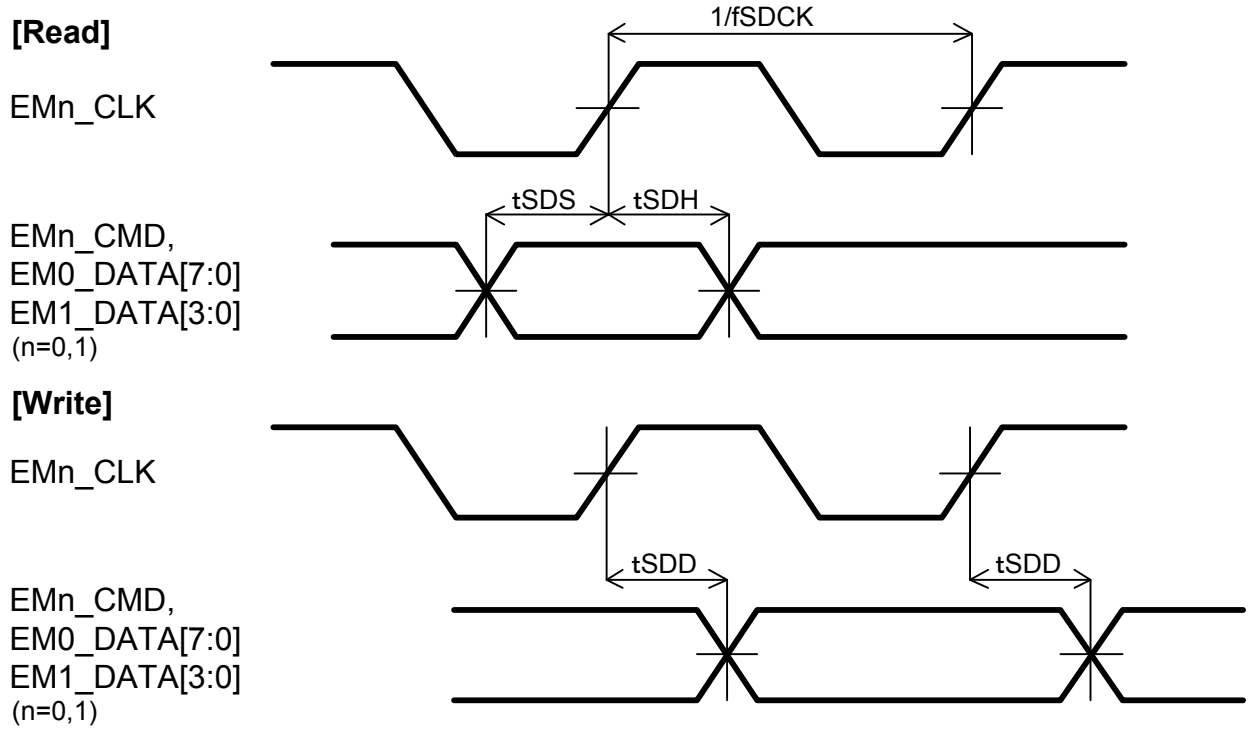


Figure 6-26 eMMC/SD Card/SDIO Interface Timing in High Speed SDR (eMMC)/High Speed (SD Card, SDIO) Mode

6.7.13. IO drive-strength table

The following table indicated IO drive strength setting (***GCONF.[IO_CFG_Pmn].CTL2***, ***GCONF.[IO_CFG_Pmn].CTL1***) for max frequency in each voltage mode.

Table 6-67 IO drive-strength

Function	Over Drive	Mode A	Mode B	Mode D
Serial wire	00,01,10,11	00,01,10,11	00,01,10,11	—
TRACE	00,01,10,11	00,01,10,11	00,01,10,11	—
DBIBC	00,01,10,11	00,01,10,11	00,01,10,11	—
EBIF (48/60MHz)	01,10,11	01,10,11	01,10,11	—
EBIF (to 30MHz)	00,01,10,11	00,01,10,11	00,01,10,11	—
EMMC (HS)	01,10,11	01,10,11	01,10,11	—
EMMC (DS)	00,01,10,11	00,01,10,11	00,01,10,11	—
EMMC (HS, Internal loopback clock mode)	01,10,11	01,10,11	01,10,11	—
EMMC (DS, Internal loopback clock mode)	00,01,10,11	00,01,10,11	00,01,10,11	—
I2C	01,10,11	01,10,11	01,10,11	01,10,11
I2S	00,01,10,11	00,01,10,11	00,01,10,11	—
SPINOFC (48/60MHz)	11	01,10,11	10,11	—
SPINOFC (to 30MHz)	00,01,10,11	00,01,10,11	00,01,10,11	—
SPIFC (48/60MHz)	11	01,10,11	10,11	—
SPIFC (to 30MHz)	00,01,10,11	00,01,10,11	00,01,10,11	—
SPIM	01,10,11	01,10,11	01,10,11	01,10,11
UART	00,01,10,11	00,01,10,11	00,01,10,11	00,01,10,11

7. Package Information

Package Name: P-UFBGA210-0808-0.40-001
Size: 8.0 mm (typ.) × 8.0 mm (typ.)
Height: 0.6 mm (max)
Ball Pitch: 0.4 mm
Weight: 75mg (Typ.)

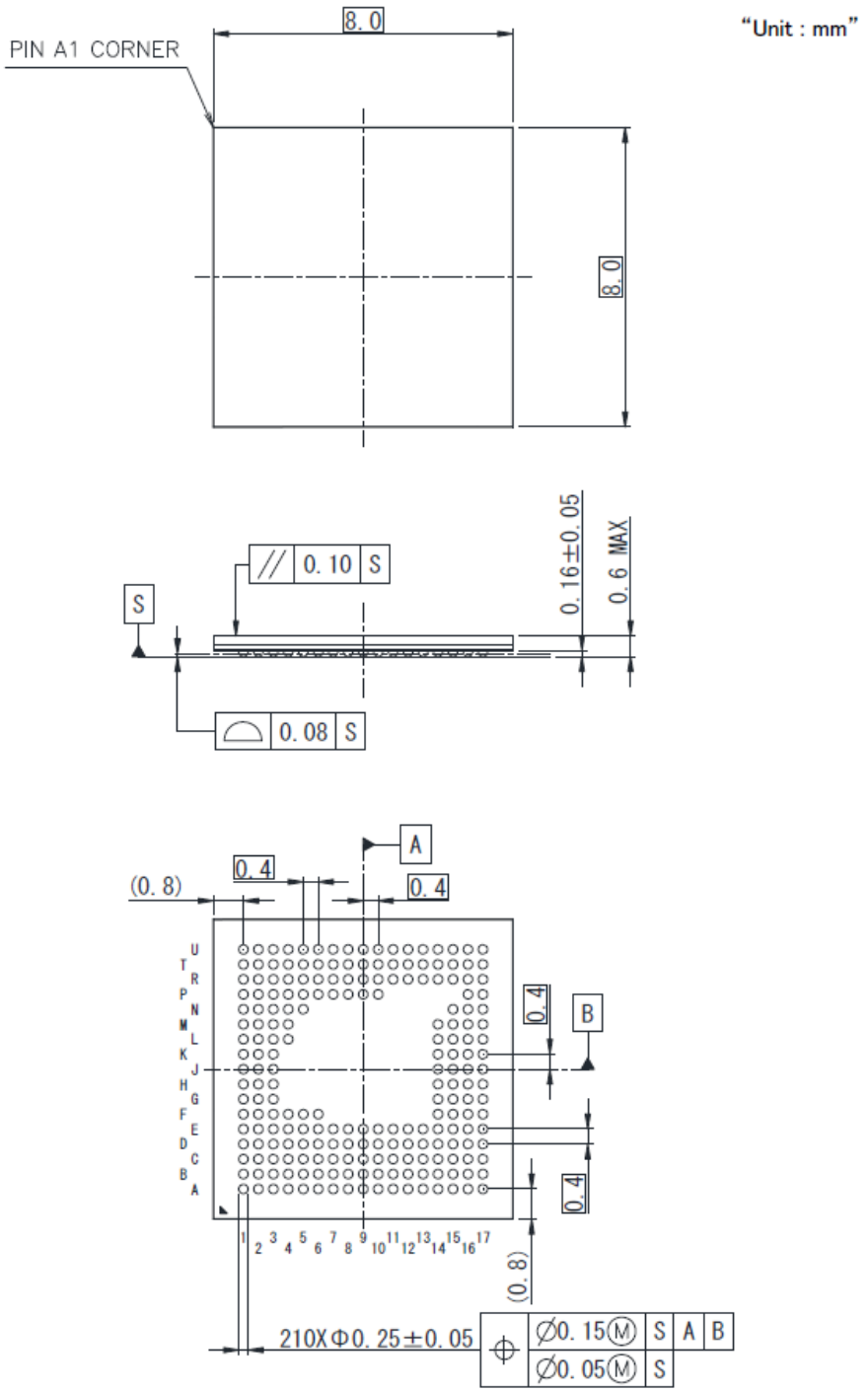


Figure 7-1 Package Drawing

Note: Figure 7-1 are for explanation. Please contact your TOSHIBA sales representative for the dimensions that are not written on the figures.

8. Revision History

Table 8-1 Revision History

Revision	Date	Description
0.0	2015-04-07	Created tentative version.
0.1	2015-07-24	Added "Section 3.block diagram." Added section 6 and 7. Update other parts with latest spec Newly released
0.2	2015-08-31	Revised pin description. Other minor revicese
0.3	2015-12-02	Added "Section 6.1. Absolute Maximum Ratings," "Section 6.4. DC Characteristics," "Section 6.5. Clock Source Characteristics," "Section 6.6. Analog Characteristics" and "Section 6.7. AC Characteristics" Figure 5.1 Pin Alignment: Corrected D14 Pin Name
0.4	2016-03-02	Added 32 kHz oscillator in Section 2.3, 4.2.1, 6.5.2.2 and Table 5.2. Added gradient feature in Section 2.6. Revised sine wave output frequency in Section 2.10. Revised BDSPAZ structure in Table 5.1. Added 5 V Tolerant of ILEDA0 and ILEDA1 pin in Table 5.2. Corrected Table 6.25 and Table 6.26. Changed input current characteristcs in Table 6.4. Changed AC specifications in Table 6.45, Table 6.46, Table 6.47, Table 6.48, Table 6.49, Table 6.51, Table 6.52, Table 6.53 and Table 6.54
1.0	2016-07-19	Added Section 6.3, 6.6.6.3, 6.6.6.4 and 6.7.13. Added IMAX in Table 6-1. Added package weight in Section 7. Revised the descriptions in Table 5-1, Table 6-1, Table 6-3, Table 6-7, Table 6-12, Table 6-13, Table 6-15, Table 6-18, Table 6-19, Table 6-20, Table 6-24, Table 6-25, Table 6-26, Table 6-27, Table 6-28, Table 6-31, Table 6-34, Table 6-53, Table 6-54, Table 6-55, Table 6-56, Table 6-57, Table 6-59, Table 6-60, Table 6-61, Table 6-62, Table 6-63, Table 6-64, Table 6-65 and Table 6-66. Revised the descriptions in Section 1, 6.6.5, 6.6.8, 6.7.3 and 6.7.5. Revised the descriptions of SPINOFC and EMMC in Section 2.4. Corrected Data Rate of ADC12 and AFEZ in Section 2.10. Corrected the D16 / D17 pin name in Figure 5-1.
1.1	2016-08-05	Changed INL MAX characteristc in Table 6-31.
1.2	2017-04-10	Revised description in section 1. Revised description in section 2.2. Revised description about UART in section 2.9. Changed Figure 3-1 Block Diagram. Changed Figure 4-1. Revised Table 4-1. Revised Lockup Time in Table 6-16.
1.3	2017-08-28	Changed header, footer and the last page. Changed corporate name and descriptions.

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