RF Vector Modulator 1.5 – 2.4 GHz

Preliminary Technical Data

AD8341

FEATURES

Cartesian Amplitude and Phase Modulation
Frequency Range 1.5 – 2.4 GHz
Continuous Magnitude Control of 0 to –30 dB
Continuous Phase Control of 0 to 360 Degrees
Output Third Order Intercept +20 dBm
Output 1 dB Compression Point +10 dBm
Single Supply Voltage 4.75 – 5.25 V
Adjustable Large Signal Modulation Bandwidth to 230 MHz
Differential I & Q Control Inputs
Fast Output Power Disable
Output Noise Floor –148 dBm/Hz

APPLICATIONS

RF PA Linearization/RF Predistortion
Amplitude and Phase Modulation
Variable Impedance-Matched Attenuator and Phase Shifter
Smart Antennas
PCS/DCS/CDMA/EDGE/W-CDMA/FWA Frequency Bands

FUNCTIONAL BLOCK DIAGRAM

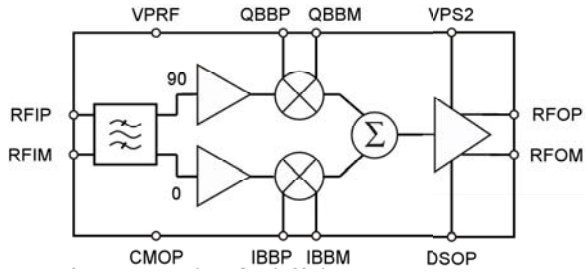

Figure 1. AD8341 Functional Block Diagram

GENERAL DESCRIPTION

The AD8341 Vector Modulator performs arbitrary amplitude and phase modulation of an RF signal. Since the RF signal path is linear, the original modulation is preserved. The AD8341can be used as a general-purpose RF modulator, a variable attenuator/phase shifter or a re-modulator. The amplitude can be controlled from a maximum of 0 dB to less than –30 dB and the phase can be shifted continuously over the entire 360 degree range. For 0 dB gain, the AD8341 delivers a P1dB of 10 dBm, an OIP3 of 20 dBm and an output noise floor of –148 dBm/Hz, independent of phase. It can operate over a frequency range from 1.5 to 2.4GHz with gain and phase flatness less than 0.2 dB and 0.5 degree.

The base-band inputs in Cartesian I and Q format control the amplitude and phase modulation imposed on the RF input signal. Both I and Q inputs are DC-coupled with a +/-500 mV differential full-scale range. The maximum modulation bandwidth is 200 MHz which can be reduced by adding external capacitors to limit the noise bandwidth on the control lines.

Both the RF inputs and outputs can be used differentially or single-ended and must be AC-coupled. The RF input and output impedances are nominally 50 ohms over the operating frequency range. The DSOP pin allows the output stage to be disabled quickly in order to protect subsequent stages from over-drive. The AD8341 operates off supply voltages from 4.75 to 5.25 V while consuming 130 mA.

The AD8341 is fabricated on Analog Devices' proprietary, high performance 25 GHz SOI complementary bipolar IC process. It is available in a 24-pin CSP package and operates over-a -40 to +85 °C temperature range. Evaluation boards are available.

Rev. PrL 1/23/2004

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REVISION HISTORY

Rev. Prl L: Updated supply voltage range, Features section, Applications section, Specifications section

AD8341—SPECIFICATIONS

Table 1. V_S = 5 V, T_A = 25°C, Z_O = 50 Ω, f = 1900 MHz, single-ended source drive to RFIP through ~2 nH series inductor, RFIM ac-coupled through ~2 nH series inductor to common, differential to single-ended converstion at output using 1:1 balun.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		1.5		2.4	GHz
Maximum Gain	Maximum gain set-point for all phase set-points		0		dB
Minimum Gain	$V_{BBI} = V_{BBQ}$ = 0V		-30		dB
Gain Control Range	Relative to maximum gain		30		dB
Phase Control Range	Over 30 dB control range		360		°
Gain Conformance	Any fixed angle over gain range of 0.1 to 0.9		TBD		%
Phase Conformance	Any fixed angle over gain range of 0.1 to 0.9		TBD		°
Gain Flatness	Over any 60 MHz bandwidth		0.25		dB
Group Delay Flatness	Over any 60 MHz bandwidth		TBD		ps
RF INPUT STAGE	**RFIM, RFIP** (Pins 3 and 4)				
Input Return Loss	From **RFIP** to **CMRF**		10		dB
CARTESIAN CONTROL INTERFACE (I & Q)	**IBBP, IBBM, QBBP, QBBM** (Pins 21, 22, 9, 10)				
Gain Scaling			2		1/V
Modulation Bandwidth	250 mVpk, single-ended sinusoidal baseband input		230		MHz
Second Harmonic Distortion	250 mVpk, 20 MHz, sinusoidal baseband input		TBD		dBc
Third Harmonic Distortion	250 mVpk, 20 MHz, sinusoidal baseband input		TBD		dBc
Step Response	Output Envelope 10% - 90%		TBD		µs
	Output Envelope 90% - 10%		TBD		µs
RF OUTPUT STAGE	**RFOP, RFOM** (Pins 15, 16)				
Output Return Loss	Measured through balun		10		dB
f = 1900 MHz					
Gain	Maximum gain set-point		0		dB
Output Noise Floor	Maximum gain set-point		-148		dBm/Hz
Output IP3	f1 = 1900 MHz, f2 = 1902.5 MHz, maximum gain set-point		+20		dBm
ACPR	CDMA, single carrier, P_{out} = TBD, maximum gain		TBD		dBc
Output 1 dB Compression Point	Maximum gain		10		dBm
f = 2200 MHz					
Gain	Maximum gain set-point		0		dB
Output Noise Floor	Maximum gain set-point		-148		dBm/Hz
Output IP3	f1 = 2200 MHz, f2 = 2202.5 MHz, maximum gain set-point		+20		dBm
ACPR	WCDMA, single carrier, P_{out} = TBD, maximum gain		TBD		dBc
Output 1 dB Compression Point	Maximum gain		10		dBm
POWER SUPPLY	**VPS2** (Pins 11, 12, 20); **RFOP, RFOM** (Pins 15, 16)				
Positive Supply Voltage		4.75	5	5.25	V
Total Supply Current	Includes load current		130		mA
OUTPUT DISABLE	**DSOP** (Pin 19)				
Disable Threshold			2.5		V
Maximum Attenuation	DSOP = 5 V		40		dB

Enable Response Time	Delay following high to low transition until device meets full specifications	10	ns
Disable Response Time	Delay following low to high transition until device produces full attenuation	tbd	ns

ABSOLUTE MAXIMUM RATINGS

Table 2. AD8341 Absolute Maximum Ratings

Parameter	Rating
Supply Voltage **VPRF, VPS2**	5.5 V
Input Voltage:	
DSOP	VPS2 + tbd V
IBBP, IBBM, QBBP, QBBM	VPS 2+ tbd V
RFOP, RFOM	VPS 2+ tbd V
RF Input Power at Maximum Gain	tbd mW
Equivalent Voltage	tbd V
Internal Power Dissipation	tbd mW
θ_{JA}	tbd °C/W
Maximum Junction Temperature	tbd°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

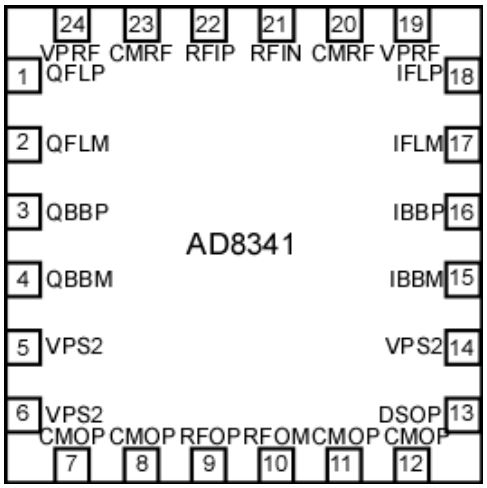

Figure 1. 24-Lead Leadframe Chip Scale Package (LFCSP)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 2	**QFLP, QFLM**	Q baseband input filter pins. Connect optional capacitor to reduce Q baseband channel lowpass corner frequency.
3, 4	**QBBP, QBBM**	Q channel differential baseband inputs.
5, 6, 14, 19, 24	**VPS2, VPRF**	Positive supply voltage. +4.75 to +5.25 V
7, 8, 11, 12, 20, 23	**CMOP, CMRF**	Device common. Connect via lowest possible impedance to external circuit common.
9, 10	**RFOP, RFOM**	Differential RF outputs. Must be AC-coupled. Differential impedance 50Ω nominal.
13	**DSOP**	Output disable. Pull high to disable output stage.
15, 16	**IBBP, IBBM**	I channel differential baseband inputs.
17, 18	**IFLP, IFLM**	I baseband input filter pins. Connect optional capacitor to reduce I baseband channel lowpass corner frequency.
21, 22	**RFIP, RFIM**	Differential RF inputs. Must be AC-coupled. Differential impedance 50Ω nominal.

GENERAL STRUCTURE

THEORY OF OPERATION

The AD8341 is a linear RF vector modulator with Cartesian base-band controls. A simplified block diagram is given in Figure 1. The RF input is first split into in-phase (I) and quadrature (Q) components. The linear variable attenuators dedicated to each branch scale their respective inputs. The attenuator outputs are then summed and buffered to the output. The RF signal path generally propagates from the left to the right while baseband controls are placed above and below.

By controlling the relative amounts of I and Q signal components that are summed, arbitrary, continuous magnitude and phase control of the input signal is possible. Figure 2 represents a vector gain transfer function of the AD8341 in polar form. The attenuation factor for the I and Q signal components are represented on the x and y-axis, respectively and their vector sum indicates the vector gain at a particular gain and phase set-point. The correspondence between these set-points and the Cartesian inputs, V_{BBI} and V_{BBQ} is given by simple trigonometric identities,

$Gain_{SP}$ =sqrt [(V_{BBI}/V_o)2 + (V_{BBQ}/V_o)2]

$Phase_{SP}$ = arctan (V_{BBQ}/V_{BBI}),

where V_o is the baseband scaling constant (500mV) and $Gain_{SP}$ and $Phase_{SP}$ are the desired gain and phase set-points. In general, both V_{BBI} and V_{BBQ} are needed in concert to modulate the gain and the phase.

Pure amplitude modulation is represented by radial movement of the gain vector tip at a fixed angle while pure phase modulation by rotation of the tip around the circle at a fixed radius. Unlike traditional I-Q modulators, the AD8341 is designed to have a linear RF signal path from input to output. Traditional I-Q modulators provide a limited LO carrier path through which any amplitude information is removed.

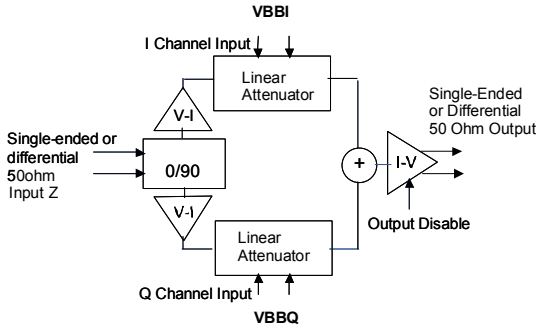

Figure 1. Simplified architecture of the AD8341

RF Quadrature Generator

The RF input is directly coupled to the quadrature generator, which consists of a multi-stage R16 poly-phase network tuned over the operating frequency range of 1.5 to 2.7 GHz. The recycling nature of the poly-phase network is responsible for generating two replicas of the input signal, which are in precise quadrature, i.e. 90°, to each other. Since the passive network is perfectly linear, the amplitude information is transmitted to both channels unaffected. The quadrature outputs are then separately buffered to drive the respective attenuators. The characteristic impedance of the poly-phase network is used to set the input impedance to the AD8341.

I-Q Attenuators and Baseband Amplifiers

The proprietary linear-responding attenuator structure is an active solution with differential inputs and outputs that offers excellent linearity, low noise, <0.1% conformance error and immunity from mismatches. The "gain", in linear terms, is proportional to its control voltage with a scaling factor designed to be 2/V, i.e. a full-scale gain magnitude of 1 for a +/-500mV differential input, V_{BB}, and a minimum gain magnitude, limited by RF feed-through, of <0.1 for a V_{BB} of 0V. The differential base-band inputs should be centered at about a 500mV common-mode. Single-ended drive is also possible by applying the same common-mode voltage to the unused input and swinging the other input from 0 to 1V. The combination of the baseband amplifiers and attenuators enable maximum modulation bandwidth up to 200 MHz.

Output Amplifier

The output amplifier accepts the sum of the attenuator outputs and delivers a differential output signal into the external load. The output pins must be pulled up to an external supply, preferably through RF chokes. When the 50 ohm load is taken differentially, an output P1dB and IP3 of 10 dBm and 20 dBm are achieved, respectively, at 1.9 GHz. The output can be taken in single-ended fashion, albeit at lower performance levels.

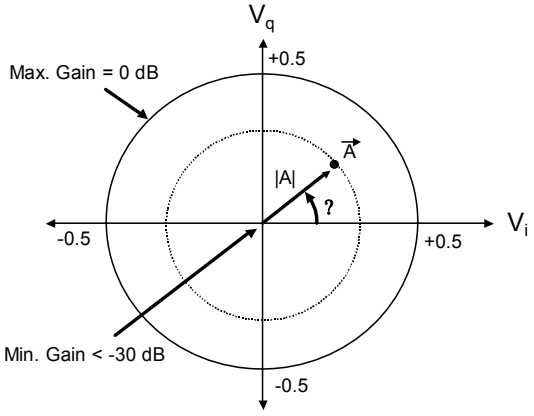

Figure 2. Vector Gain Representation

EVALUATION BOARD

The evaluation board circuit schematic for the AD8341 is shown in Figure 3. This evaluation board is shipped from the factory without the following components: C11, C12, R1, R3, R7, R9, R16, R17, R18, R19, R20 and R21. These uninstalled components may be installed for optional configurations, as described below.

The evaluation board RF input, J1, is driven from a single-ended 50 Ω source. Although the input of the AD8341 is differential, it may be driven single-ended, as provided for on the eval board, with no loss of performance.

The lowpass corner frequency of the baseband I and Q channels can be reduced by installing capacitors in positions C11 and C12. The lowpass corner frequency for either channel is approximated by

$$f_{3dB} \approx \frac{50kHz \times 10nF}{C_{external} + 0.5pF}$$

It is important to note that this is an approximation that has been derived from small signal simulation. The actual lowpass corner frequency may be slightly different than that predicted by this expression.

The I and Q baseband input circuitry on this evaluation board are identical to each other, so the following description applies equally to each. The connections and circuit configuration for the Q baseband input are described below.

The baseband input of the AD8341 requires a differential voltage drive. In the default condition, the evaluation board is set up to allow such drive by connecting the differential voltage source to QBBP, J4, and QBBM, J5. The common mode voltage should be maintained at approximately 0.5 V.

The baseband input of the evaluation board may also be driven with a single-ended voltage. In this case, a 0 Ω resistor is installed in position R18, W1 is installed, R16 remains open, and R17 and/or W2 also remain open. R10 is adjusted to apply the center voltage of the baseband input voltage range (e.g., 0.5 V with reference to common). Then, the baseband drive signal is applied to QBBP, J4. It is equally acceptable to provide a DC bias voltage to the P baseband input by installing the W2 link and a 0 Ω resistor in position R17 and to drive the M port with the baseband signal.

The voltage at the wiper of R10 can also be used to establish a common-mode voltage at pins QBBP and QBBM, by installing a 0 Ω resistor at R16 and by installing resistors at R1 and R3. In this case, the values of R1 and R3 should be the appropriate value to terminate the transmission lines that are driving QBBP, J4, and QBBM, J5.

Setting SW1 in position A disables the AD8341 output amplifier. With SW1 set to position B and no external voltage applied to Output Disable, J6, the output amplifier is enabled. With SW1 set to position B, a voltage signal such as a pulse can be applied to Output Disable, J6, to exercise the output amplifier disable function.

Table 4. Evaluation Board Configuration Options

Component	Function	Default Conditions
R7, R9, R11, R14, R15, R19, R20, R21, C15, C19, W3, W4	**I Channel Baseband Interface**. Resistors R7 and R9 may be installed to accommodate a baseband source that requires a specific terminating impedance. Capacitors C15 and C19 are bypass capacitors. The voltage divider comprised of fixed resistors R14 and R15 and potentiometer R11 can optionally be used to provide a common mode voltage of 0.5 V to the I baseband input by installing a 0 Ω resistor in position R19 and suitably-valued resistors in positions R7 and R9. The baseband input may be driven from a single-ended voltage source, which ranges from 0 V wrt common to 1.0 V wrt common, by setting R11 to produce 0.5 V at its wiper and installing W4, leaving W3 open, if the baseband port that will be driven by an external generator is IBBM, J3. If the baseband input to be driven is IBBP, J2, then install jumper W3 only.	R7, R9, R19 = Not Installed R11 = Potentiometer, 2 kΩ, 10 turn (Bourns) R14 = 4 kΩ (Size 0603) R15 = 44 kΩ (Size 0603) R20. R21 = 0 Ω (Size 0603) C15, C19 = 0.1 μF (Size 0603) W3, W4 = jumper
R1, R3, R10, R12, R13, R16, R17, R18, C16, C20, W1, W2	**Q Channel Baseband Interface**. (See "I Channel Baseband Interface")	R1, R3, R16 = Not Installed R10 = Potentiometer, 2 kΩ, 10 turn (Bourns) R12 = 4 kΩ (Size 0603) R13 = 44 kΩ (Size 0603) R17. R18 = 0 Ω (Size 0603) C16, C20 = 0.1 μF (Size 0603) W1, W2 = jumper
C11, C12	**Baseband Lowpass Filtering**. By adding capacitor C11 between **QFLP** and **QFLM**, and C12 between **IFLP** and **IFLM**, the 3 dB lowpass corner frequency of the baseband interface can be reduced from 200 MHz (nominal) as given by the equation in the Evaluation Board section of this data sheet.	C1, C2 = Not Installed
T1, C17, C18	**Output Interface**. The 1:1 balun transformer, T1, converts the 50 Ω differential output to 50 Ω single-ended. C17 and C18 are DC blocks.	C17, C18 = 100 pF (Size 0603) T1 = ETC1-1-13 (Tycoelectronics M/A-COM)
L3, L4, C5, C6	**Input Interface**. The input impedance of the AD8341 requires ~1.2 nH inductors in series with **RFIP** and **RFIM** for optimal perfromance when driven by a single-ended 50 Ω line. The inductance and mounting parasitics of 0402 0 Ω resistors provide approximately the required inductance values. C5 and C6 are DC blocks.	L3, L4 = 0 Ω (Size 0402) C5, C6 = 100 pF (Size 0603)
R2, R4, R6, C7, C8, C3, C4, C9, C10, C1, C2, C14, L1, L2	**Supply Decoupling**	C2, C4, C7, C9, C14 = 0.1 μF (Size 0603) C1, C3, C8, C10 = 100 pF (Size 0603) R2, R4, R6 = 0 Ω (Size 0603) L1, L2 = 120 nH (Size 0603)
C5, C6, C17, C18	**DC Blocks on RF Input and Output**	C5, C6, C17, C18 = 100 pF (Size 0603)
R8, SW1	**Output Disable Interface**. The output stage of the AD8341 is disabled by applying a high voltage to the **DSOP** pin, either via SW1 switched to position A, or by switching SW1 to position B and applying a high voltage to J6. The output stage is enabled via the pulldown resistor R8 when SW1 is switched to position B and no voltage, or a voltage less than the threshold value, is applied to J6.	R8 = 10 kΩ (Size 0603) SW1 = SPDT

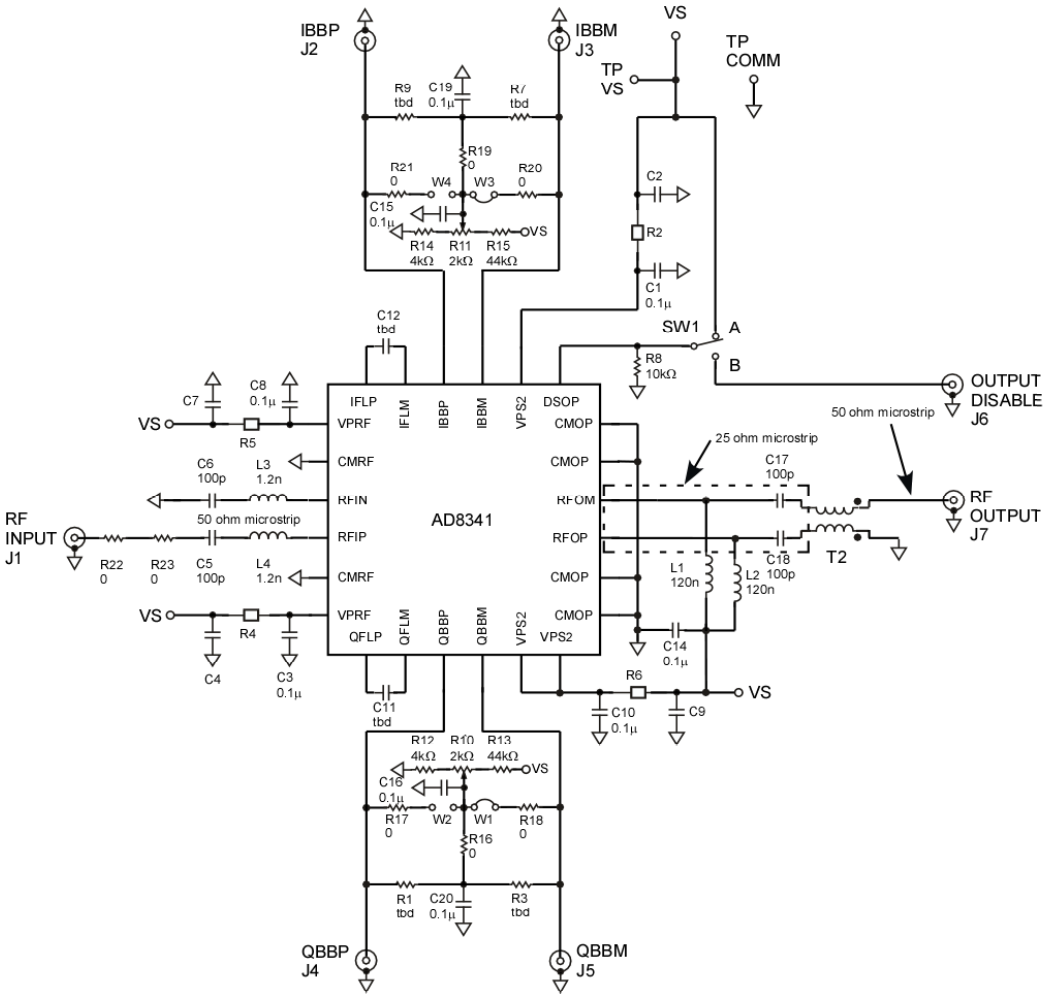

Figure 2. Evaluation Board Schematic

OUTLINE DIMENSIONS

ANALOG DEVICES

24-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-24)
Dimensions shown in millimeters

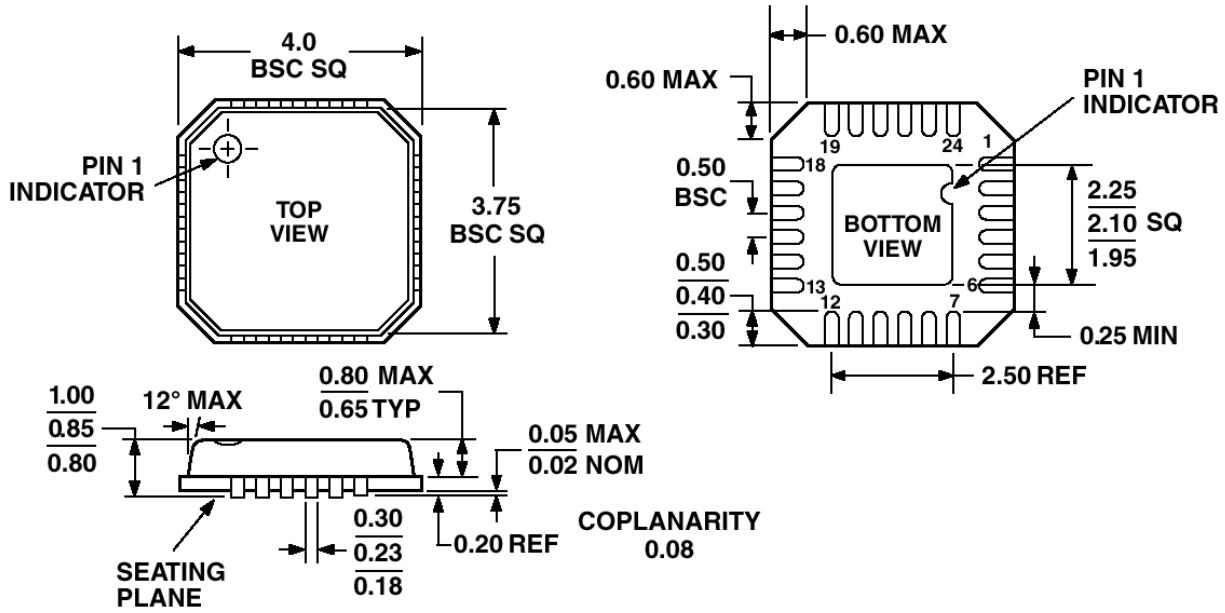

Figure 3. 24-Lead Lead Frame Chip Scale Package

PR04700-0-2/04(PrL)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8341 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 5. Ordering Guide

AD8341 Products	Temperature Package	Package Description	Package Outline	Branding
AD8341ACP	–40°C to +85°C	24-Lead LFCSP	CP-24	
AD8341-EVAL		Evaluation Board		