TC532000AP/AF

SILICON STACKED GATE CMOS

262,144 WORD x 8 BIT CMOS MASK ROM

Description

The TC532000AP/AF is a 2,097,152 bit read only memory organized as 262,144 words by 8 bits.

The TC532000AP/AF is fabricated using Toshiba's advanced CMOS technology which results in high speed and low power features: an access time of 150ns, an operating current of 40mA at 6.7MHz, and a standby current of 20μA.

The TC532000AP/AF has a programmable chip enable input ($\overline{\text{CE}}$/CE) for device selection.

The TC532000AP/AF is packaged in a standard 600mil 32-pin DIP or 525mil 32-pin SOP.

Features

- Single 5V power supply
- Access time : 150ns (max.)
- Power dissipation
  - Operating current : 40mA (max.)
  - Standby current : 20μA (max.)
- Inputs and outputs TTL compatible
- Three state outputs
- Fully static operation
- Programmable chip enable
- Package

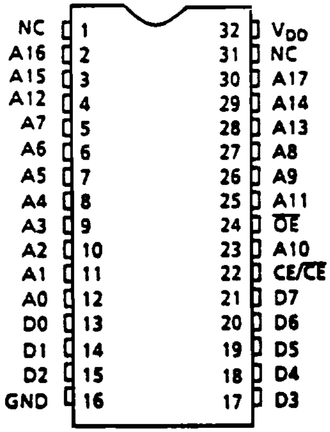
  TC532000AP : DIP32-P-600

  TC532000AF : SOP32-P-525

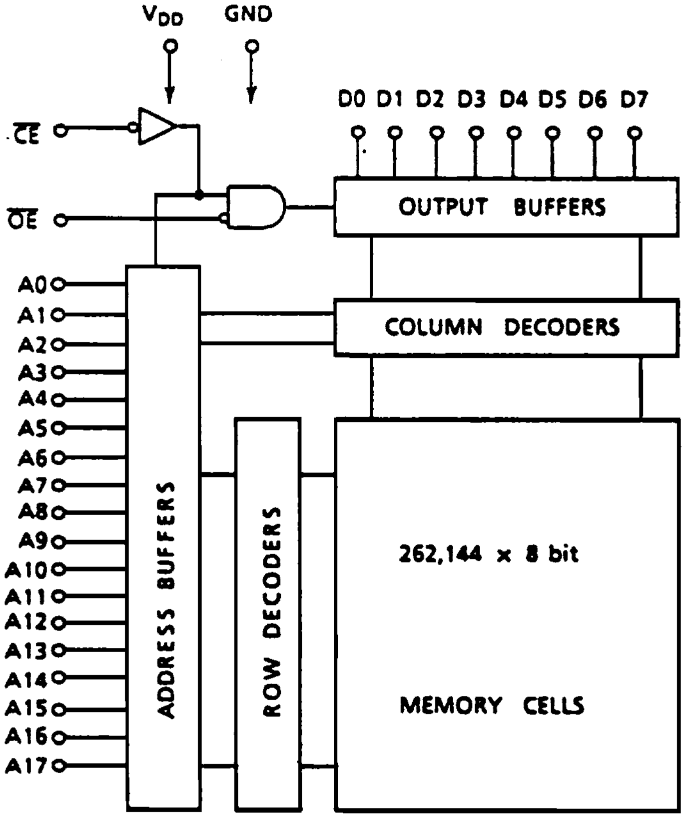
Pin Names

A0 ~ A17	Address Inputs
D0 ~ D7	Data Outputs
$\overline{\text{OE}}$	Output Enable Input
CE/$\overline{\text{CE}}$	Chip Enable Input
V_{DD}	Power Supply Voltage (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	A0 ~ 17	OUTPUTS	POWER
Read	L(H)	L	Valid	Data Out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	H	*	High-Z	Operating

H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-0.5 ~ V_{DD}	
V_{OUT}	Output Voltage	0 ~ V_{DD}	
P_D	Power Dissipation	1.0/0.6*	W
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

* SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3	–	0.8	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	–	±5.0	
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-1.0	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	2.0	–	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	–	2	
I_{DDS2}		$\overline{CE} = V_{DD}$ and $V_{IN} = 0V/V_{DD}$	–	20	μA
I_{DDO1}	Operating Current	$V_{IN} = V_{IH}/V_{IL}$, $t_{cycle} = 150ns$	–	50	mA
I_{DDO2}		$V_{IN} = V_{DD}/0V$, $t_{cycle} = 150ns$	–	40	

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	–	ns
t_{ACC}	Address Access Time	–	150	
t_{CE}	Chip Enable Access Time	–	150	
t_{OE}	Output Enable Access Time	–	70	
t_{CED}	Output Disable Time from $\overline{CE}$	0	60	
t_{OED}	Output Disable Time from $\overline{OE}$	0	60	
t_{OH}	Output Hold Time	5	–	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Times	5ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	–	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	–	10	

*This parameter is periodically sampled and is not 100% tested.

Timing Waveforms