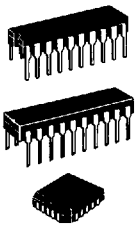
Quad CMOS to PECL* Translator

MC10H352



L SUFFIX
CERAMIC PACKAGE
CASE 732–03

P SUFFIX
PLASTIC PACKAGE
CASE 738–03

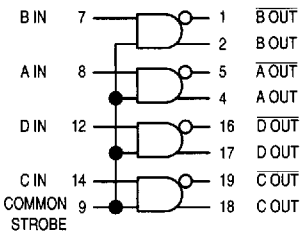
FN SUFFIX
PLCC
CASE 775–02

The MC10H352 is a quad translator for interfacing data between a CMOS logic section and the PECL section of digital systems when only a +5.0 Vdc power supply is available. The MC10H352 has CMOS compatible inputs and PECL complementary open–emitter outputs that allow use as an inverting/non–inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state (≈ +3.2 V) and all inverting outputs to the PECL high logic state (≈ +4.1 V).

The MC10H352 can also be used with the MC10H350 to transmit and receive CMOS information differentially via balanced twisted pair lines.

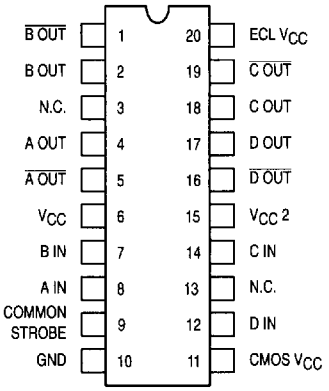
- Single +5.0 V Power Supply
- All V_{CC} Pins Isolated On Chip
- Differentially Drive Balanced Lines
- t_{pd} = 1.3 nsec Typical

LOGIC DIAGRAM



V_{CC} (+5.0 VDC) = PINS 6, 11, 15, 20
GND = PIN 10

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

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MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply	V_{CC}	0 to +7.0	Vdc
Input Voltage (V_{CC} = 5.0 V)	V_I	0 to V_{CC}	Vdc
Output Current— Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range— Plastic — Ceramic	T_{stg}	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC1} = V_{CC2} = 5.0 V ± 5.0%)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ECL	—	50	—	45	—	50	mA
	TTL	—	20	—	15	—	20	mA
Reverse Current Pins 7, 8, 12, 14 Pin 9	I_R	 — —	 25 100	 — —	 20 80	 — —	 25 100	µA
Forward Current Pins 7, 8, 12, 14 Pin 9	I_F	 — —	 –0.8 –3.2	 — —	 –0.6 –2.4	 — —	 –0.8 –3.2	mA
Input Voltage Breakdown	$V_{(BR)in}$	5.5	—	5.5	—	5.5	—	Vdc
Input Clamp Voltage (I_{in} = –18 mA)	V_I	—	–1.5	—	–1.5	—	–1.5	Vdc
High Output Voltage (1)	V_{OH}	3.98	4.16	4.02	4.19	4.08	4.27	Vdc
Low Output Voltage (1)	V_{OL}	3.05	3.37	3.05	3.37	3.05	3.37	Vdc
High Input Voltage	V_{IH}	3.15	—	3.15	—	3.15	—	Vdc
Low Input Voltage	V_{IL}	—	1.5	—	1.5	—	1.5	Vdc

(1) With V_{CC} at 5.0 V. V_{OH}/V_{OL} change 1:1 with V_{CC}.
*Positive Emitter Coupled Logic

AC PARAMETERS

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Propagation Delay (1)	t_{pd}	0.4	1.9	0.4	2.0	0.4	2.1	ns
Rise Time (20% to 80%)	t_r	0.4	1.9	0.4	2.0	0.4	2.1	ns
Fall Time (80% to 20%)	t_f	0.4	1.9	0.4	2.0	0.4	2.1	ns
Maximum Operating Frequency	f_{max}	150	—	150	—	150	—	MHz

(1) Propagation delay is measured on this circuit from $V_{CC}/2$ on the input waveform to the 50% point on the output waveform.

NOTE:

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to $V_{CC} - 2.0$ Vdc.

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