

OBJECTIVE SPECIFICATIONS

Features

- 8-latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ($I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

74AHCT: -40°C to +85°C
54AHCT: -55°C to +125°C

Function Table

(Each Latch)			
Inputs			Output
\overline{OC}	Enable C	D	\overline{Q}
L	H	D	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

Octal D-Type Transparent Latches with 3-State Outputs

Description

The '563 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

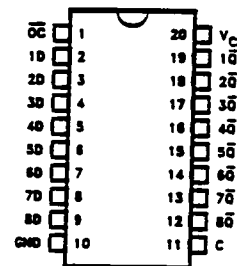
The latches are transparent: when the enable (C) is high, the Q outputs follow complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (\overline{OC}) which places the outputs at a high-impedance state when it is taken high. The \overline{OC} signal does not effect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

Fabrication using ISI proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

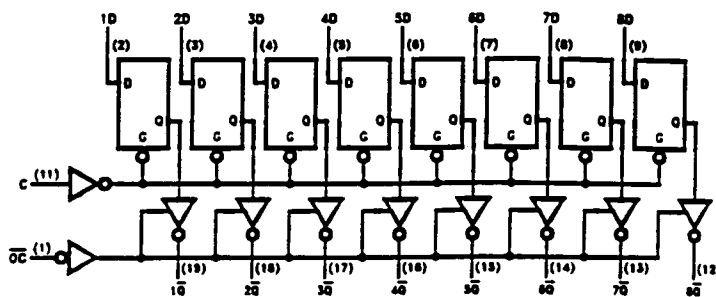
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Configuration



0052-1

Logic Diagram



0052-2

Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 70 mA
 Continuous Current Through
 V_{CC} or GND pins ± 250 mA
 Storage Temperature Range, T_{STG} $-65^\circ C$ to $+150^\circ C$
 Power Dissipation Per Package, P_D * 500 mW

*Power Dissipation temperature derating:
 Plastic Package (N): $-12mW/^\circ C$ from $65^\circ C$ to $85^\circ C$
 Ceramic Package (J): $-12mW/^\circ C$ from $100^\circ C$ to $125^\circ C$

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} 0V to V_{CC}

Operating Temperature

Range 74AHCT: $-40^\circ C$ to $+85^\circ C$
 54AHCT: $-55^\circ C$ to $+125^\circ C$

Input Rise & Fall Times, t_r , t_f Max 500 ns

*Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$ Unless Otherwise Specified)

Sym	Parameter	Test Conditions	$T_A = 25^\circ C$			74AHCT	54AHCT	Unit
			Typ	Guaranteed Limits		$T_A = -40^\circ C$ to $+85^\circ C$	$T_A = -55^\circ C$ to $+125^\circ C$	
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V	
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V	
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20 \mu A$ $I_O = -6 mA$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V	
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = 20 \mu A$ $I_O = 12 mA$ $I_O = 24 mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA	
I_{OZ}	Maximum 3-State Leakage Current	Output Enable = V_{IH} $V_{OUT} = V_{CC}$ or GND		± 0.5	± 5.0	± 10.0	μA	
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$		8.0	80.0	160.0	μA	

AC Electrical Characteristics (Input $t_r, t_f \leq 2$ ns), AHCT563

Sym	Parameter	Conditions •	$T_A = 25^\circ\text{C}$	74AHCT	54AHCT	Unit
			$V_{CC} = 5.0\text{V}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V } \pm 10\%$	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V } \pm 10\%$	
			Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay, D to Q	$C_L = 50$ pF	8	14	17	ns
		$C_L = 150$ pF	14	23	28	
t_{PHL}		$C_L = 50$ pF	8	14	17	ns
		$C_L = 150$ pF	14	23	28	
t_{PLH}	Maximum Propagation Delay, C to any Q	$C_L = 50$ pF	14	23	27	ns
		$C_L = 150$ pF	20	32	38	
t_{PHL}		$C_L = 50$ pF	14	23	27	ns
		$C_L = 150$ pF	20	32	38	
t_{PZH}	Maximum Output Enable Time, \overline{OC} to any Q	$R_L = 1K\Omega$ $C_L = 50$ pF	12	20	24	ns
		$C_L = 150$ pF	18	29	35	
t_{PZL}		$C_L = 50$ pF	12	20	24	ns
		$C_L = 150$ pF	18	29	35	
t_{PHZ}	Maximum Output Disable Time	$R_L = 1K\Omega$	8	13	16	ns
t_{PLZ}	\overline{OC} to any Q	$C_L = 50$ pF	8	13	16	
t_w	Minimum Pulse Width, C High		6	10	10	ns
t_{in}	Minimum Setup Time, D before C \downarrow		6	10	10	ns
t_h	Minimum Hold Time, D after C \downarrow		3	5	7	ns
C_{IN}	Maximum Input Capacitance		5			pF
C_{OUT}	Maximum Output Capacitance	Output Disabled	10			pF

AC Electrical Characteristics (Input $t_r, t_f \leq 2$ ns), AHCT563

Sym	Parameter	Conditions •	$T_A = 25^\circ C$ $V_{CC} = 5.0V$	74AHCT $T_A = -40^\circ C$ to $+85^\circ C$ $V_{CC} = 5.0V \pm 10\%$	54AHCT $T_A = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits		
C_{PD}	Power Dissipation Capacitance* (per stage)	$\overline{OC} = V_{CC}$	5			pF
		$\overline{OC} = GND$	30			

* C_{PD} determines the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

• For AC switching test circuits and timing waveforms see section 2.